VLSI DESIGN

VII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
AEC017	Core	L	T	P	C	CIA	SEE	Total
		3	1	-	4	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

OBJECTIVES:

The course should enable the students to:

I. Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II. Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III. Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout.
IV. Focus in selecting appropriate building blocks of data path for given system.

COURSE OUTCOME:

CO I: Explore the basic operations of MOSFET, parameters to be considered which effects the operation of MOS, effect of scaling on MOS devices, how to overcome draw back.
CO II : Understand various VLSI design styles, fabrication process of MOS, able to analyze the inverter Characteristics, understand the delay, noise margin and power dissipation of MOS transistor.
COIII: Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up.
CO IV: Understand various gate level designs, analyze various performance parameters like area, speed and capacitance and study the Fan-In and Fan-out.
CO V: Understand design options for common datapath operators, various memories, low power memories. Analyze various timing issues, clocking strategies of VLSI designs and study various digital designs.

COURSE LEARNING OUTCOME:

1. Understand fundamentals of MOS devices and its V-I characteristics.
2. Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
3. Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
4. Understand the basic CMOS nano technology and the importance of it.
5. Understand the fabrications steps involved in the MOS transistor.
6. Study various inverter characteristics of NMOS, CMOS.
7. Understand the effect of delay, noise margin and power dissipation of MOS devices.
8. Understand implementation of logic designs using MOS transistors series & parallel circuits.
9. Study other logic families like pass transistor logic, Bi-CMOS logic and various pull-up networks.
10. Understand to implement layers using stick diagram along with the color representation.
11. Study the design rules of transistors, wires, contacts and layouts with respect to width, length and spacing based on type of technology.
12. Understand effects on VLSI Interconnects and electron migration.
13. Study the latch up problems and reliability issues of CMOS.
14. Understand various gate level designs for the logics and study about Fan-In and Fan-out.

15. Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
16. Understand the implementation strategies of VLSI design.
17. Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
18. Understand data path subsystem designs, array subsystem designs
19. Understand the operation of various static and dynamic latches and registers.
20. Analyze the timing issues and the clock strategies of VLSI designs.
21. Understand the purpose and operation of Low power memory Circuits.
22. Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

UNIT-I	**MOSFETS**	**Classes: 08**

Fundamentals of MOSFETs; Weak & strong inversion conditions; Threshold voltage concept in MOSFETs; Current - voltage characteristics of a MOSFET; MOSFET parasitics; Trends & projections in VLSI design & technology; Scaling in MOS devices; Effects in scaling of MOS devices; BiCMOS technologies; CMOS nanotechnology.

UNIT-II	**VLSI DESIGN STYLES**	**Classes: 09**

NMOS, PMOS and CMOS fabrication Flow; Noise Margin; Inverter Threshold Voltage; NMOS inverter design and characteristics; CMOS inverter design and properties; Delay and power dissipation; Parallel & series equivalent circuits; Pass transistor; Various pull ups; Bi-CMOS inverters

UNIT-III	**VLSI PHYSICAL DESIGN**	**Classes: 09**

Stick Diagrams; Physical design rules: 2 μm and lambda CMOS design rules for wires, contacts and transistors; Layout design; Euler's rule for physical design.

VLSI Interconnects; Reliability issues in CMOS VLSI; Latching; Electromigration.

UNIT-IV	**LOGIC DESIGN AND IMPLEMENTATION STRATEGIES**	**Classes: 09**

Gate Level Design: Complex gates; Switch logic; Transmission gates; Static and dynamic CMOS design; Time delays; Driving large capacitive loads; Wiring capacitances; Fan-in and Fan-out; Choice of layers implementation strategies full custom and semi custom design; Standard cell design and cell libraries; Programmable logic devices; CPLDs; FPGA building block architectures; FPGA interconnect routing procedures; Speed and area tradeoff.

UNIT-V	**SUB SYSTEM DESIGN**	**Classes: 10**

Data Path Sub Systems: Sub system design; Shifters; Adders; ALUs; Multipliers; Parity generators; Comparators; Zero/one detectors; Counters Array Subsystems: SRAM; DRAM; ROM; Serial access Memories; Static and dynamic latches and registers; Timing issues; Clock strategies; Low power memory Circuits; Synchronous and asynchronous circuit design.

Text Books:

1. A. Pucknell, Kamran Eshraghian, "BASIC VLSI Design," Third Edition, Prentice Hall of India, 2007. ISBN: 978- 81- 203- 0986- 9
2. R. Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation," Wiley-IEEE Press, USA, 2005. ISBN: 978-0-470-88132-3
3. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective," Second Edition, Phi Learning, 2009. ISBN: 9788120322578

Reference Books:

1. N. Weste, K. Eshraghian, “Principles of CMOS VLSI Design”, Second Edition, Addision Wesley, 1993. ISBN: 978-81-317-1942-8
2. M.J. Smith, “Application Specific Integrated Circuits”, Addisson Wesley, First edition, 1997. ISBN-13: 978-0321602756
3. John P. Uyemura, “CMOS Logic Circuit Design,” Springer, USA, 2007. ISBN: 0-7923-8452-0

Web References:

1. http://www.nptel.ac.in/downloads/117101058/
2. https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

E-Text Books:

1. http://www.csit-sun.pub.ro/courses/vlsi/Modern_VLSI_Design.pdf
2. http://ic.sjtu.edu.cn/ic/wp-content/uploads/sites/10/2013/04/CMOS-VLSI-design.pdf