INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE DESCRIPTOR

Course Title	DIGITAL ELECTRONICS				
Course Code	AECB03				
Programme	B.Tech				
Semester	III	EEE			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	0	3	-	-
Chief Coordinator	Ms.V.Bindusree, Assistant professor.				
Course Faculty	Ms.J.Sravana, Assistant professor.				

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
-	-	-	-

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
DIGITAL ELECTRONICS	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**			**Total Marks**
Type of Assessment	CIE Exam	Quiz	AAT	
CIA Marks	20	05	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz - Online Examination

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

Alternative Assessment Tool (AAT)

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	1	Presentation on real-world problems
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Seminar
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Term Paper

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Problem Solving**: Exploit the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work.	1	Seminar
PSO 2	**Professional Skills:** Identify the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering, and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally.	-	-
PSO 3	**Modern Tools in Electrical Engineering:** Comprehend the technologies like PLC, PMC, process controllers, transducers and HMI and design, install, test, maintain power systems and industrial applications.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES :

The course should enable the students to:	
I	Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra.
II	Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip flops and latches.
III	Understand about synchronous and asynchronous sequential logic circuits.
IV	Analyze and design analog to digital and digital to analog Converters.
V	Impart the basic understanding of memory organization, ROM, RAM, CPLD, FPGA, and CCD.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Understand the basic concept of number systems and integrated circuits.	CLO 1	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.
		CLO 2	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements
		CLO 3	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.
		CLO 4	Design TTL/CMOS integrated circuits and study the TTL and CMOS logic families.
CO 2	Analyze Combination logic circuit such as multiplexers, adders, decoders	CLO 5	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
		CLO 6	Design Gate level minimization using KMaps and realize the Boolean function using logic gates.

		CLO 7	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.
		CLO 8	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit.
		CLO 9	Discuss about MSI chip, ALU design.
COs	**Course Outcome**	**CLOs**	**Course Learning Outcome**
CO 3	Understand about synchronous and asynchronous sequential logic circuits.	CLO 10	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops.
		CLO 11	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
		CLO 12	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
		CLO 13	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
		CLO 14	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CO 4	Analyze analog to digital and digital to analog Converters.	CLO 15	Understand the classifications, characteristics and need of data converters such as ADC and DAC.
		CLO 16	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC
		CLO 17	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters, Dual slope converter.
		CLO 18	Implement the A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters
CO 5	Understanding of memory organization, ROM, RAM, CPLD, FPGA, and CCD.	CLO 19	Understand the concept of memory organization, Read only memory and random access memory.
		CLO 20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.
		CLO 21	Analyze the concepts of CAM, FPGA.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB03.01	CLO 1	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.	PO 1	1
AECB03.02	CLO 2	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.	PO 1	1
AECB03.03	CLO 3	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.	PO 1	1
AECB03.04	CLO 4	Design TTL/CMOS integrated circuits and study the TTL and CMOS logic families.	PO 4	3
AECB03.05	CLO 5	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method	PO 4	3
AECB03.06	CLO 6	Design Gate level minimization using KMaps and realize the Boolean function using logic gates.	PO 4	3
AECB03.07	CLO 7	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	PO 1	1

AECB03.08	CLO 8	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit.	PO 4	3
AECB03.09	CLO 9	Discuss about MSI chip, ALU design.	PO2	2
AECB03.10	CLO 10	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops	PO 4	3
AECB03.11	CLO 11	Analyze and apply the design procedures of small sequential circuits to build the gated latches.	PO 4	3
AECB03.12	CLO 12	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers	PO 4	3
AECB03.13	CLO 13	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 4	3
AECB03.14	CLO 14	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	PO 4	3
AECB03.15	CLO 15	Understand the classifications, characteristics and need of data converters such as ADC and DAC.	PO 1	1
AECB03.16	CLO 16	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC	PO 1	1
AECB03.17	CLO 17	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters, Dual slope converter.	PO 4	3
AECB03.18	CLO 18	Implement the A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters	PO 4	3
AECB03.19	CLO 19	Understand the concept of memory organization, Read only memory and random access memory.	PO 1	1
AECB03.20	CLO 20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	PO 4	2
AECB03.21	CLO 21	Analyze the concepts of CAM, FPGA.	PO 2	2

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

Course Outcomes (COs)	Program Outcomes (POs)			
	PO 1	PO 2	PO 4	PSO2
CO 1	1			
CO 2		2	3	
CO 3	1		3	
CO 4	1		3	
CO 5			3	1

3= High; 2 = Medium; 1 = Low

XII MAPPING COURSE LEARNING OUTCOMES LEADING TOTHEACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	1														
CLO 2	1														
CLO 3	1														
CLO 4				3											
CLO 5				3											
CLO 6				3											
CLO 7	1														
CLO 8				3											
CLO 9		2												2	
CLO 10				3											
CLO 11				3											
CLO 12				3											
CLO 13				3											
CLO 14				3										2	
CLO 15	1														
CLO 16	1														
CLO 17				3											
CLO 18				3											
CLO 19	1														
CLO 20				3										2	
CLO 21		2												2	

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XIII.ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO1, PO2, PO4,PSO2	SEE Exams	PO1, PO2, PO4,PSO2	Assignments	-	Seminars	PO1, PO2, PO4,PSO2
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO1, PO2, PO4,PSO2						

XIV.ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV.SYLLABUS

Module-I	**FUNDAMENTALS OF DIGITAL SYSTEMS AND LOGIC FAMILIES**
Digital signals, digital circuits, AND, OR, NOT, NAND, NOR and Exclusive-OR operations, Boolean algebra, examples of IC gates, number systems-binary, signed binary, octal hexadecimal number, binary arithmetic, one's and two's complements arithmetic, codes, error detecting and correcting codes, characteristics of digital lCs, digital logic families, TTL, Schottky TTL and CMOS logic, interfacing CMOS and TTL, Tri-state logic.	
Module-II	**COMBINATIONAL DIGITAL CIRCUITS**
Standard representation for logic functions, K-map representation, and simplification of logic functions using Kmap, minimization of logical functions. Don't care conditions, Multiplexer, DeMultiplexer, Decoders, Adders, Sub tractors, BCD arithmetic, carry look ahead adder, serial adder, ALU, elementary ALU design, popular MSI chips, digital comparator, parity checker/generator, code converters, priority encoders, decoders, drivers for display devices, Q-M method of function realization.	
Module-III	**SEQUENTIAL CIRCUITS AND SYSTEMS**
1-bit memory, the circuit properties of Bi-stable latch, the clocked SR flip flop, J- K-T and D types flip flops, applications of flip flops, shift registers, applications of shift registers. Serial to parallel converter: Parallel to serial converter, ring counter, sequence generator, ripple (Asynchronous) counters, synchronous counters, counters design using flip flops, special counter IC's, asynchronous sequential counters, applications of counters.	
Module-IV	**A/D AND D/A CONVERTERS**
Digital to analog converters: weighted resistor, converter, R-2R Ladder D/A converter, specifications for D/A converters, examples of D/A converter lCs, sample and hold circuit, analog to digital converters: quantization and encoding, parallel comparator A/D converter, successive approximation A/D converter, counting A/D converter, dual slope A/D converter, A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters, example of A/D converter ICs.	
Module-V	**SEMICONDUCTOR MEMORIES AND PROGRAMMABLE LOGIC DEVICES**
Memory organization and operation, expanding memory size, classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM), content addressable memory (CAM), charge de coupled device memory (CCD), commonly used memory chips, ROM as a PLD, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).	
Text Books:	
1. P Jain, "Modern Digital Electronics", McGraw Hill Education, 2009 2. M M Mano, "Digital logic and Computer design", Pearson Education India, 2016. 3. D. Roy Chowdhury, "Linear Integrated Circuits", New age international (p) Ltd, 2nd Edition, 2003. 4. Ramakanth A. Gayakwad, "Op-Amps & linear ICs", PHI, 3rd Edition, 2003. 5. John F. Wakerly, "Digital Design Principles and Practices", Prentice Hall, 3rd Edition, 2005	

Reference Books:
1. A Kumar, "Fundamentals of Digital Circuits", Prentice Hall India, 2016. 2. Salivahanan, ―Linear Integrated Circuits and Applications‖, TMH, 1st Edition, 2008.

XIV.COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-5	Understand the need for digital systems, review of number systems, number base conversion	CLO 1	T1:1.5-1.7 R1:1.6-1.8
6-8	Complements of numbers, codes-binary codes, BCD code and its Properties.	CLO 2	T1:1.7 R1:1.9
9-11	Unit distance code, alphanumeric codes, and error detecting and correcting codes	CLO 2	T1:1.7 R1:2.0
12-13	Design and analyze the combinational circuits using TTL/CMOS logic.	CLO 3	T3:10.3 R2:5.4
14-16	Design and analyze the sequential circuits using TTL/CMOS logic.	CLO 4	T5:3.12 R2:12.7
17-19	Identify basic building blocks of digital systems and Minimization using three variable; four variable; five variable K-Maps; Don‘t Care Conditions.	CLO 5	T1:2.8
20-22	Design functions using universal gates. NAND and NOR Implementation; Other Two-Level Implementation; Exclusive –OR function.	CLO 6	T2:0.1
23-25	Combinational design, arithmetic circuits- adders, substractors.	CLO 7	T1:4.1-4.9 R1:4.2-4.6
26-30	Design different combinational logic circuits comparators Multiplexers,Demultiplexer,Decoder	CLO 8	T1:3.1
31-32	Understand the elementary ALU design, popular MSI chips	CLO 9	T2:3.2
33-36	Combinational and sequential circuits, the binary cell, the Fundamentals of sequential machine operation.	CLO 10	T1:5.3-5.5 R1:5.0-5.2
37-40	Flip-flop, D-Latch Flip-flop, “Clocked T” Flip-flop, “Clocked JK“Flip-flop.	CLO 11	T1:5.3-5.5 R1:5.3-5.4
41-42	Shift Registers	CLO 12	T1:6.1-6.5 R1:6.1-6.3
43-45	Synchronous, Asynchronous Counters	CLO 13	R2:21.33
46-47	Excitation tables of Flip-flops	CLO 14	T1:5.3-5.5 R1:5.3-5.4
48	Discuss the classifications of data converters	CLO 15	T3:9.2-9.7
49-51	Discuss and Analyze DAC techniques and characteristics.	CLO 16	T3:10.1
52-54	Discuss and Analyze ADC techniques and characteristics	CLO 17	T3:10.2
55-57	Discuss and Analyze the voltage to frequency converters	CLO 18	T3:9.2-9.7
58	Discuss flash memory ,dual slope	CLO 19	T2:27.4 R2:21.68
59-60	classification and characteristics of memories, sequential memory, read only memory (ROM), read and write memory(RAM),	CLO 20	T2:27.7 R2:21.74
61	Discuss and analyze PLA,PAL,PLD	CLO 21	T2:27.12 R2:21.75

62	FPGA	CLO 22	T2:27.19 R2:21.814

XV.GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S NO	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POs	RELEVANCE WITH PSOs
1	Practical use of number systems.	Seminars	PO 1	PSO 2
2	Application of flip-flops and latches	Seminars / NPTEL	PO 4	PSO 2
3	Designing of circuits using flip-flops and latches.	NPTEL	PO 2	PSO 2

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