DIGITAL LOGIC DESIGN

III Semester: IT/CSE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC020	Core	3	1	-	4	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

OBJECTIVES:

The course should enable the students to:

I. Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra.
II. Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip flops and latches.
III. Understand about synchronous and asynchronous sequential logic circuits.
IV. Impart the basic understanding of memory organization, ROM, RAM, PLA and PAL.

COURSE LEARNING OUTCOMES (CLOs):

1. Understand the basic concept of number systems, binary addition and subtraction for digital systems.
2. Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.
3. Discuss about digital logic gates, error detecting and correcting codes for digital systems.
4. Describe the importance of SOP and POS canonical forms with examples.
5. Describe minimization techniques and other optimization techniques for Boolean formulas in general and digital circuits.
6. Evaluate Boolean algebra expressions by minimizing algorithms like sop and pos using Boolean Postulates and theorems.
7. Solve various Boolean algebraic functions using Karnaugh map and Tabulation Method.
8. Understand bi-stable elements and different type's combinational logic circuits.
9. Analyze the design procedures of Sequential logic circuits with the help of registers.
10. Discuss the concept of flip flops and latches by using sequential logic circuits.
11. Differentiate combinational logic circuits with sequential logic circuits along with examples.
12. Understand the concept of memory organization, read only memory and random access memory.
13. Discuss and implement combinational and sequential logic circuits using PLA and PLDs.
14. Explain the concept of memory hierarchy in terms of capacity and access time.
15. Explain about Synchronous and Asynchronous Sequential Circuits: Reduction of state tables for Mealy and Moore machines.
16. Discuss about various memory concepts with respect to temporary and permanent memory organizations.

Unit-I	NUMBER SYSTEMS AND CODES	Classes: 11

Review of number systems, number base conversion; Binary arithmetic: Binary weighted and non-weighted codes; Complements: Signed binary numbers; Error Detection and Correcting Codes; Binary logic.

Unit -II	BOOLEAN ALGEBRA AND GATE LEVEL MINIMIZATION	Classes: 09

Postulates and theorems; representation of switching functions; SOP and POS forms; Canonical forms; Digital logic gates; Karnaugh Maps: Minimization using three variable; four variable; five variable KMaps; Don't Care Conditions; NAND and NOR implementation; Other Two-Level Implementation; Exclusive –OR function.

Unit -III	DESIGN OF COMBINATIONAL CIRCUITS (CC)	Classes: 10

Combinational Circuits: Analysis and Design Procedure; Binary adder and subtractors; Carry Look-a-head adder; Binary multiplier.
Magnitude comparator;BCD adder; Decoders; Encoders; Multiplexers; Demultiplexer.

Unit -IV	DESIGN OF SEQUENTIAL CIRCUITS	Classes: 09

Combinational Vs Sequential Circuits ; Latches, Flip Flops: RS flip flop, JK flip flop, T flip flop, D flip flop, Master-Slave Flip flop, Flip Flops excitation functions; Conversion of one flip flop to another flip flop; Shift Registers; Design of Asynchronous and Synchronous circuits; State Table, State diagram, State Reduction and State Assignment for Mealy and Moore Machines.

Unit -V	MEMORY	Classes: 09

Random access memory; Types of ROM; Memory decoding; Address and Data bus; Sequential memory; Cache memory; Programmable logic arrays; Memory hierarchy in terms of capacity and access time

Text Books:

1. M. Morris Mano, Digital Design‖, Pearson Education/PHI, 3rdEdition 2001.
2. Charles H. Roth, Jr,Fundamentals of Logic Design‖, Thomson Brooks/Cole, 5thEdition, 2004.

Reference Books:

1. C. V. S. Rao, Switching Theory and Logic Design, Pearson Education, 1st Edition, 2005.
2. M. Rafiquzzaman, Fundamentals of Digital Logic & Micro Computer Design‖, John Wiley, 5th Edition, 2005.
3. Zvi. Kohavi, Switching and Finite Automata Theory‖, Tata McGraw-Hill, 2nd Edition 1991.

Web References:

1. http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf
2. http://www.engrcs.com/courses/engr250/engr250lecture.pdf
3. http://www.ece.rutgers.edu/~marsic/Teaching/DLD/slides/lec-1.pdf

E-Text Books:

1. https://drive.google.com/file/d/0B4ChICvNGHlfN2NmODE1NjAtZWI5Zi00MmU0LWIyMmQtOTU3ZGUyMzAwODc1/view
2. https://accessengineeringlibrary.com/browse/digital-logic-design-and-computer-organization-withcomputer-architecture-for-security
3. http://www.ece.rutgers.edu/~marsic/Teaching/DLD/syllabus.html