DIGITAL SYSTEM DESIGN

III Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC002	Core	3	1	-	4	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

OBJECTIVES:

The course should enable the students to:

I. Formulate and solve problems involving number systems and operations related to them and generate different digital codes.
II. Describe and analyze functions of logic gates and optimize the logic functions using K -map and Quine - McClusky methods.
III. Demonstrate knowledge of combinational and sequential logic circuits elements like Adders, Multipliers, flip-flops and use them in the design of latches, counters, sequence detectors, and similar circuits.
IV. Design a simple finite state machine from a specification and be able to implement this in gates and edge triggered flip-flops.

COURSE LEARNING OUTCOMES (CLOs):

1. Understand number systems, binary addition and subtraction, 2"s complement representation and operations with this representation and understand the different binary codes.
2. Illustrate the switching algebra theorems and apply them for reduction of Boolean function.
3. Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
4. Discuss about digital logic gates and their properties, and implement logic gates using universal gates.
5. Evaluate functions using various types of minimizing algorithms like Boolean algebra.
6. Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
7. Design Gate level minimization using K-Maps and realize the Boolean function using logic gates.
8. Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.
9. Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
10. Analyze and apply the design procedures of small sequential circuits to build the gated latches.
11. Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
12. Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
13. Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
14. Understand and analyze the design of a finite state machine and implement Moore and mealy machine.
15. Understand and analyze the merger chart methods like merger graphs, merger table for completely and incompletely specified machines.
16. Apply the concept of digital logic circuits to understand and analyze real time applications.

17. Acquire the knowledge and develop capability to succeed national and international level competitive examinations.

Unit-I	FUNDAMENTALS OF DIGITAL TECHNIQUES	Classes: 08

Review of number systems: Decimal, binary, octal and hexa decimal, base conversion methods, complements of numbers; binary codes: Binary coded decimal, excess-3, gray codes, error detecting and error correcting codes.

Unit -II	BOOLEAN ALGEBRA AND THEOREMS	Classes: 10

Boolean algebra: Postulates and theorems; Logic gates and truth tables, representation of switching functions, sum of products and product of sums forms, karnaugh map representation, minimization using karnaugh map Quine - McClusky method of minimization.

Unit -III	DESIGN OF COMBINATIONAL CIRCUITS	Classes: 08

Design of combinational circuits using conventional AND, OR, NOT, NAND, NOR and EX-OR gates; Adders and subtractors: Half adder, full adder, half subtractor, full subtractor.

Parallel adder, serial adder, carry look ahead adder, binary coded decimal adder, 1's complement subtractor, 2's complement subtractor.

Unit -IV	SEQUENTIAL CIRCUITS	Classes: 10

Flip Flops: SR flip flop, JK flip flop, D flip flop, T flip flop, excitation tables, race around condition, master slave flip flop; Counters: Design of synchronous and asynchronous counters; Shift registers: Modes of operation, bidirectional shift registers, ring counters, Johnson counters.

Unit -V	CAPABILITIES AND MINIMIZATION OF SEQUENTIAL MACHINES	Classes: 09

Synchronous sequential circuits: State table, state diagram, state assignment, state minimization; Sequential circuits example: Sequence detectors, binary counters; Mealy and Moore machines: Capabilities and limitations of finite state machine, state equivalence and machine minimization of completely specified or incompletely specified machines, partition method, Merger table and graph method.

Text Books:

1. M. Morris Mano, Michael D. Ciletti, "Digital Design", Pearson Education/PHI, 3rd Edition, 2008.
2. Zvi. Kohavi, "Switching and Finite Automata Theory", Tata McGraw Hill, 3rd Edition, 2004.
3. John M. Yarbrough, "Digital logic applications and design", Thomson publications, 2nd Edition, 2006.

Reference Books:

1. Roth, "Fundamentals of Logic Design", Cengage learning, 5th Edition, 2004.
2. A. Anand Kumar, "Switching Theory and Logic Design", Prentice Hall of India, 1st Edition, 2014.

Web References:

1. mcsbzu.blogspot.com
2. http://books.askvenkat.com/
3. http://worldclassprogramme.com/
4. http://www.daenotes.com/
5. http://nptel.ac.in/courses/117106086/1

E-Text Books:
1. https://books.google.co.in/books/about/Switching_Theory_and_Logic_Design 2. https://www.smartzworld.com/notes/switching-theory-and-logic-design-stld 3. https://www.researchgate.net/.../295616521_Switching_Theory_and_Logic_Design 4. https://books.askvenkat.com/switching-theory-and-logic-design-textbook-by-anand-kumar/ 5. http://www.springer.com/in/book/9780387285931