INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**COMPUTER ORGANIZATION**				
Course Code	**AEC010**				
Programme	**B.Tech**				
Semester	**V**	**ECE**			
Course Type	**Core**				
Regulation	**IARE - R16**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	-	-
Chief Coordinator	Mr. N V Krishna Rao, Assistant Professor				
Course Faculty	Mr. P Anjaiah, Assistant Professor Ms. G Nishwitha, Assistant Professor Ms. B Vijaya Durga, Assistant Professor				

I. COURSEOVERVIEW:

This course introduces the principles of basic computer organization, CPU organization, and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, register transfer languages, arithmetic, logic and shift micro operations, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O organization of computer, parallel processing and inter process communication and synchronization. This course in reached to student by power point presentations, lecture notes, and assignment questions,previous model question papers, multiple choice questions and question bank of long and short answers.

II. COURSEPRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Digital System Design	4

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Computer Organization	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATIONMETHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weight age in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept or to test the application skill of The concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	LPGCIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8thand 16thweek of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks

shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES AREASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	2	Presentation on real-world problems
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics,natural sciences, and engineering sciences	2	Seminar
PO3	**Design/Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations	1	Seminar

3 = High; 2= Mediumt 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES AREASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems..	2	Seminar
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	-	-
PSO 3	**Successful Career and Entrepreneurship**: An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES(COs):

The course should enable the students to:	
I	Understand the basic structure and operation of a digital computer.
II	Understand the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
III	Interpret the different types of control and the concept of pipelining.
IV	To study the different ways of communicating with I/O devices and standard I/O interfacesand RISC and CISC processors.
V	To study the hierarchical memory system including cache memories and virtual memory.

IX. COURSE OUTCOMES (COs):

Cos	Course Outcome	CLOs	Course Learning Outcome
CO 1	Ability to understand the concepts of associated with the computer system design and data representation.	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of acomputer.
		CLO 2	Understand the concepts associated with the computer organization.
		CLO 3	Describe various data representations and explain how arithmetic and logical operations are performed by computers.
		CLO 4	Understand instruction types, addressing modes and theirformats in the assembly language programs.
CO 2	Explore the concepts associated with the fixed point arithmetic operations and algorithms.	CLO 5	Describe the implementation of fixed point and floating point addition, subtraction operations.
		CLO 6	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).
		CLO 7	Describe the pipeline processing concept with multiple functional units.
		CLO 8	Understand the concept of the modified booth’s algorithm.
CO 3	Understand the concepts of Control design of a computer.	CLO 9	Understand the connections among the circuits and the functionalities in the hardwired control unit.
		CLO 10	Describe the design of control unit with address sequencing and microprogramming Concepts.
		CLO 11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.
		CLO 12	Understand the functionality of super scalar processing and Nano programming.
CO 4	Ability to learn the concepts associated with the memory organization.	CLO 13	Understand the concept of memory hierarchy and different typed of memory chips.
		CLO 14	Describe the concepts of magnetic surface recording, optical memories
		CLO 15	Understand the cache and virtual memory concept in memory organization.
		CLO 16	Describe the hardware organization of associate memory and understand the read and write operations.

Cos	Course Outcome	CLOs	Course Learning Outcome
CO 5	Explore the concepts of System Organization including types of interrupts and processors.	CLO 17	Understand the various bus control interfaces and system control interfaces.
		CLO 18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).
		CLO 19	Understand the functionally of RISC and CISC processors.
		CLO 20	Describe the concepts of superscalar and vector processor.

X. COURSE LEARNING OUTCOMES(CLOs):

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
AEC010.01	CLO 1	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of acomputer.	PO1	2
AEC010.02	CLO 2	Understand the concepts associated with the computer organization.	PO1	2
AEC010.03	CLO 3	Describe various data representations and explain howarithmetic and logical operations are performed by computers.	PO1	2
AEC010.04	CLO 4	Understand instruction types, addressing modesand theirformats in the assembly language programs.	PO1	2
AEC010.05	CLO 5	Describe the implementation of fixed point and floating point addition, subtraction operations.	PO1	3
AEC010.06	CLO 6	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).	PO2	1
AEC010.07	CLO 7	Describe the pipeline processing concept with multiple functional units.	PO1	2
AEC010.08	CLO 8	Understand the concept of the modified booth’s algorithm	PO1	1
AEC010.09	CLO 9	Understand the connections among the circuits and the functionalities in the hardwired control unit.	PO1	2
AEC010.10	CLO 10	Describe the design of control unit with address sequencing and microprogramming Concepts.	PO1	2
AEC010.11	CLO 11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.	PO1	2
AEC010.12	CLO 12	Understand the functionality of super scalar processing and Nano programming.	PO3	1
AEC010.13	CLO 13	Understand the concept of memory hierarchyand different typed of memory chips.	PO1	2
AEC010.14	CLO 14	Describe the concepts of magnetic surface recording, optical memories	PO1	2
AEC010.15	CLO 15	Understand the cache and virtual memory concept in memory organization.	PO1	2
AEC010.16	CLO 16	Describe the hardware organizationof associate memory and understand the read and write operations.	PO1	2

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
AEC010.17	CLO 17	Understand the various bus control interfaces and system control interfaces.	PO1	3
AEC010.18	CLO 18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).	PO1	2
AEC010.19	CLO 19	Understand the functionally of RISC and CISC processors.	PO3	1
AEC010.20	CLO 20	Describe the concepts of superscalar and vector processor.	PO3	1

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADINGTO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)			
	PO 1	PO 2	PO 3	PSO1
CO 1	2			
CO 2	3	1		1
CO 3	2		1	
CO 4	2			1
CO 5	3		1	1

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XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFICOUTCOMES:

CLOs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	2														
CLO 2	2														
CLO 3	2														
CLO 4	2														
CLO 5	3												1		
CLO 6		1											1		
CLO 7	2												1		
CLO 8	1														
CLO 9	2														
CLO 10	2														

CLOs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 11	2														
CLO 12			1												
CLO 13	2												1		
CLO 14	2														
CLO 15	2												1		
CLO 16	2														
CLO 17	3														
CLO 18	2														
CLO 19			1										1		
CLO 20			1										1		

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XIII. ASSESSMENTMETHODOLOGIES–DIRECT

CIE Exams	PO 1, PO 2, PO 3	SEE Exams	PO1, PO 2, PO3	Assignments	PO3	Seminars	PO2, PO 3
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 1, PO 2, PO 3						

XIV. ASSESSMENTMETHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

UNIT-I	INTRODUCTION
Computing and computers, evolution of computers, VLSI Era, System design, register level, processor level, CPU organization, data representation, fixed-point numbers, floating point numbers, instruction formats, instruction types, addressing modes.	
UNIT-II	**DATA PATH DESIGN**
Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division, Combinational and Sequential ALUs, Carry look ahead adder, Robertson algorithm, booth's algorithm, non restoring division algorithm, Floating Point Arithmetic, Coprocessor, Pipeline Processing, Pipeline Design,Modified booth's Algorithm.	
UNIT-III	**CONTROL DESIGN**
Hardwired control, micro programmed control, multiplier control unit, CPU control unit.Pipeline control, instruction pipelines, pipeline performance, superscalar processing, Nano programming.	

UNIT-IV	MEMORY ORGANIZATION
Random access memories, serial access memories, RAM interfaces, magnetic surface recording, optical memories, multilevel memories, cache & virtual memory, memory allocation, associative memory.	
UNIT-V	**SYSTEM ORGANIZATION**
Communication methods, buses, bus control, bus interfacing, bus arbitration, IO and system control, IO interface circuits, handshaking, DMA and interrupts, vectored interrupts, PCI interrupts, pipeline interrupts, IOP organization, operation systems, multiprocessors, fault tolerance, RISC and CISCprocessors, superscalar and vector processor.	
Text Books:	
1. John P. Hayes, "Computer architecture and Organization", Tata McGraw-Hill, 3rd Edition,1998. 2. V Carl Hamacher, Zvonko G. Varanesic, Safat G. Zaky, "Computer Organization", Tata McGraw- Hill Inc, 5th Edition,1996.	
Reference Books:	
1. Morris Mano, "Computer System Architecture", Prentice-Hall of India,2000. 2. Paraami, "Computer Architecture", BEH R002, OxfordPress. 3. P Pal Chaudhuri,"Computer organization and design", Prentice Hall, 2nd Edition,2007.	

XVI. COURSEPLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-3	Computing and computers,Evolutionof Computers, VLSIera	CLO 1	T1:1.1-1.3
4-6	System design, register level, processor level, CPU organization	CLO 2	T1:2.1-2.3
7	data representation, fixed-point numbers, floating point numbers	CLO 3	T1:3.1-3.2
8-10	Instruction formats, instruction types, addressing modes.	CLO 4	T1:3.3
11-14	Fixed Point Arithmetic, Addition, Subtraction, Multiplication and Division, Combinational and Sequential ALUs, Carry look ahead adder	CLO 5	T1:4.1-4.3
15-20	Robertson algorithm, booth's algorithm, non-restoring division algorithm, Floating Point Arithmetic.	CLO 6	T1:4.12
21-25	Coprocessor, Pipeline Processing, Pipeline Design, Modified booth's Algorithm.	CLO 7 CLO 8	T1:4.3
26-27	Hardwired control, micro-programmed control, multipliercontrolunit.	CLO 9	T1:5.1-5.3
28-29	CPUcontrolunit.Pipeline control, instruction pipelines.	CLO 10, CLO 11	T1:5.1-5.3
30-34	Pipeline performance, Superscalar Processing, Nano-Programming.	CLO 12	T1:5.3
35-36	Random access memories, serial access memories, RAM interfaces, magnetic surfacerecording	CLO 13	T1:6.1
37-41	Optical memories, multilevel memories, cache & virtual memory, memory allocation, associative memory	CLO 14, CLO 15	T1:6.2
42-44	Communication methods, buses, bus control, bus interfacing, bus arbitration, IO and system control, IO interface Circuits.	CLO 16, CLO 17	T1:7.1-7.2
45-49	Handshaking, DMA and interrupts, vectored interrupts, PCI interrupts, and pipeline interrupts, IOP organization, operationsystems.	CLO 18	T1:7.2

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
50-55	Multi processors, fault tolerance, RISC and CISC processors, superscalar and vector processor.	CLO 19, CLO 20	T1:7.3

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSIONREQUIREMENTS:

S No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	To improve standards and analyze theconcepts.	Seminars	PO 1	PSO 1
2	Encourage students to solve real time applications and prepare towardscompetitive security mechanisms.	NPTEL	PO 2	PSO 1

Prepared by:
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