



# INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

## COMPUTER SCIENCE AND ENGINEERING

### COURSE DESCRIPTOR

<b>Course Title</b>	<b>MICROPROCESSORS AND INTERFACING</b>				
<b>Course Code</b>	AEC021				
<b>Programme</b>	B.Tech				
<b>Semester</b>	V	CSE			
<b>Course Type</b>	Core				
<b>Regulation</b>	IARE - R16				
<b>Course Structure</b>	<b>Theory</b>			<b>Practical</b>	
	<b>Lectures</b>	<b>Tutorials</b>	<b>Credits</b>	<b>Laboratory</b>	<b>Credits</b>
	3	1	4	3	2
<b>Chief Coordinator</b>	Mr.V R Seshagiri Rao, Assistant Professor				
<b>Course Faculty</b>	Dr.P S L Murthy, Professor Mr. Mohd.Khadir, Assistant Professor Ms. K Sravani, Assistant Professor Mrs. Lakshmi Prasanna, Assistant Professor				

#### I. COURSE OVERVIEW:

The course will make them learn the basic theory of microprocessor and their applications in detail. Subsequently the course covers important concepts like how to write an assembly language programming. They will learn to write an assembly language programming for interfacing various I/O modules. They will learn to design different advance architectures to design a new communication interfaces.

#### II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	ACS004	III	Computer Organization and Architecture	4
UG	AEC020	III	Digital Logic Design	4

#### III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microprocessors and Interfacing	70 Marks	30 Marks	100

#### IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✓	Chalk & Talk	✓	Quiz	✓	Assignments	✗	MOOCs
✓	LCD / PPT	✓	Seminars	✗	Mini Project	✓	Videos
✗	Open Ended Experiments						

#### V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

**Semester End Examination (SEE):** The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with “either” or “choice” will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

#### **Continuous Internal Assessment (CIA):**

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
	CIE Exam	Quiz/AAT	
CIA Marks	25	05	30

#### **Continuous Internal Examination (CIE):**

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

### Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

### VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	<b>Engineering knowledge:</b> Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Quiz
PO 2	<b>Problem analysis:</b> Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	2	Assignments
PO 4	<b>Conduct investigations of complex problems:</b> Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Seminars

**3 = High; 2 = Medium; 1 = Low**

### VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	<b>Professional Skills:</b> The ability to understand , analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based system of varying complexity.	2	Seminars and Assignments
PSO 2	<b>Problem-Solving Skills:</b> The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	1	Quiz and Assignments
PSO 3	<b>Successful Career and Entrepreneurship:</b> The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

**3 = High; 2 = Medium; 1 = Low**

### VIII. COURSE OBJECTIVES :

The course should enable the students to:	
I	Understand the basic concepts of microprocessors and develop the architectures of 8085 and 8086.
II	Analyze and develop assembly language programming for 8086 microprocessor.
III	Develop various interfacing modules by using assembly language programming.
IV	Understand and know the basic concepts of advance micro processor architectures like 80386 and 80486.

### IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Describe the concepts of Architectures of 8085 and 8086 with its functionalities and understand the addressing modes and instructions sets of 8086.	CLO 1	Differentiate between 8085 and 8086 microprocessors architectures and its functionalities. Distinguish between RISC and CISC architecture based microprocessors
		CLO 2	Describe the internal Architecture of 8086 microprocessor and explain its functionalities.
		CLO 3	Describe in detail about functions of general purpose register and 8086 flag register with its functions.
		CLO 4	Explain various addressing modes and instruction set present in 8086 microprocessors and Describe in detail about the concept of interrupt, types of interrupts 8086 microprocessor.
		CLO 5	Understand and apply the fundamentals and procedures and assembler directives of assembly level programming of microprocessors.
		CLO 6	Develop low level languages like ALP in 8086 Microprocessor systems for real time applications
CO 2	Describe Minimum mode and maximum mode of operation of 8086 and Analyze the Assembly language programs involving in various arithmetic and logical operations.	CLO 7	Describe Minimum mode and maximum mode of operation and timing diagram of 8086 Microprocessor
		CLO 8	Explain various Assembly language programs involving logical, branch and call instructions.
		CLO 9	Evaluation of arithmetic expressions, string manipulation, sorting using various Assembly language programs.
CO 3	Discuss the importance of 8251, 8255 and explain interfacing of	CLO 10	Identify the importance of Various modes of 8255 operation and interfacing to 8086.

COs	Course Outcome	CLOs	Course Learning Outcome
	I/O device with different modules.	CLO 11	Discuss the interfacing diagram of I/O devices with keyboard, stepper motor, 7-segment display, LCD and digital to analog and analog to digital converter.
		CLO 12	Explain in detail about the importance of interrupt and interrupt sub routines in 8086 microprocessor
		CLO 13	Explain the advance architectures of PIC and also the importance of interfacing a interrupt controller in PIC.
CO 4	Analyze the various synchronous and asynchronous serial data transfer schemes in 8086	CLO 14	Analyze and understand various synchronous and asynchronous serial data transfer schemes in 8086.
		CLO 15	Develop and design the interfacing circuit diagram of 8251USART with 8086 processor.
		CLO 16	Understand the high- speed serial communications standards, USB.
CO 5	Understand the advanced 16 and 32 bit microprocessors architectures and its features.	CLO 17	Understand basic architecture of 16 bit and 32 bit Microprocessors with the help of GDT, LDT and multitasking and addressing modes.
		CLO 18	Flag register 80386: Architecture, register organization, memory access in protected mode
		CLO 19	Analyze the various advanced microprocessors internal architectures for 80X86 by paging and technical features.

#### X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC021.01	CLO 1	Differentiate between 8085 and 8086 Microprocessors architectures and its functionalities. Distinguish between RISC and CISC architecture based microprocessors	PO 1	3
AEC021.02	CLO 2	Describe the internal Architecture of 8086 microprocessor and explain its functionalities.	PO 1	3
AEC021.03	CLO 3	Describe in detail about functions of general purpose register and 8086 flag register with its functions.	PO 1	3
AEC021.04	CLO 4	Explain various addressing modes and instruction set present in 8086	PO 1	3

<b>CLO Code</b>	<b>CLO's</b>	<b>At the end of the course, the student will have the ability to:</b>	<b>PO's Mapped</b>	<b>Strength of Mapping</b>
		microprocessors and Describe in detail about the concept of interrupt, types of interrupts 8086 microprocessor.		
AEC021.05	CLO 5	Understand and apply the fundamentals and procedures and assembler directives of assembly level programming of microprocessors.	PO 2	2
AEC021.06	CLO 6	Develop low level languages like ALP in 8086 microprocessor systems for real time applications	PO 2	2
AEC021.07	CLO 7	Describe Minimum mode and maximum mode of operation and timing diagram of 8086 microprocessor	PO 1	3
AEC021.08	CLO 8	Explain various Assembly language programs involving logical, branch and call instructions.	PO 2	2
AEC021.09	CLO 9	Evaluation of arithmetic expressions, string manipulation, sorting using various Assembly language programs.	PO 2	2
AEC021.10	CLO 10	Identify the importance of Various modes of 8255 operation and interfacing to 8086.	PO 1	3
AEC021.11	CLO 11	Discuss the interfacing diagram of I/O devices with keyboard, stepper motor, 7-segment display, LCD and digital to analog and analog to digital converter.	PO 4, PO2	2
AEC021.12	CLO 12	Explain in detail about the importance of interrupt and interrupt sub routines in 8086 microprocessor	PO 1	3
AEC021.13	CLO 13	Explain the advance architectures of PIC and also the importance of interfacing a interrupt controller in PIC.	PO 1	3
AEC021.14	CLO 14	Analyze and understand various synchronous and asynchronous serial data transfer schemes in 8086.	PO 4, PO1	2
AEC021.15	CLO 15	Develop and design the interfacing circuit diagram of 8251USART with 8086 processor.	PO 1, PO2	3
AEC021.16	CLO 16	Understand the high- speed serial communications standards, USB.	PO 1	3
AEC021.17	CLO 17	Understand basic architecture of 16 bit and 32 bit microprocessors with the help of GDT, LDT and multitasking and addressing modes.	PO 4	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC021.18	CLO 18	Flag register 80386: Architecture, register organization, memory access in protected mode.	PO 1	3
AEC021.19	CLO 19	Analyze the various advanced microprocessors internal architectures for 80X86 by paging and Technical features.	PO 1	3

**3= High; 2 = Medium; 1 = Low**

**XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Outcomes (COs)	Program Outcomes (POs)			Program Specific Outcomes (PSOs)	
	PO 1	PO 2	PO 4	PSO1	PSO2
CO 1	3	2		2	1
CO 2		2		2	1
CO 3	3		2	2	
CO 4	3		2		1
CO 5	3		2		1

**3 = High; 2 = Medium; 1 = Low**

**XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:**

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3														
CLO 2	3												2		
CLO 3	3												2		
CLO 4	3												2		
CLO 5		2													
CLO 6		2													
CLO 7	3												2		
CLO 8		2													
CLO 9		2											2		
CLO 10	3												2		

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 11		2		2											
CLO 12	3												2		
CLO 13	3												2		
CLO 14	3			2										1	
CLO 15	3	2												1	
CLO 16	3														
CLO 17				2										1	
CLO 18	3														
CLO 19	3													1	

3 = High; 2 = Medium; 1 = Low

### XIII. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO1,PO2, PO4,PSO1, PSO2	SEE Exams	PO1, PO2, PO4,PSO1, PSO2	Assignments	PO1,PO2, PO4,PSO1, PSO2	Seminars	PO1, PO2, PO4,PSO1, PSO2
Laboratory Practices	PO1, PO2, PO4,PSO1, PSO2	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO1, PO2, PO4,PSO1						

### XIV. ASSESSMENT METHODOLOGIES - INDIRECT

✓	Early Semester Feedback	✓	End Semester OBE Feedback
✗	Assessment of Mini Projects by Experts		

### XV. SYLLABUS

<b>Unit-I</b>	<b>OVERVIEW OF 8086 MICROPROCESSOR</b>
Introduction to 8085 microprocessor. RISC and CISC processors, architecture of 8086 microprocessor, special functions of general purpose register, 8086 flag register and function of 8086 flags, addressing modes of 8086, instruction set of 8086, assembler directives, simple programs, procedures, and macros.	
<b>Unit-II</b>	<b>PIN DIAGRAM OF 8086 AND ASSEMBLY LANGUAGE PROGRAMMING</b>
Minimum mode and maximum mode of operation, timing diagram, Assembly language programs: Assembly language programs involving logical, branch and call instructions, sorting, evaluation of arithmetic expressions, string manipulation.	



<b>Unit-III</b>	<b>8255 PROGRAMMABLE PERIPHERAL INTERFACE (PPI)</b>
<p>Various modes of 8255 operation and interfacing to 8086; Interfacing keyboard, displays, 8279 Stepper motor and actuators, digital to analog and analog to digital converter interfacing. Interrupt structure of 8086: Interrupt structure of 8086, Vector interrupt table, interrupt service routines;</p> <p>Introduction to DOS and BIOS interrupts, 8259 PIC architecture and interfacing cascading of interrupt controller and its importance.</p>	
<b>Unit-IV</b>	<b>SERIAL DATA TRANSFER SCHEMES</b>
<p>Asynchronous and synchronous data transfer schemes, 8251 USART architecture and interfacing; TTL to RS 232C and RS232C to TTL conversion; Sample program of serial data transfer; Introduction to high speed serial communications standards, USB.</p>	
<b>Unit-V</b>	<b>ADVANCED MICROPROCESSORS</b>
<p>80286 microprocessor: Architecture, registers (Real/Protected mode), privilege levels, descriptor cache, memory access in GDT and LDT, multitasking, addressing modes; Flag register 80386: Architecture, register organization, memory access in protected mode, paging; 80486: Only the technical features.</p>	
<b>Text Books:</b>	
<ol style="list-style-type: none"> <li>1. D. V. Hall, "Microprocessors and Interfacing", Tata McGraw-Hill Education, 3<sup>rd</sup> Edition 2013.</li> <li>2. A.K Ray, K. M. Bhurchandani, "Advanced Microprocessors and Peripherals" Tata McGraw-Hill Education, 2<sup>nd</sup> Edition, 2006.</li> <li>3. Savaliya M. T, "8086 Programming and Advance Processor Architecture", Wiley India Pvt., 1<sup>st</sup> Edition, 2012.</li> </ol>	
<b>Reference Books:</b>	
<ol style="list-style-type: none"> <li>1. N. Senthil Kumar, M. Saravanan, S. Jeevanathan, S. K. Shah, "Microprocessors and Interfacing", Oxford University, 1<sup>st</sup> Edition, 2012.</li> <li>2. Lyla B. Das, "The x86 Microprocessors", Pearson India, 2<sup>nd</sup> Edition, 2014.</li> </ol>	

## XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1-2	Introduction to 8085 microprocessor. RISC and CISC processors, architecture of 8086 microprocessor	CLO 1	T1:Chapter 1.1,1.2
3-5	Architecture of 8086 microprocessor, special functions of general purpose register.	CLO 2	T2: Chapter 1.2 R1: Chapter 1.2
6-7	8086 flag register and function of 8086 flags.	CLO 3	T2: Chapter 1.1 R1: Chapter 1.2
8-9	Instruction set of the processor which is used for programming, addressing modes of 8086, and instruction set of 8086.	CLO 4	T2: Chapter 2.2, T1:Chapter 5.1
10-11	Assembler directives, simple programs, procedures, and macros.	CLO 5	T1: Chapter 5.6, 5.7,5.8 T2: Chapter 2.4
12-13	Develop low level languages like ALP in 8086 Microprocessor systems	CLO6	T1: Chapter 5.6, 5.7,5.8 T2:Chapter 3.4

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
14-15	Minimum mode and maximum mode of operation, timing diagram, memory interfacing to 8086 (Static RAM and EPROM).	CLO 7	T2:Chapter1.8, 1.9 R1:Chapter 3.4
16-17	Assembly language programs: Assembly language programs involving logical, branch and call instructions.	CLO 8	T1: Chapter 5.7,5.6 T2:Chapter 3.4
18-20	Sorting, evaluation of arithmetic expressions, string manipulation, Develop low level languages like ALP in 8086 Microprocessor systems.	CLO 9	T1: Chapter 5.7,5.6 R2:Chapter 3.4,4.7
21-22	Various modes of 8255 operation and interfacing to 8086;	CLO 10	T1: Chapter 1.1,1.2.2 T2: Chapter 5.5
23-26	Interfacing keyboard, displays, 8279 Stepper motor and actuators, digital to analog and analog to digital converter interfacing	CLO11	T2: Chapter 6.3,5.6,5.7,5.8 R1:Chapter 4.4
27-29	Interrupt structure of 8086: Interrupt structure of 8086, Vector interrupt table, interrupt service routines;	CLO 12	T2:Chapter 4.3 R1:Chapter 6.4
30-32	Introduction to DOS and BIOS interrupts 8259 PIC architecture and interfacing cascading of interrupt controller and its importance.	CLO13	T2:Chapter 6.2,6.4 R2: Chapter 5.2
33-34	Asynchronous and synchronous data transfer schemes,	CLO 14	R2:Chapter 5.1
35-38	8251 USART architecture and interfacing; TTL to RS 232C and RS232C to TTL conversion; Sample program of serial data transfer;	CLO15	R2:Chapter 5.1 T2:Chapter 6.4
39-41	Introduction to high-speed serial communications standards, USB.	CLO 16	R2:Chapter 5.1
42-46	80286 microprocessor: Architecture, registers (Real/Protected mode), privilege levels, descriptor cache, memory access in GDT and LDT, multitasking, addressing modes.	CLO 17	R2:Chapter 5.2 T2: Chapter 9.2, 9.3,9.9,9.10
47-50	Flag register 80386: Architecture, register organization, memory access in protected mode, paging;	CLO 18	R2:Chapter 5.3 T2:Chapter 10.2,10.3,10.9
51-53	Memory access in protected mode, paging; 80486: Only the technical features.	CLO 19	R2:Chapter 5.3 T2:Chapter10.13

## **XVII. GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSION REQUIREMENTS:**

S No	Description	Proposed Actions	Relevance with POs	Relevance with PSOs
1	ALP for Microprocessors like 8086 and 80x86	Seminars / NPTEL	PO 1, PO 2, PO 4	PSO 1,PSO2
2	Interfacing IO devices to various types of Microprocessors	Seminars / Guest Lectures / NPTEL	PO 2, PO 4	PSO 1
3	Programming of all microprocessors by using ALP	Laboratory Practices	PO 1, PO 2, PO 4	PSO 2

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