Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC020

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER

Four Year B.Tech III Semester End Examinations, November - 2018

Regulations: R16

DIGITAL LOGIC DESIGN

(Common to CSC/IT)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT - I

1	a)	Explain error detecting and correcting codes with the help of parity bits by using hamming code for the following binary code $(1100110)_2$.	[7M]
	b)	Convert the given Boolean expression $(1001_2 + 36_{10} - C84_{16}) - 14_{10}$ and give the result in base 8 by using 2's complement method?	[7M]
2	a)	Explain about binary weighted and non-weighted codes in detail and how the binary code is converted to gray code?	[7M]
	b)	Simplify the following Boolean expression *A'C'D'+AC'+BCD+A'CD'+A'+AB'C'*, Given *AB' + AB = C* and show that *AC' + A'C = B*.	[7M]

UNIT - II

3	a)	A combinational circuit has 4 inputs(A,B,C,D) and three outputs (X,Y,Z) where XYZ represents a binary number whose value equals the number of 1's at the input *i.* State the min term expansion for the X, Y, Z. ii. State the max term expansion for the Y and Z.	[7M]
	b)	Summarize the following Boolean function by using don't care conditions? *F(w, x, y, z) = Σ(1, 3, 7, 11, 15) + d(w, x, y, z) = Σ(0. 2, 5)*	[7M]
4	a)	Design BCD to Excess-3 code converter and realize the Excess-3 code conversion by using basic and universal logic gates?	[7M]
	b)	Simplify the Boolean expression of F (A, B, C, D) = AB'C'D + ACD + A'CD'+A'BCD' neither using K-map and implement the obtained expression by using NOR gates?	[7M]

UNIT – III

5	a)	Design and implement a full adder circuit with the help of 3:8 decoder and explain it with the help of truth tables and logic circuits?	[7M]

b) Solve the following Boolean expression by using suitable decoder circuit and implement the final output by using OR gates: [7M]

i. F1 (A,B,C,D)=Σ(2,4,7,9)

ii. F2(A,B,C,D)=Σ(10,13,14,15)

6 a) Explain the design procedure and design analysis for any code converter with the help of an example? [7M]

b) Convert F(A,B,C,D) = (0,1,3,5,9,11,13,15) into the minterm form and Implement the function with a multiplexer and other necessary logic gates. Show the implementation table using *A* as input and *B,C,D* as the selectors. [7M]

UNIT – IV

7 a) Design and implement a 4-bit binary counter by using D flip flop, which can count only odd numbers? [7M]

b) Write short notes on shift register? Explain how the serial transfer occurs in 4-bit shift registers and specify some practical applications of 4-bit shift register? [7M]

8 a) Construct and verify the state transition table for the SR and D flip-flops and explain the operations of the following flip-flops by using transition table? [7M]

b) Design and implement a 3 bit ring counter and also differentiate ring counters from twisted ring counters? [7M]

UNIT – V

9 a) Design a BCD to Excess-3 code converter and implement the Converted Excess-3 code by using Suitable programmable logic devices? [7M]

b) Sketch the programmable logic array table for the given Boolean functions given by minimizing the number of product terms for each Boolean function? [7M]

A(x,y,z)=Σ(0,1,3,5)

B(x,y,z)=Σ(2,6)

C(x,y,z)=Σ(1,2,3,5,7)

D(x,y,z)=Σ(0,1,6)

10 a) Define Random access memory and distinguish between SRAM and DRAM with the help of a block diagram? [7M]

b) Solve the following multiple Boolean function using 3*4*2 PLA and PLD? [7M]

i. F1(a2, a1, a0)=∑m(0,1,3,5),

ii. F2(a2, a1, a0)=∑m(3,5,7)

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I. COURSE OBJECTIVES

The course should enable the students to:

S.No	Description
I	Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algrbra.
II	Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip-flops and latches
III	Understand about synchronous and asynchronous sequential logic circuits.
IV	Impart the basic understanding of memory organization, ROM, RAM, PLA and PAL.

II. COURSE OUTCOMES

Students who complete the course will have demonstrated the ability to do the following.

S.No	Description	Blooms Taxonomy Level
AEC020.01	Understand the basic concept of number systems, binary addition and subtraction for digital systems.	Remember
AEC020.02	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.	Understand
AEC020.03	Discuss about digital logic gates, error detecting and correcting codes for digital systems.	Understand
AEC020.04	Describe the importance of SOP and POS canonical forms with examples.	Remember
AEC020.05	Describe minimization techniques and other optimization techniques for Boolean formulas in general and digital circuits.	Understand
AEC020.06	Evaluate Boolean algebra expressions by minimizing algorithms like sop and pos using Boolean Postulates and theorems.	Understand
AEC020.07	Solve various Boolean algebraic functions using Karnaugh map and Tabulation Method.	Remember
AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.	Understand
AEC020.09	Analyze the design procedures of Sequential logic circuits with the help of registers	Remember
AEC020.10	Discuss the concept of flip flops and latches by using sequential logic circuits.	Understand
AEC020.11	Differentiate combinational logic circuits with sequential logic circuits along with examples.	Remember
AEC020.12	Understand the concept of memory organization, read only memory and random access memory.	Remember
AEC020.13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	Remember

AEC020.14	Explain the concept of memory hierarchy in terms of capacity and access time.	Understand
AEC020.15	Explain about Synchronous and Asynchronous Sequential Circuits: Reduction of state tables for Mealy and Moore machines	Understand
AEC020.16	Discuss about various memory concepts with respect to temporary and permanent memory organizations.	Remember

III. MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNING OUTCOMES:

SEE Question No.		Course Outcomes		Blooms Taxonomy Level
1	a	AEC020.03	Discuss about digital logic gates, error detecting and correcting codes for digital systems.	Remember
	b	AEC020.02	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.	Understand
2	a	AEC020.01	Understand the basic concept of number systems, binary addition and subtraction for digital systems.	Understand
	b	AEC020.04	Identify the importance of SOP and POS canonical forms with examples.	Remember
3	a	AEC020.05	Describe minimization techniques and other optimization techniques for Boolean formulas in general and digital circuits.	Understand
	b	AEC020.07	Solve various Boolean algebraic functions using Karnaugh map and Tabulation Method.	Remember
4	a	AEC020.03	Discuss about digital logic gates, error detecting and correcting codes for digital systems.	Understand
	b	AEC020.06	Evaluate Boolean algebra expressions by minimizing algorithms like sop and pos using Boolean Postulates and theorems.	Remember
5	a	AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.	Understand
	b	AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.	Understand
6	a	AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.	Understand
	b	AEC020.08	Understand bi-stable elements and different type's combinational logic circuits.	Understand
7	a	AEC020.10	Discuss the concept of flip flops and latches by using sequential logic circuits.	Understand
	b	AEC020.09	Analyze the design procedures of Sequential logic circuits with the help of registers	Remember
8	a	AEC020.10	Discuss the concept of flip flops and latches by using sequential logic circuits.	Understand
	b	AEC020.10	Discuss the concept of flip flops and latches by using sequential logic circuits.	Understand
9	a	AEC020.13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	Understand
	b	AEC020.13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	Understand
10	a	AEC020.12	Understand the concept of memory organization, read only memory and random access memory.	Remember
	b	AEC020.13	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	Understand

Signature of Course Coordinator **HOD,CSE**