INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**MICROPROCESSORS AND MICROCONTROLLERS**				
Course Code	AEC013				
Programme	B.Tech				
Semester	VI	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	**Mr. V R Seshagiri Rao, Associate Professor**				
Course Faculty	**Mr. D KhalandarBasha, Associate Professor** **Mr. B Naresh, Assistant Professor**				

I. COURSE OVERVIEW:

The course focuses on the architecture, programming of microprocessors, microcontrollers and also interfacing. The course includes architecture, addressing modes, instruction set of 8086 and 8051, minimum and maximum mode operation of 8086, Assembly language programming fundamentals, interfacing of static Ram, EPROM, DMA Controller, keyboard, display, 8279, stepper motor, A/D and D/A converter, 8259 interrupt controller, data transmission, 8251 USART, modes of timer operation of 8051, programming of real time control by using basic microcontroller. The knowledge derived from this course is useful in development of various projects and models in engineering and scientific professions.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Digital System Design	4
UG	AEC010	V	Computer Organization	3

III. MARKSDISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microprocessors and Microcontrollers	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✔	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz/ Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall

have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Quiz
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences	3	Assignments
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Mini Project
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Seminars / Mini Project

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Seminars and Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Quiz and Assignments

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Imbibe sound knowledge about architecture, instruction set and concepts of 8086 and 8051.
II	Demonstrate the ability to develop programmes for different applications using assembly language of 8086 and 8051.
III	Impart knowledge of different types of external peripherals like 8255, 8259,8279,8251,8257.
IV	Be proficient in Memory and I/O interfacing with 8086 and 8051.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Acquire knowledge about architecture and functional features of microprocessors particularly 8086.	CLO 1	Understand the internal Architecture and different modes of operation of popular 8086 microprocessors.
		CLO 2	Basic understanding of 8085 and 8086 microprocessors architectures and its functionalities.
		CLO 3	An ability to distinguish between RISC and CISC based microprocessors.
		CLO 4	Understand the importance of addressing modes and the instruction set of the processor which is used for programming.
CO 2	Obtain an insight in to the instruction set of 8086 and write programs in assembly level language.	CLO 5	Understand and apply the fundamentals of assembly level programming of microprocessors.
		CLO 6	Design and develop 8086 Microprocessor based systems for real time applications using low level language like ALP.
		CLO 7	Understand the memory organization and interrupts of processors helps in various system designing aspects.
		CLO 8	Identify the significance of interrupts and interrupt service routines with appropriate illustrations.
CO 3	Interface different types of external peripherals like 8255,8259,8279, 8251 &8257 with 8086.	CLO 9	Ability to interface the external peripherals and I/O devices and program the 8086 microprocessor using 8255.
		CLO 10	Identify the significance of serial communication in8086 with required baud rate.
		CLO 11	An ability to distinguish between the serial and parallel data transfer schemes.
		CLO 12	Develop the interfacing of universal synchronous asynchronous receiver transmitter 8251 with 8086 processor
		CLO 13	Ability to interface the programmable interrupt controller 8259 with 8086.

COs	Course Outcome	CLOs	Course Learning Outcome
CO 4	Imbibe knowledge about hardware details of 8051 microcontrollers and develop assembly language programs for data transfer, arithmetic, logical and branch instructions.	CLO 14	Understand the internal Architecture and different modes of operation of popular 8051 microcontrollers.
		CLO 15	Basic understanding of 8051 microcontrollers functionalities.
		CLO 16	Understand the different addressing modes used in assembly language programming of microcontrollers.
		CLO 17	Write programs for arithmetic and logical computations using 8051 instruction sets.
CO 5	Design simple systems using timers, interrupts, memories ADC and DACs etc. using 8051.	CLO 18	Construct, and develop of required delay circuits using timers of 8051 in the laboratory.
		CLO 19	Interfacing of physical elements using Digital and analog converters with microcontrollers.
		CLO 20	Assess and interface required memory to microcontrollers with appropriate memory mapping.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC013.01	CLO 1	Understand the internal Architecture and different modes of operation of popular 8086 microprocessors.	PO1	3
AEC013.02	CLO 2	Basic understanding of 8085 and 8086 microprocessors architectures and its functionalities.	PO2	2
AEC013.03	CLO 3	An ability to distinguish between RISC and CISC based microprocessors.	PO1	2
AEC013.04	CLO 4	Understand the importance of addressing modes and the instruction set of the processor which is used for programming.	PO2	1
AEC013.05	CLO 5	Understand and apply the fundamentals of assembly level programming of microprocessors.	PO2	3
AEC013.06	CLO 6	Design and develop 8086 Microprocessor based systems for real time applications using low level language like ALP.	PO3	3
AEC013.07	CLO 7	Understand the memory organization and interrupts of processors helps in various system designingaspects.	PO3	2
AEC013.08	CLO 8	Identify the significance of interrupts and interrupt service routines with appropriate illustrations.	PO1	2
AEC013.09	CLO 9	Ability to interface the external peripherals and I/O devices and program the 8086 microprocessor using 8255.	PO3	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC013.10	CLO 10	Identify the significance of serial communication in8086 with required baud rate.	PO4	2
AEC013.11	CLO 11	An ability to distinguish between the serial and parallel data transfer schemes.	PO1, PO2	2
AEC013.12	CLO 12	Develop the interfacing of universal synchronous asynchronous receiver transmitter 8251 with 8086 processor	PO3	3
AEC013.13	CLO 13	Ability to interface the programmable interrupt controller 8259 with 8086.	PO3	2
AEC013.14	CLO 14	Understand the internal Architecture and different modes of operation of popular 8051 microcontrollers.	PO3	2
AEC013.15	CLO 15	Basic understanding of 8051 microcontrollers functionalities.	PO1	3
AEC013.16	CLO 16	Understand the different addressing modes used in assembly language programming of microcontrollers.	PO1	2
AEC013.17	CLO 17	Write programs for arithmetic and logical computations using 8051 instruction sets.	PO4	2
AEC013.18	CLO 18	Construct, and develop of required delay circuits using timers of 8051 in the laboratory.	PO3	3
AEC013.19	CLO 19	Interfacing of physical elements using Digital and analog converters with microcontrollers.	PO3	3
AEC013.20	CLO 20	Assess and interface required memory to microcontrollers with appropriate memory mapping.	PO3	3

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes	Program Outcomes and Program Specific Outcomes					
	PO1	PO2	PO 3	PO4	PSO 1	PSO 2
CO 1	3	2				
CO 2	2	3	3		2	
CO 3	2	2	3	2		2
CO 4	3		2	2	2	
CO 5			3			2

XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3														
CLO 2		2											1	3	
CLO 3	2												2		
CLO 4		2												3	
CLO 5		3												3	
CLO 6			3											2	
CLO 7			3											2	
CLO 8	2												3		
CLO 9			3										1		
CLO 10				2										3	
CLO 11	2	2											2		
CLO 12			3											2	
CLO 13			2											2	
CLO 14			2										2		
CLO 15	3												3		
CLO 16	2												2		
CLO 17				2										2	
CLO 18			3											1	
CLO 19			3											1	
CLO 20			3										2		

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES–DIRECT

CIE Exams	PO 1	SEE Exams	PO 1	Assignments	-	Seminars	PO 2
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 4						

XIV. ASSESSMENT METHODOLOGIES-INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

UNIT – I	**8086 MICROPROCESSORS**	**CLASSES: 11**
Register organization of 8086, Architecture, signal description of 8086, physical memory organization, general bus operation, I/O addressing capability, special purpose activities, Minimum mode, maximum mode of 8086 system and timings, machine language instruction formats, addressing mode of 8086, instruction set of 8086,assembler directives and operators.		
UNIT – II	**PROGRAMMING WITH 8086 MICROPROCESSOR**	**CLASSES: 09**
Machine level programs, programming with an assembler, Assembly language programs, introduction to stack, stack structure of 8086/8088, interrupts and interrupt service routines. Interrupt cycle of 8086, non-mask able interrupt and mask able interrupts, interrupt programming.		
UNIT – III	**INTERFACING WITH 8086/88**	**CLASSES: 10**
Semiconductor memory interfacing, dynamic RAM interfacing, interfacing i/o ports, PIO 8255 modes of operation of 8255,interfacing to D/A and A/D converters, stepper motor interfacing, control of high power devices using 8255. Programmable interrupt controller 8259A, the keyboard /display controller8279, programmable communication interface 8251 USART, DMA Controller 8257.		
UNIT – IV	**8051 MICROCONTROLLER**	**CLASSES: 09**
8051 Microcontroller – Internal architecture and pin configuration, 8051 addressing modes, instruction set, Bit addressable features. I/O Port structures, assembly language programming using data transfer, arithmetic, logical and branch instructions.		
UNIT – V	**SYSTEM DESIGNUSING MICROCONTROLLER**	**CLASSES: 09**
8051 Timers/Counters, Serial data communication and its programming, 8051 interrupts, Interrupt vector table, Interrupt programming. Real world interfacing of 8051 with external memory, expansion of I/O ports, LCD, ADC, DAC, stepper motor interfacing.		
Text Books:		
1. D. V. Hall, "Microprocessors and Interfacing", Tata McGraw-Hill Education, 3rd Edition 2013. 2. A.K Ray, K. M. Bhurchandani, "Advanced Microprocessors and Peripherals" Tata McGraw-Hill Education, 2nd Edition, 2006. 3. Savaliya M. T, "8086 Programming and Advance Processor Architecture", Wiley India Pvt., 1st Edition, 2012.		
Reference Books:		
1. N. Senthil Kumar, M. Saravanan, S. Jeevanathan, S. K. Shah, "Microprocessors and Interfacing", Oxford University, 1st Edition, 2012. 2. Lyla B. Das, "The x86 Microprocessors", Pearson India, 2nd Edition, 2014.		
Web References:		
1.http://www.daenotes.com/electronics/digital-electronics/Intel-80858bitmicroprocessor#axzz2I9yUSe7I 2.https://www.smartzworld.com/notes/microprocessors-and-microcontrollers-mpmc/ 3. http://www.iare.ac.in		

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Understand the Register organization of 8086	CLO 1	T3:2.1
2	Understand the architecture 8086	CLO 1	T3:2.1
3	Explain the ssignal description of 8086	CLO 1	T3:1.2
4	Understand the physical memory organization, general bus operation,	CLO 1	T3:1.1,1.2.2
5	Ability of I/O addressing capability, special purpose activities	CLO 2	T3:1.4
6	Distinguish betweenminimum mode, maximum mode of 8086 system and timings,	CLO 2	T3:1.3,1.8, 1.9
7	Compare between the minimum mode, maximum mode of 8086 system and timings	CLO 1	T3:2.1
8	Learn the machine language instruction formats, addressing mode of 8086	CLO 2	T3:2.2
9	Differentiate different addressing modes of 8086	CLO 3	T3:2.3
10	Explain the instruction set of 8086	CLO 4	T3:2.4 T1:5.1-5.20
11	Explain the instruction set of 8086	CLO 4	T3:2.4 T1:5.1-5.20
12	Explain the instruction set of 8086	CLO 4	T3:2.4 T1:5.1-5.20
13	Grasp the instruction set of 8086	CLO 4	T3:5.4
14	Learn the instruction set of 8086	CLO 4	T3:5.5
15	Grasp the instruction set of 8086	CLO 4	T1:9.19 T3: 5.8
16	Contrast between the assembler directives and operators.	CLO 5	T3:5.7,5.6
17	Contrast between the assembler directives and operators.	CLO 5	T3:5.1
18	Know how to write the machine level programs, programming with an assembler, Assembly language programs	CLO 5	T1-8.1,T1-8.7
19	Know how to write the machine level programs, programming with an assembler, Assembly language programs	CLO 5	T3:6.4.3 T1:14.9,14 .48
20	Describe the stack, stack structure of 8086/8088, interrupts and interrupt service routines	CLO 8	T3:6.4,6.4 4
21	Describe the interrupt cycle of 8086, non-mask able interrupt and mask able interrupts, interrupt programming	CLO 8	R3:2.1
22	Understand semiconductor memory interfacing, dynamic RAM interfacing	CLO 9	R3:2.1
23	Understand semiconductor memory interfacing, dynamic RAM interfacing	CLO 9	T3:1.2

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
24	Explain how to Interface I/O ports	CLO 9	T3:1.1
25	Contrast different modes of operation of 8255	CLO 9	T3:1.4
26	Contrast different modes of operation of 8255	CLO 9	T3:1.3,1.8, 1.9
27	Explain how to interface to D/A and A/D converters	CLO 9	T3:2.1
28	Explain how to interface stepper motor, control of high power devices using 8255	CLO 9	T3:2.2
29	Understand the programmable interrupt controller 8259A	CLO 13	T3:2.3
30	Describe the programmable interrupt controller 8259A	CLO 13	T3:2.4T1:5 .1-5.20
31	Interface the keyboard /display controller8279	CLO 9	T3:2.4, T1:5 .1-5.20
32	Elaborate the details of programmable communication interface 8251	CLO 10	T3:2.4T1:5 .1-5.20
33	Elaborate the details of programmable communication interface 8251	CLO 11	T3:2.4T1:5 .1-5.20
34	Interfacing 8251 with 8086	CLO 12	T3:2.4T1:5 .1-5.20
35	Functional block explanation the DMA Controller 8257	CLO 9	T3:5.4
36	Functional block explanation the DMA Controller 8257	CLO 9	T3:5.5
37	Understand the internal architecture of 8051	CLO 14	T2:3.1
38	Understand the pin configuration of 8051	CLO 14	T2:3.1
39	Distinguish between the 8051 addressing modes	CLO 15	T2:3.2
40	Elaborate the instruction set, Bit addressable features of 8051	CLO 15	T2:3.3
41	Elaborate the instruction set, Bit addressable features of 8051	CLO 15	T2:5.1
42	Appreciate the I/O Port structure of 8051	CLO14	T2:6.1,6.6,7.1 7.6, 8.1 -8.3
43	Implementation of assembly language programs for 8051MC.	CLO16	T2:6.1 to 6.6,7.1 to 7.6,
44	Implementation of assembly language programs for 8051MC.	CLO 16 CLO 17	T2:3.6
45	Understand the Timers/Counters in 8051	CLO 18	T2:3.4
46	Explanation of the serial data communication and its programming	CLO 18	T2:3.6,3.4 R5:24.5- 24.7
47	Describe the interrupts, Interrupt vector table, Interrupt programming	CLO 19	T2:3.6,3.4 R5:24.5- 24.7
48	Design real world interfacing of 8051 with external memory, expansion of I/O ports	CLO 20	T2:3.1
49	Design real world interfacing of 8051 with LCD, ADC, DAC	CLO 19	T2:3.2

Lecture No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
50	Ability to interface stepper motor	CLO 19	T2:3.3

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	ALP for Microprocessors like 8086 and 80x86	Seminars / NPTEL	PO 1, PO 2, PO 4	PSO 1
2	Interfacing IO devices to various types of Microprocessors	Seminars / Guest Lectures / NPTEL	PO 1, PO 2, PO 4	PSO 1
3	Programming of all microprocessors by using ALP	Laboratory Practices	PO 1, PO 2, PO 4	PSO 2

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