# ELECTRONIC DEVICES AND CIRCUITS (ECE)

## II B.Tech III semester

## (IARE - R18)

## (2019 - 2020)

Institute of Aeronautical Engineering

# SYLLABUS

Module-1:DIODE APPLICATIONS

Module-2:BIPOLAR JUNCTION TRANSISTOR (BJT)

Module-3:TRANSISTOR BIASING AND STABILIZATION

Module-4: JUNCTION FIELD EFFECT TRANSISTOR

Module-5:FET AMPLIFIERS

# DIODE AND APPLICATIONS

# MATERIALS

Based on the electrical properties of the materials like conductivity, materials are divided into three types.

i) Conductors
ii) Semiconductors
iii) Insulators

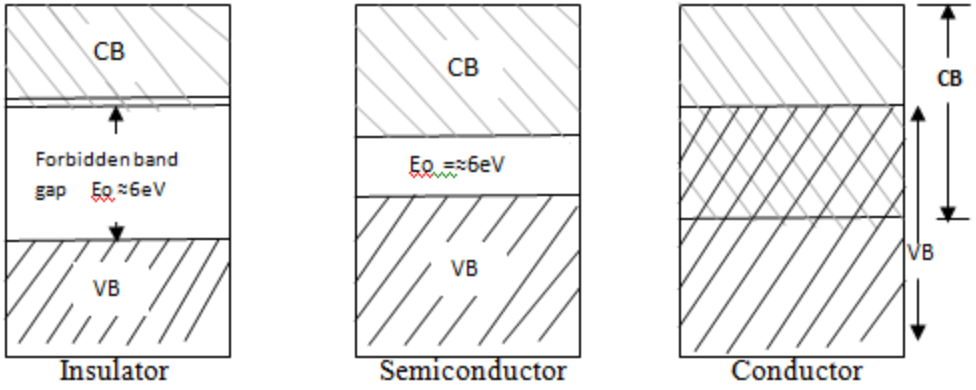



**Fig.1: Energy band diagrams for insulator, semiconductor and conductor**

# CONDUCTORS

- A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity.
- Ex: Copper, Aluminum, Silver, and Gold. The resistivity of a conductor is in the order of $10^{-4}$ and $10^{-6}$ Ω-cm.

# INSULATORS

- An insulator is a material that offers a very low level of conductivity when voltage is applied.
- Ex: Paper, Mica, glass, quartz.
- Typical resistivity level of an insulator is of the order of $10^{10}$ to $10^{12}$ Ω-cm.

# SEMICONDUCTORS

- A semiconductor is a material that has its conductivity lies between the insulator and conductor.
- The resistivity level is in the range of 10 and $10^4$ Ω-cm.
- Ex: Si & Ge

# TYPES OF SEMICONDUCTORS

## i) Intrinsic Semiconductor:

- A pure form of semiconductor is called as intrinsic semiconductor.
- Conduction in intrinsic sc is either due to thermal excitation or crystal defects.
- Ex: Si and Ge

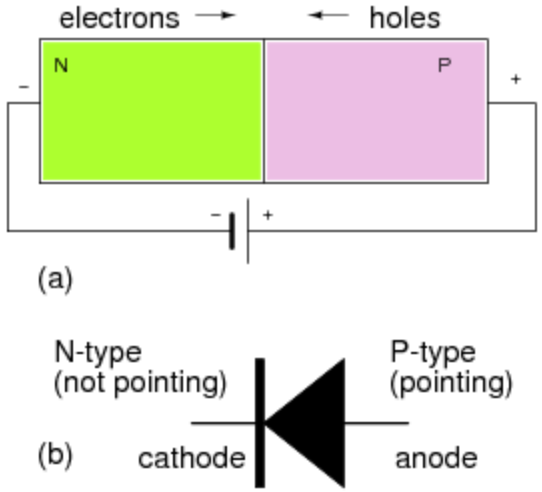
# TYPES OF SEMICONDUCTORS

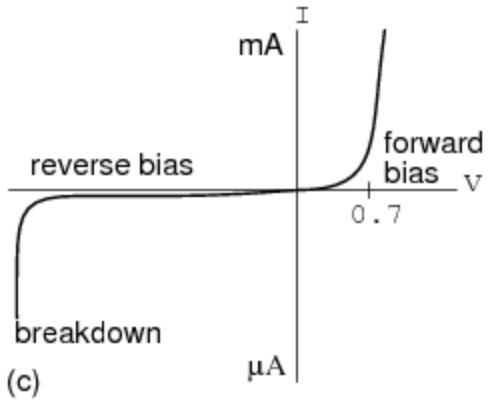
## ii) Extrinsic Semiconductor:

- The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amount of impurity to the intrinsic semiconductor.
- By adding impurities it becomes impure or extrinsic semiconductor.
- ***The process of adding impurities to the intrinsic semiconductor is called as doping.***

# WHAT DO YOU MEAN BY DIODE?

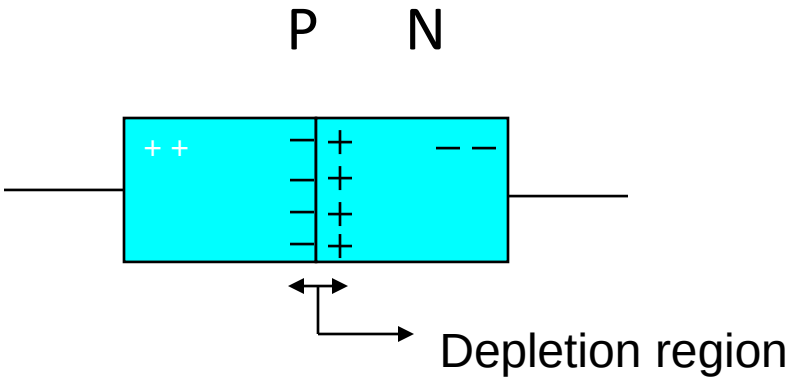
A PN junction is a device formed by joining p-type with n-type semiconductors and separated by a thin junction is called PN Junction diode or junction diode.



# THEORY OF P-N JUNCTION

When a p-type semiconductor material is suitably joined to n-type semiconductor the contact surface is called a p-n junction.



# THEORY OF PN JUNCTION DIODE

- Suppose the two pieces are suitably treated to form PN junction, then there is a tendency for the free electrons from n-type to diffuse over to the p-side and holes from p-type to the n-side . This process is called **diffusion.**

- The holes from the p-side diffuse to the n-side and the electrons from the n-side diffuse to the p-side. This gives rise to a diffusion current across the junction.

# THEORY OF PN JUNCTION DIODE

- As the free electrons move across the junction from n-type to p-type, +ve donor ions are uncovered. Hence a +ve charge is built on the n-side of the junction.
- At the same time, the free electrons cross the junction and uncover the –ve acceptor ions by filling in the holes. Therefore a net –ve charge is established on p-side of the junction.

# THEORY OF PN JUNCTION DIODE

- When a sufficient number of donor and acceptor ions is uncovered further diffusion is prevented.
- Thus a barrier is set up against further movement of charge carriers. This is called potential barrier or junction barrier Vo. The potential barrier is of the order of 0.1 to 0.3V.
- **Note:** outside this barrier on each side of the junction, the material is still neutral. Only inside the barrier, there is a +ve charge on n-side and –ve charge on p-side. This region is called depletion layer.

# THEORY OF PN JUNCTION DIODE

- The depletion layer contains no free and mobile charge carriers but only fixed and immobile ions.
- Its width depends upon the doping level..

- Heavily doped……..thin depletion layer
- lightly doped……..thick depletion layer

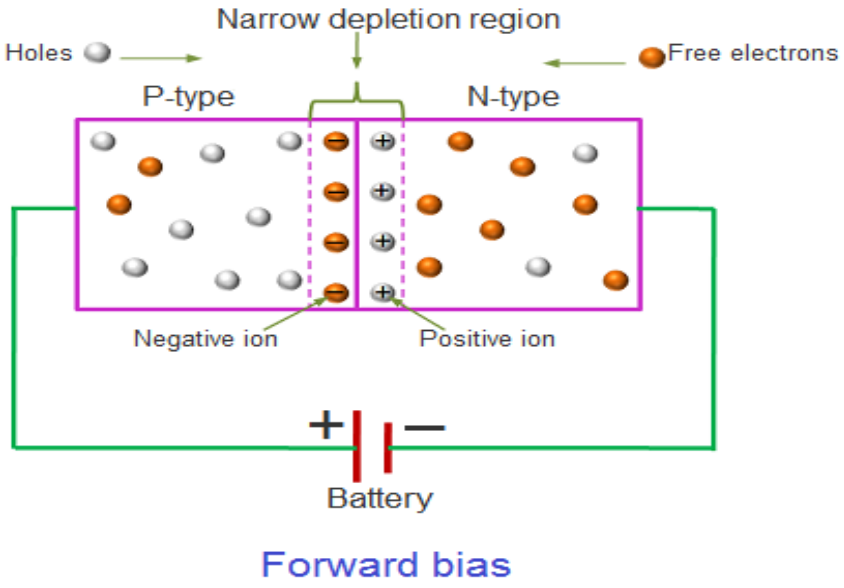
# THEORY OF PN JUNCTION DIODE

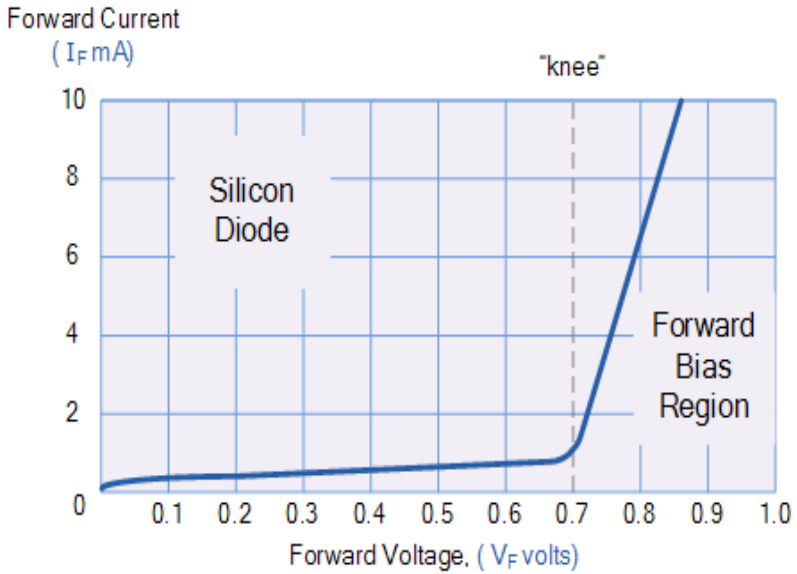
PN junction can basically work in two modes, (***A battery is connected to the diode*** ).

**Forward bias mode :** positive terminal connected to p-region and negative terminal connected to n region.

***Reverse bias mode:*** negative terminal connected to p-region and positive terminal connected to n region

# PN JUNCTION –FORWARD BIAS



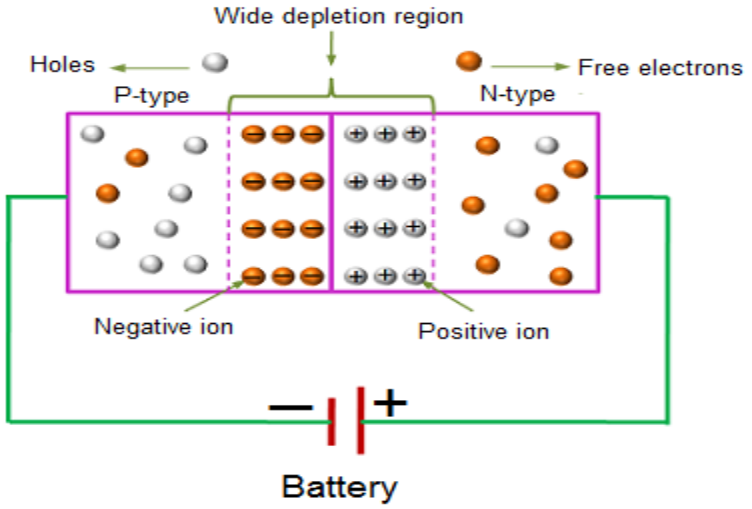




- It forces the majority charge carriers to move across the junction ….decreasing the width of the depletion layer.

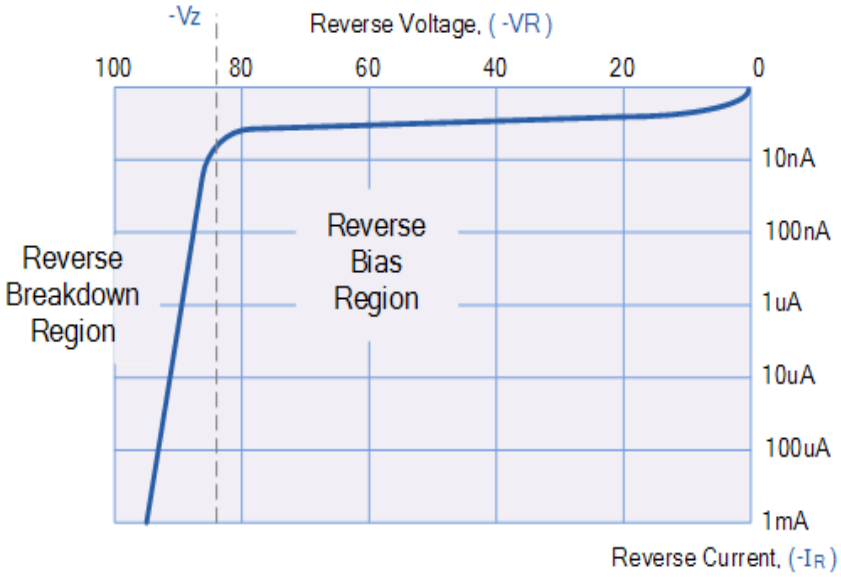
# PN junction –Forward Bias

- When a diode is connected in a FB condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material.
- If this external voltage becomes greater than the value of the potential barrier, i.e. 0.7V for Si and 0.3V for Ge, the potential barriers opposition will be overcome and current will start.
- The application of a FB voltage on the junction diode results in the depletion layer becoming very thin which represents a low impedance path through the junction thereby allowing high currents to flow.

# PN JUNCTION –REVERSE BIAS




Reverse bias




- The free electrons and free holes are attracted towards the battery, hence depletion layer width increases.

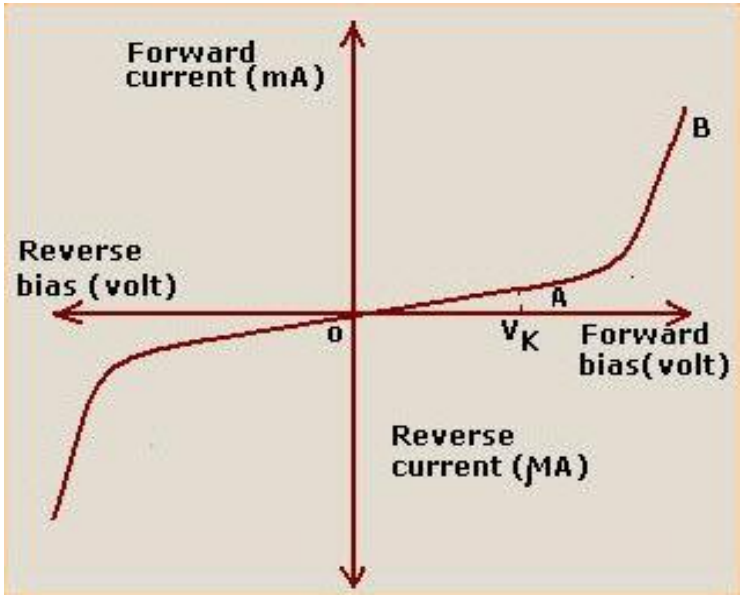
# PN JUNCTION –REVERSE BIAS

- When a diode is connected in a Reverse bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.

- The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

- The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

# V-I CHARACTERISTICS OF PN JUNCTION DIODE




V-I characteristics of PN junction diode

# V-I CHARACTERISTICS OF PN JUNCTION DIODE

- When the diode is F.B., the current increases exponentially with voltage except for a small range close to the origin.
- When the diode is R.B., the reverse current is constant and independent of the applied reverse bias.
- Turn-on or cut-in (threshold) voltage Vγ: for a F.B. diode it is the voltage when the current increases appreciably from zero.
- It is roughly equal to the barrier p.d.:
- For Ge, Vγ ~ 0.2 – 0.4 V (at room temp.) For Si, Vγ ~ 0.6 – 0.8 V (at room temp.)

# STATIC OR DC RESISTANCE

The resistance of a diode at a particular operating point is called the dc or static resistance diode.

The resistance of the diode at the operating point can be found simply by finding the corresponding levels of $V_D$ and $I_D$.

It can be determined using equation

$$R_D = V_D / I_D$$

The lower current through a diode the higher the dc resistance level

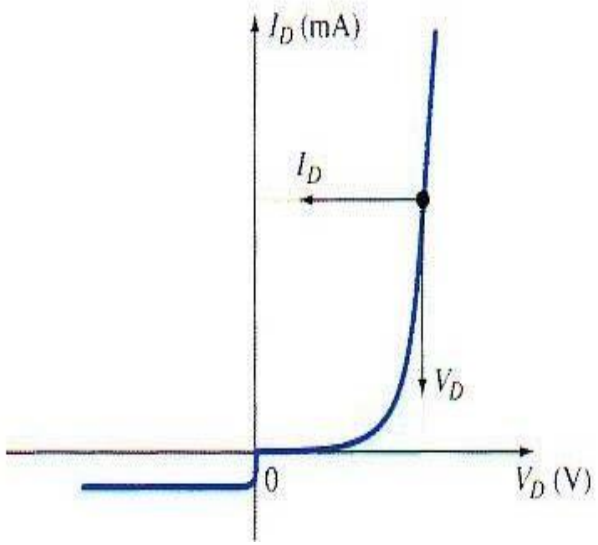



Fig: Static resistance curve

# DYNAMIC OR AC RESISTANCE

Static resistance is using dc input. If the input is sinusoidal the scenario will be change.

The ac resistance is determined by a straight line drawn between the two intersections of the maximum and minimum values of input voltage.

Thus the specific changes in current and voltage is obtained. It can be determined using equation $r_d = \Delta V_D / \Delta I_D$

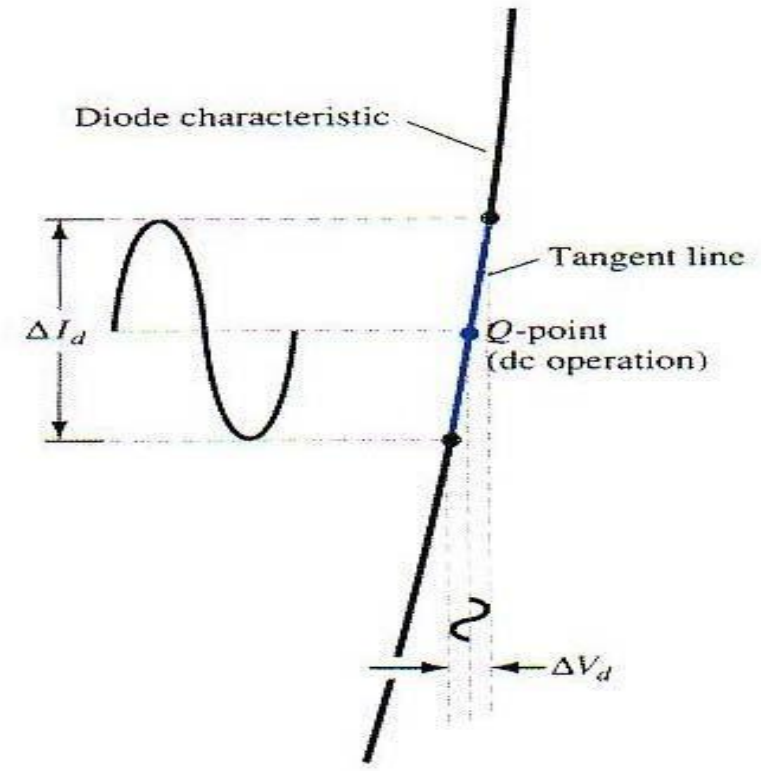
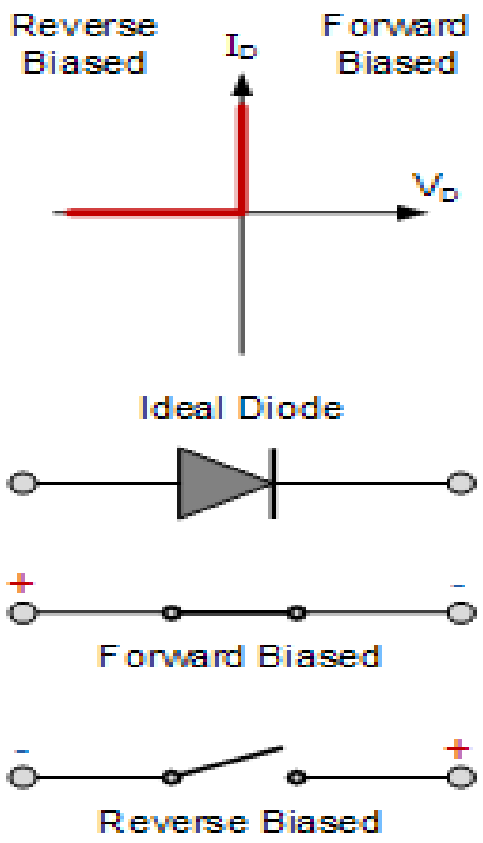
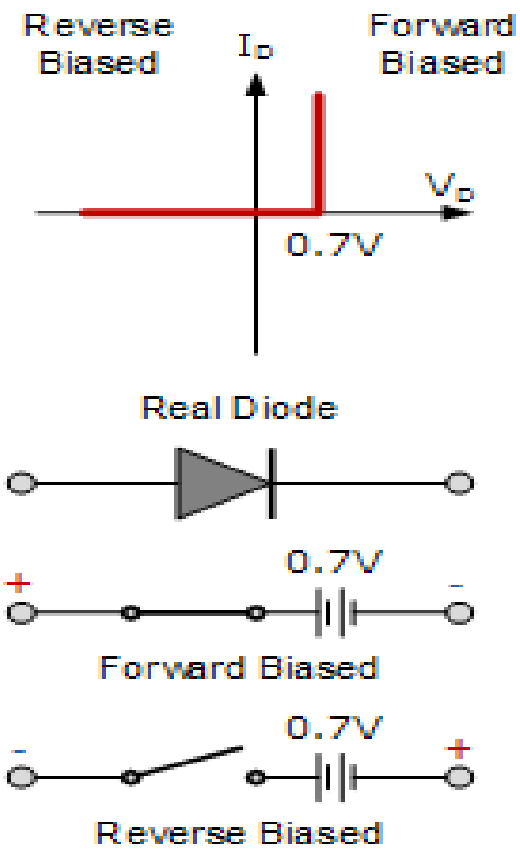



Fig: Dynamic resistance curve

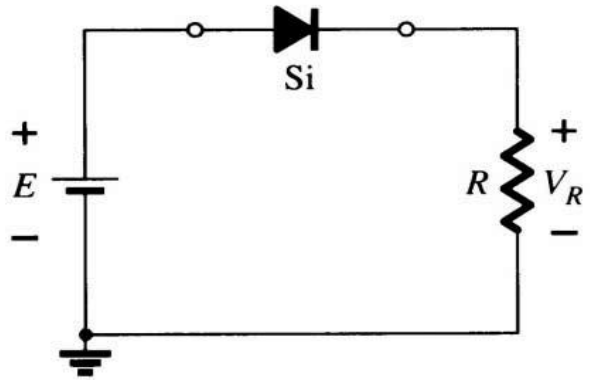
# PN JUNCTION DIODE IDEAL AND REAL CHARACTERIS

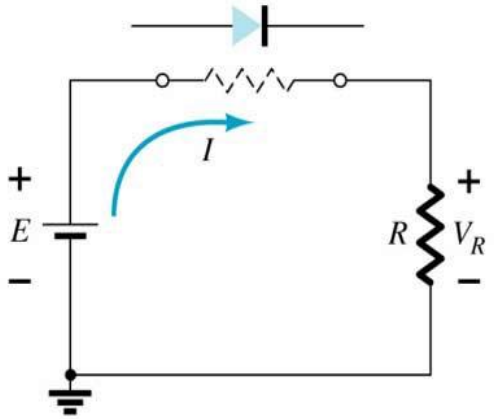


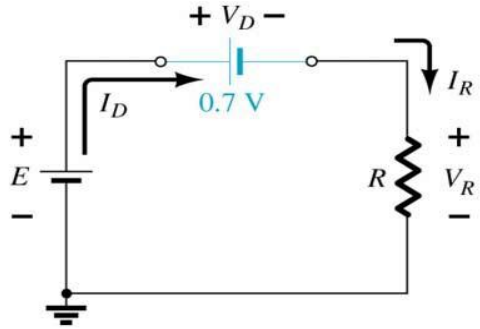



# DIODE EQUIVALENT CIRCUIT

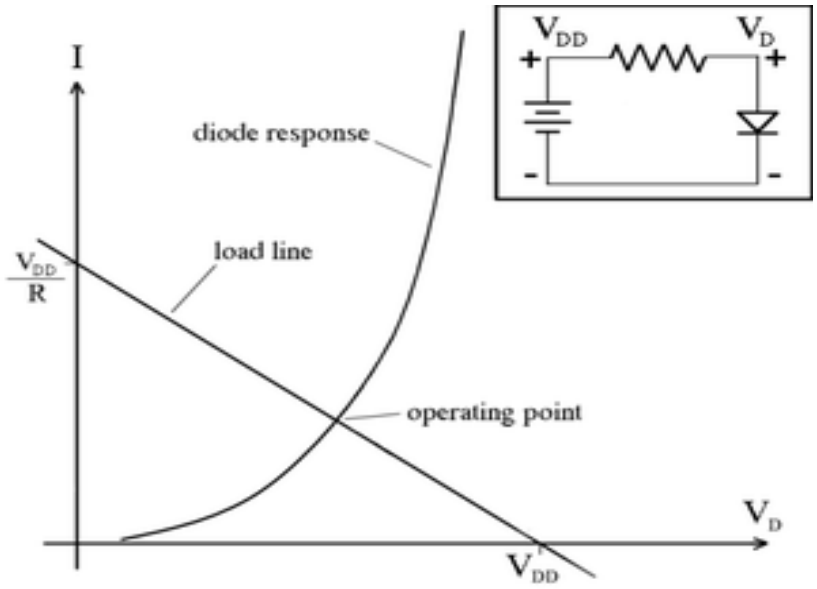
When a diode is F.B, we can use the approximate model for the on state



# PN DIODE- LOAD LINE ANALYSIS




**A load line** is a line drawn on the characteristic curve, a graph of the current vs. voltage in a nonlinear device like a diode.

- The curve shows the diode response (I vs $V_D$) while the straight line shows the behavior of the linear part of the circuit:

$$I=(V_{DD}-V_D)/R.$$

- The point of intersection gives the actual current and voltage.

# JUNCTION CAPACITANCE

In a p-n junction diode, two types of capacitance take place. They are,

- Transition capacitance ($C_T$)
- Diffusion capacitance ($C_D$)

## Transition Capacitance $C_T$

The amount of capacitance changed with increase in voltage is called transition capacitance. The transition capacitance is also known as depletion region capacitance, junction capacitance or barrier capacitance.

# TRANSITION CAPACITANCE $C_T$

The change of capacitance at the depletion region can be defined as the change in electric charge per change in voltage.

$$C_T = dQ / dV$$

Where,

$C_T$= Transition capacitance

dQ = Change in electric charge

dV = Change in voltage

The transition capacitance can be mathematically written as, $C_T = \varepsilon A / W$

Where,

ε = Permittivity of the semiconductor

A = Area of plates or p-type and n-type regions

W = Width of the depletion region

# DIFFUSION CAPACITANCE ($C_D$)

Diffusion capacitance occurs in a forward biased p-n junction diode. Diffusion capacitance is also sometimes referred as storage capacitance. It is denoted as $C_D$.

The formula for diffusion capacitance is

$$C_D = dQ / dV$$

Where,

$C_D$ = Diffusion capacitance

dQ = Change in number of minority carriers stored outside the depletion region

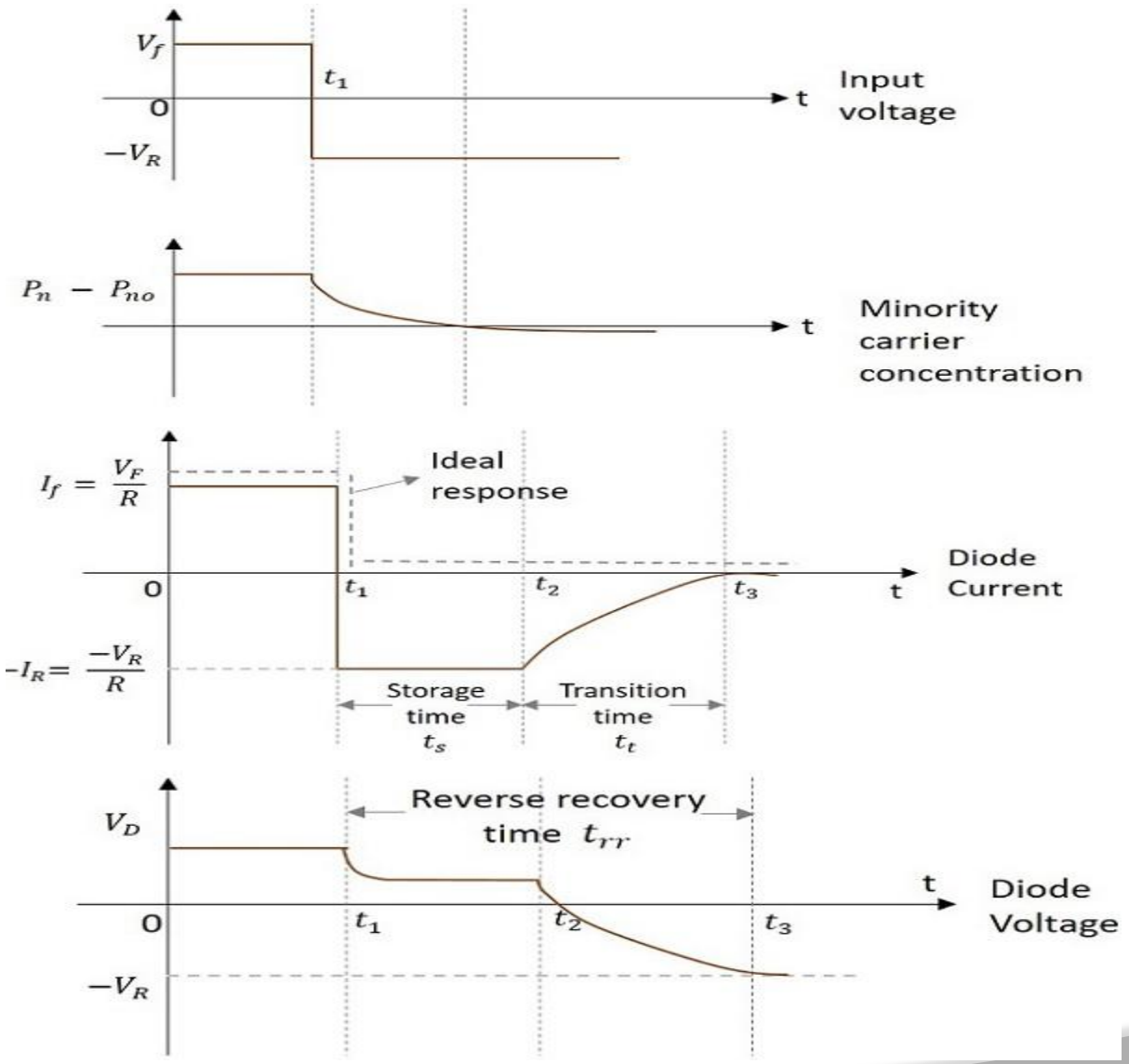
dV = Change in voltage applied across diode

# DIODE APPLICATIONS

common applications of diodes are

- Switches
- Rectifiers
- Clipper Circuits
- Clamping Circuits
- Reverse Current Protection Circuits
- In Logic Gates
- Voltage Multipliers

# PN DIODE SWITCHING TIMES




- The majority carriers in P-type (holes) = $P_{po}$
- The majority carriers in N-type (electrons) = $N_{no}$
- The minority carriers in P-type (electrons) = $N_{po}$
- The majority carriers in N-type (holes) = $P_{no}$

# PN DIODE SWITCHING TIMES

**Storage time** − The time period for which the diode remains in the conduction state even in the reverse biased state, is called as **Storage time**.

**Transition time** − The time elapsed in returning back to the state of non-conduction, i.e. steady state reverse bias, is called **Transition time**.

**Reverse recovery time** − The time required for the diode to change from forward bias to reverse bias is called as **Reverse recovery time**.

**Forward recovery time** − The time required for the diode to change from reverse bias to forward bias is called as **Forward recovery time**.

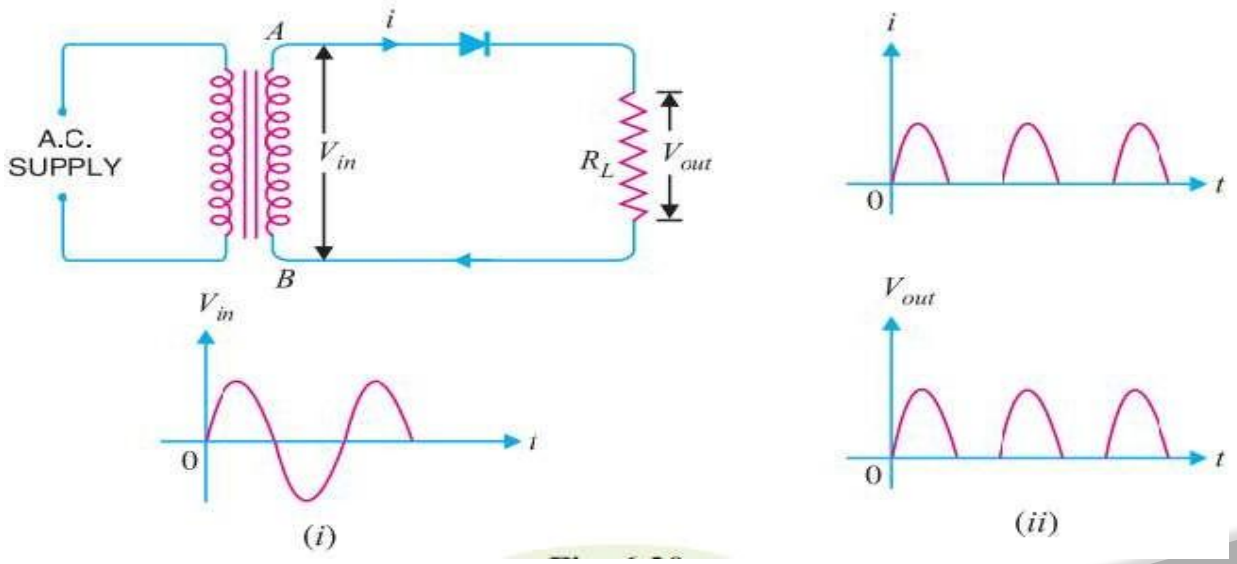
# RECTIFIER

- A circuit that converts ac voltage of main supply into pulsating dc voltage using one or more PN junction diodes is called rectifier.

- Half Wave Rectifier
- Full Wave Rectifier
- Bridge Rectifier

# HALF WAVE RECTIFIER

- The process of removing one-half the input signal to establish a dc level is called *half-wave rectification.*
- In Half wave rectification, the rectifier conducts current during positive half cycle of input ac signal only.
- Negative half cycle is suppressed.



# HALF WAVE RECTIFIER

- During the positive half cycle, the diode is under forward bias condition and it conducts current to RL (Load resistance). A voltage is developed across the load, which is same as the input AC signal of the positive half cycle.

- During the negative half cycle, the diode is under reverse bias condition and there is no current flow through the diode. Only the AC input voltage appears across the load and it is the net result which is possible during the positive half cycle. The output voltage pulsates the DC voltage.

## Average DC load Current ($I_{DC}$):

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \quad \text{for } 0 \le \omega t \le \pi$$

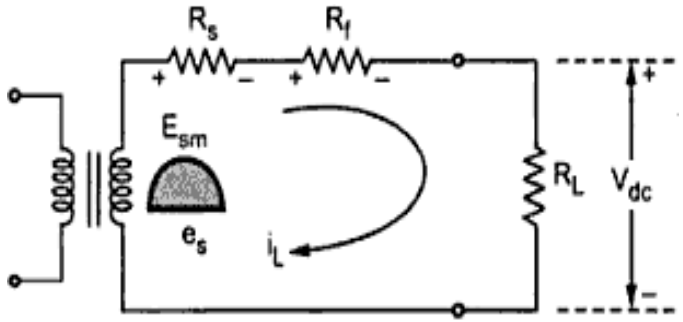
$$i_L = 0 \quad \text{for } \pi \le \omega t \le 2\pi$$

$I_m$ = peak value of load current

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

$$I_{DC} = \frac{I_m}{\pi} = \text{average value}$$

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$




(a) Equivalent circuit

where $R_s$ = resistance of secondary winding of transformer. If $R_s$ is not given it should be neglected while calculating $I_m$.

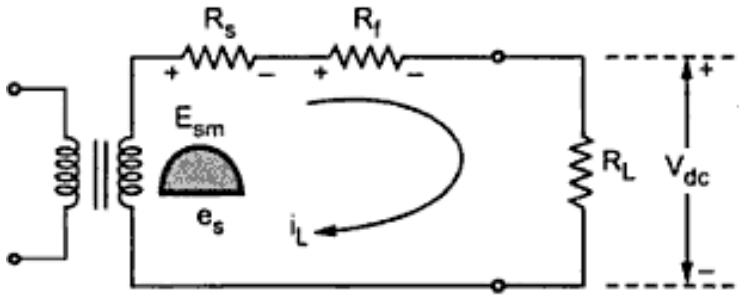
# HALF WAVE RECTIFIER

## Average DC voltage (Edc):

$$E_{DC} = I_{DC} R_L$$

$$E_{DC} = \frac{I_m}{\pi} R_L$$

$$= \frac{E_{sm}}{(R_f + R_L + R_s)\pi} R_L$$




(a) Equivalent circuit

But as $R_f$ and $R_s$ are small compared to $R_L$ , $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

$$E_{DC} \approx \frac{E_{sm}}{\pi}$$

# HALF WAVE RECTIFIER

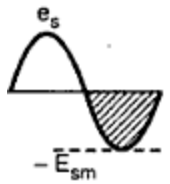
## RMS Load Current (Irms):

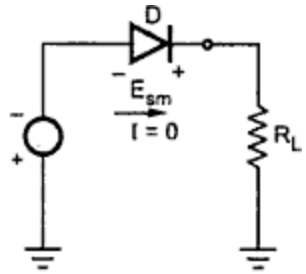
$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin \omega t)^2 \, d(\omega t)} \quad \rightarrow \quad \boxed{I_{RMS} = \frac{I_m}{2}}$$

## RMS Load Voltage (Erms):

$$E_{L\,(RMS)} = \frac{E_{sm}}{2}$$

## Peak Inverse Voltage (PIV):




PIV = Em

Diode must be selected based on the PIV rating and the circuit specification.

# HALF WAVE RECTIFIER

## DC Power Delivered to the load:

$$P_{DC} = E_{DC} I_{DC} = I_{DC}^2 R_L$$

$$\text{D.C. Power output} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi}\right]^2 R_L = \frac{I_m^2}{\pi^2} R_L$$

$$P_{DC} = \frac{I_m^2}{\pi^2} R_L$$

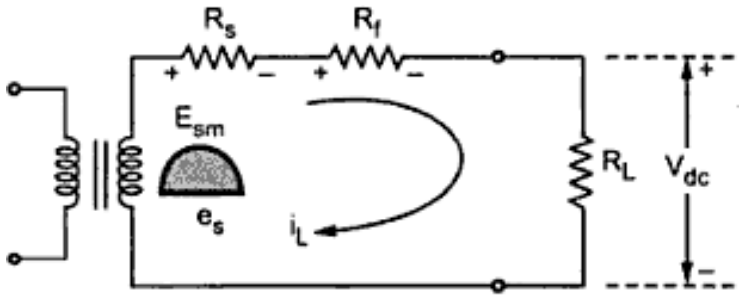
## AC input power from transformer secondary:

The power input taken from the secondary of transformer is the power supplied to three resistances namely load resistance $R_L$ , the diode resistance $R_f$ and winding resistance $R_s$. The a.c. power is given by,

$$P_{AC} = I_{RMS}^2[R_L + R_f + R_s]$$

$I_{RMS} = \frac{I_m}{2}$ for half wave,

$$P_{AC} = \frac{I_m^2}{4}[R_L + R_f + R_s]$$




(a) Equivalent circuit

## Rectifier Efficiency (η):

$$\eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\eta = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4}[R_f + R_L + R_s]} = \frac{(4/\pi^2)R_L}{(R_f + R_L + R_s)}$$

; η= 40.6 %

Under best conditions (no diode loss) only 40.6% of the ac input power is converted into dc power.

The rest remains as the ac power in the load

# HALF WAVE RECTIFIER

## Ripple Factor:

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S. value of a.c. component of output}}{\text{Average or d.c. component of output}}$$

(or)

$$\text{Ripple factor} = \frac{I_{ac}}{I_{DC}}$$

$$\gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

$$\gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2}\right)}{\left(\frac{I_m}{\pi}\right)}\right]^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674} \quad \rightarrow \quad \gamma = 1.211$$

This indicates that the ripple content in the output are 1.211 times the dc component.

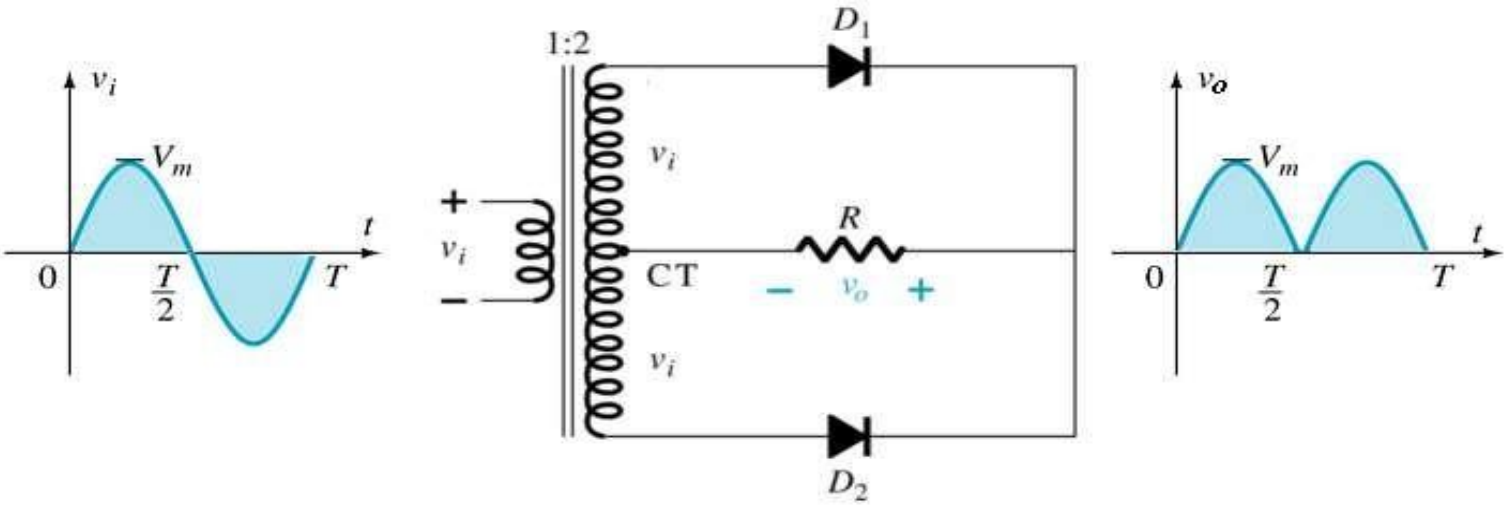
i.e. 121.1 % of dc component.

# HALF WAVE RECTIFIER

**Disadvantage of HWR:**

- The ripple factor of half wave rectifier is 1.21, which is quite high.
- The output contains lot of ripples
- The maximum theoretical efficiency is 40%.
- The practical value will be quite less than this.
- This indicates that HWR is quite inefficient.

# FULL-WAVE RECTIFIER



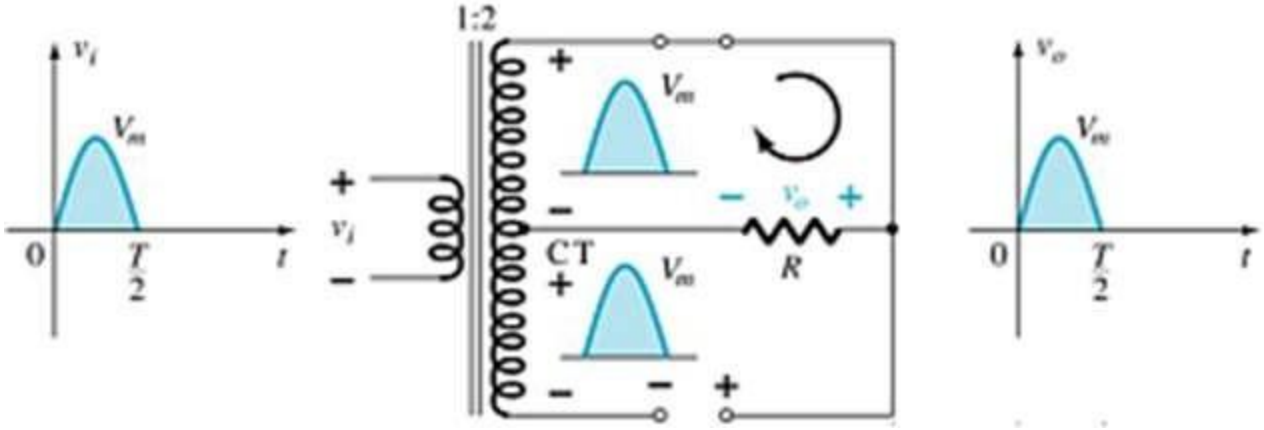

- The full wave rectifier circuit consists of two *power diodes* connected to a single load resistance ($R_L$) with each diode taking it in turn to supply current to the load.
- When point A of the transformer is positive with respect to point C, diode $D_1$ conducts in the forward direction as indicated by the arrows.

# FULL-WAVE RECTIFIER

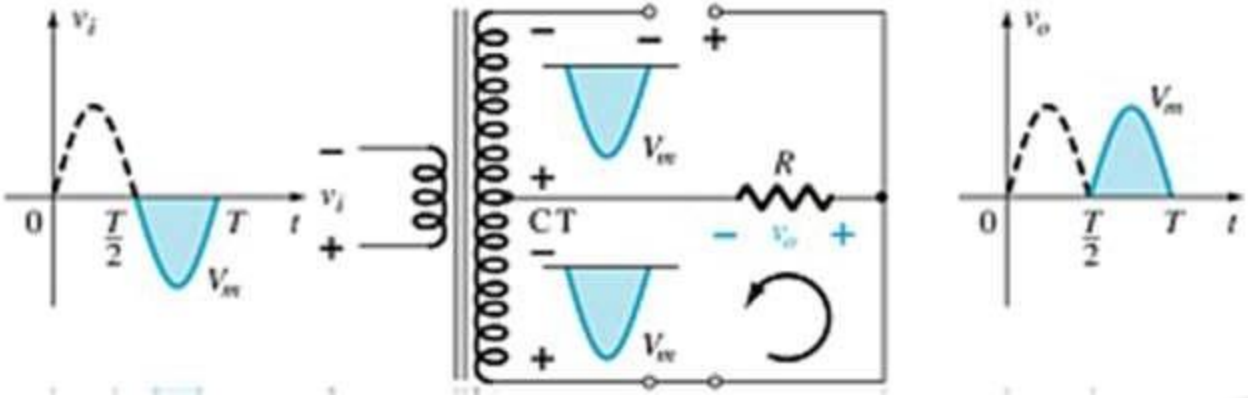
- When point B is positive (in the negative half of the cycle) with respect to point C, diode $D_2$ conducts in the forward direction and the current flowing through resistor R is in the same direction for both half-cycles.

- As the output voltage across the resistor R is the phasor sum of the two waveforms combined, this type of full wave rectifier circuit is also known as a “bi-phase” circuit.

# FULL-WAVE RECTIFIER




Current Flow during the positive half of the input cycle




Current Flow during the negative half of the input cycle

# FULL-WAVE RECTIFIER

## Average DC current:

$$I_{av} = I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t \, d\omega t$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$ for full wave rectifier

## Average (DC):

$$E_{DC} = I_{DC}R_L = \frac{2I_mR_L}{\pi}$$

Substituting value of $I_m$,

$$E_{DC} = \frac{2E_{sm}R_L}{\pi[R_f + R_s + R_L]} = \frac{2E_{sm}}{\pi\left[1 + \frac{R_f + R_s}{R_L}\right]}$$

But as $R_f$ and $R_s << R_L$ hence $\frac{R_f + R_s}{R_L} << 1$

$$\boxed{E_{DC} = \frac{2E_{sm}}{\pi}}$$

# FULL-WAVE RECTIFIER

## RMS Load Current (Irms):

$$I_{RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2 d(\omega t)} \rightarrow I_{RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi} [I_m \sin \omega t]^2 d(\omega t)} \rightarrow \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

## RMS Load Voltage:

$$\boxed{E_{L\,(RMS)} = I_{RMS} R_L = \frac{I_m}{\sqrt{2}} R_L}$$

## DC Output Power:

$$\text{D.C. Power output} = E_{DC} I_{DC} = I_{DC}^2 R_L$$

$$P_{DC} = I_{DC}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$P_{DC} = \frac{4}{\pi^2} I_m^2 R_L$$

# FULL-WAVE RECTIFIER

## AC input power (Pac):

The a.c. power input is given by,

$$\therefore \quad P_{AC} = I_{RMS}^2(R_f + R_s + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$\therefore \quad P_{AC} = \frac{I_m^2(R_f + R_s + R_L)}{2}$$

## Rectifier Efficiency (η):

$$\eta = \frac{P_{DC}\ \text{output}}{P_{AC}\ \text{input}} \Rightarrow \eta = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2(R_f + R_s + R_L)}{2}} \Rightarrow \eta = \frac{8\,R_L}{\pi^2(R_f + R_s + R_L)}$$

But if $R_f + R_s << R_L$, neglecting it from denominator

$$\eta = \frac{8\,R_L}{\pi^2(R_L)} = \frac{8}{\pi^2}$$

$$\therefore \quad \%\,\eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2\ \%$$

# FULL-WAVE RECTIFIER

## Ripple Factor:

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For full wave $I_{RMS} = I_m/\sqrt{2}$ and $I_{DC} = 2I_m/\pi$

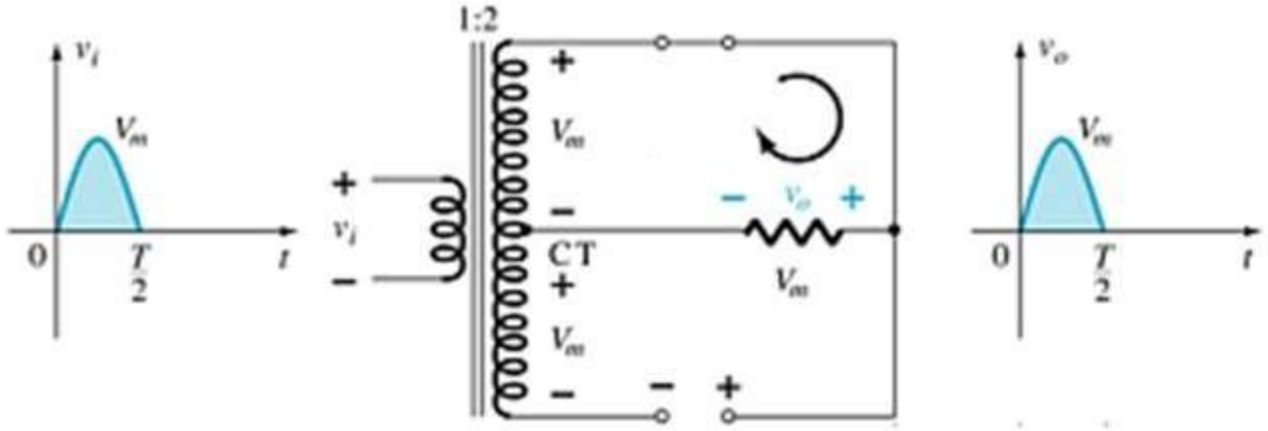
$$\text{Ripple factor} = \sqrt{\left[\frac{I_m/\sqrt{2}}{2I_m/\pi}\right]^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

Ripple factor = $\gamma = 0.48$

This indicates that the ripple contents in the output are 48% of the dc component which is much less than that for the half wave rectifier.

# FULL-WAVE RECTIFIER

## Peak Inverse Voltage:




PIV of diode = 2 $E_{sm}$

# FULL-WAVE RECTIFIER

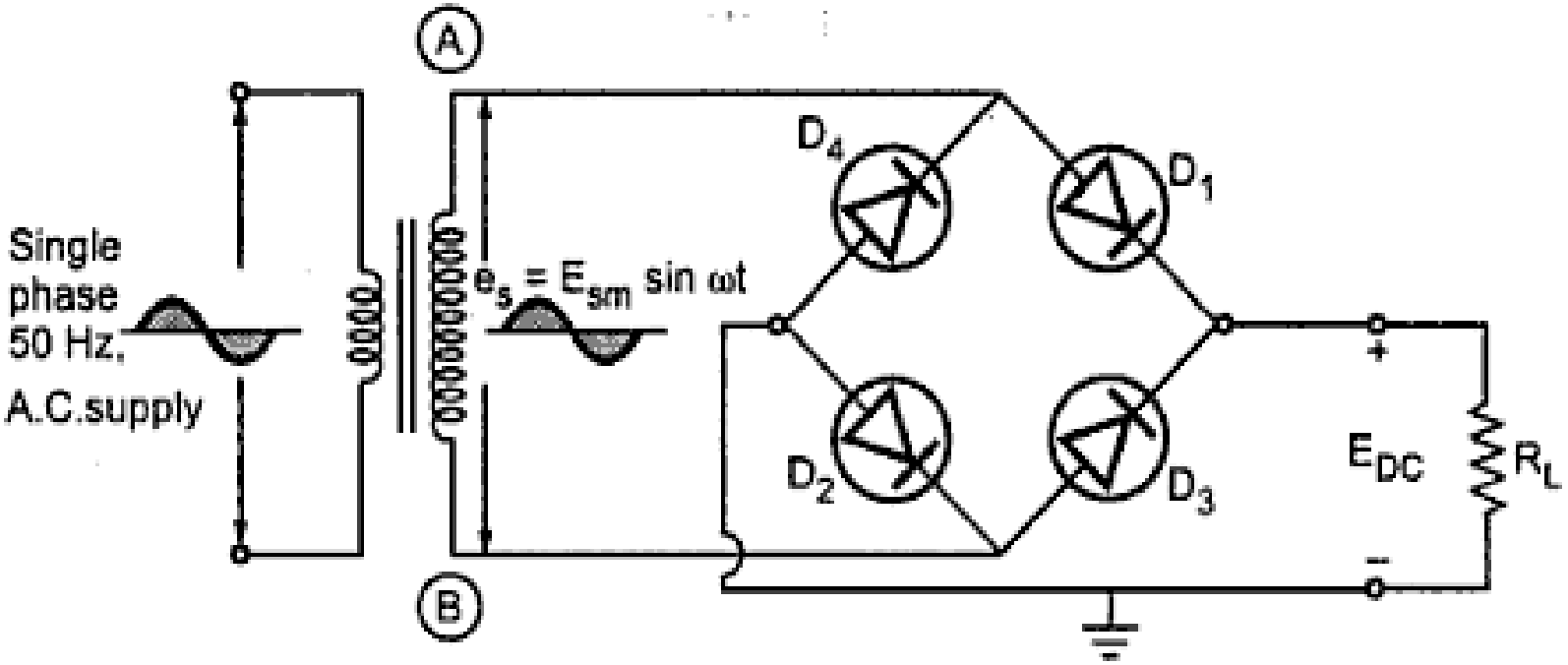
**Advantages of Full Wave Rectifier:**

- Efficiency is higher.
- The large dc power output
- The ripple factor is less

**Disadvantages of Full Wave Rectifier:**

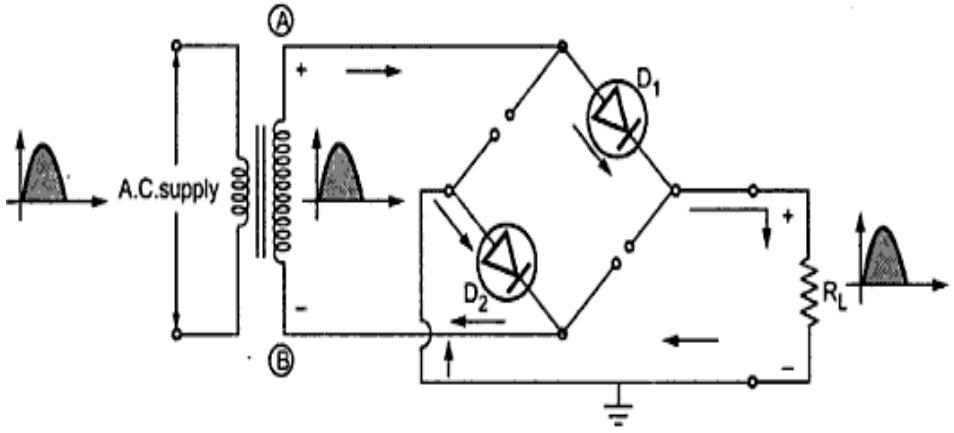
- PIV rating of diode is higher.
- Higher PIV diodes are larger in size and costlier.
- The cost of center tap transformer is high.

# BRIDGE RECTIFIER

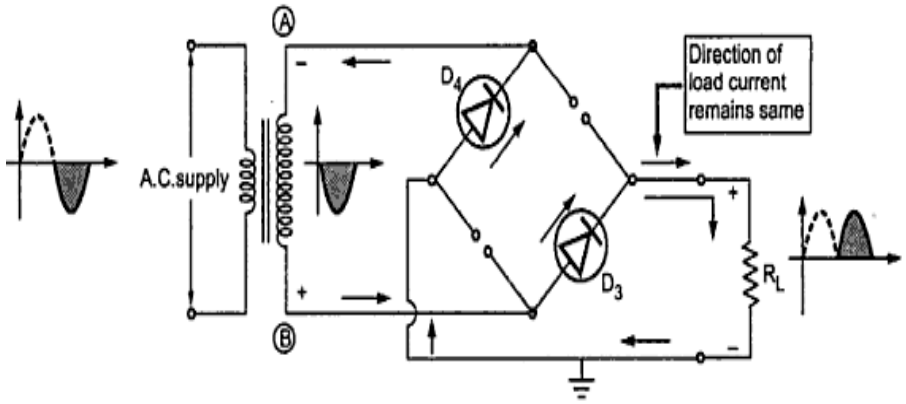



A Bridge rectifier that rectifies mains AC input to DC output. Bridge Rectifiers are widely used in power supplies that provide necessary DC voltage for the electronic components or devices.

# WORKING OF BRIDGE RECTIFIER



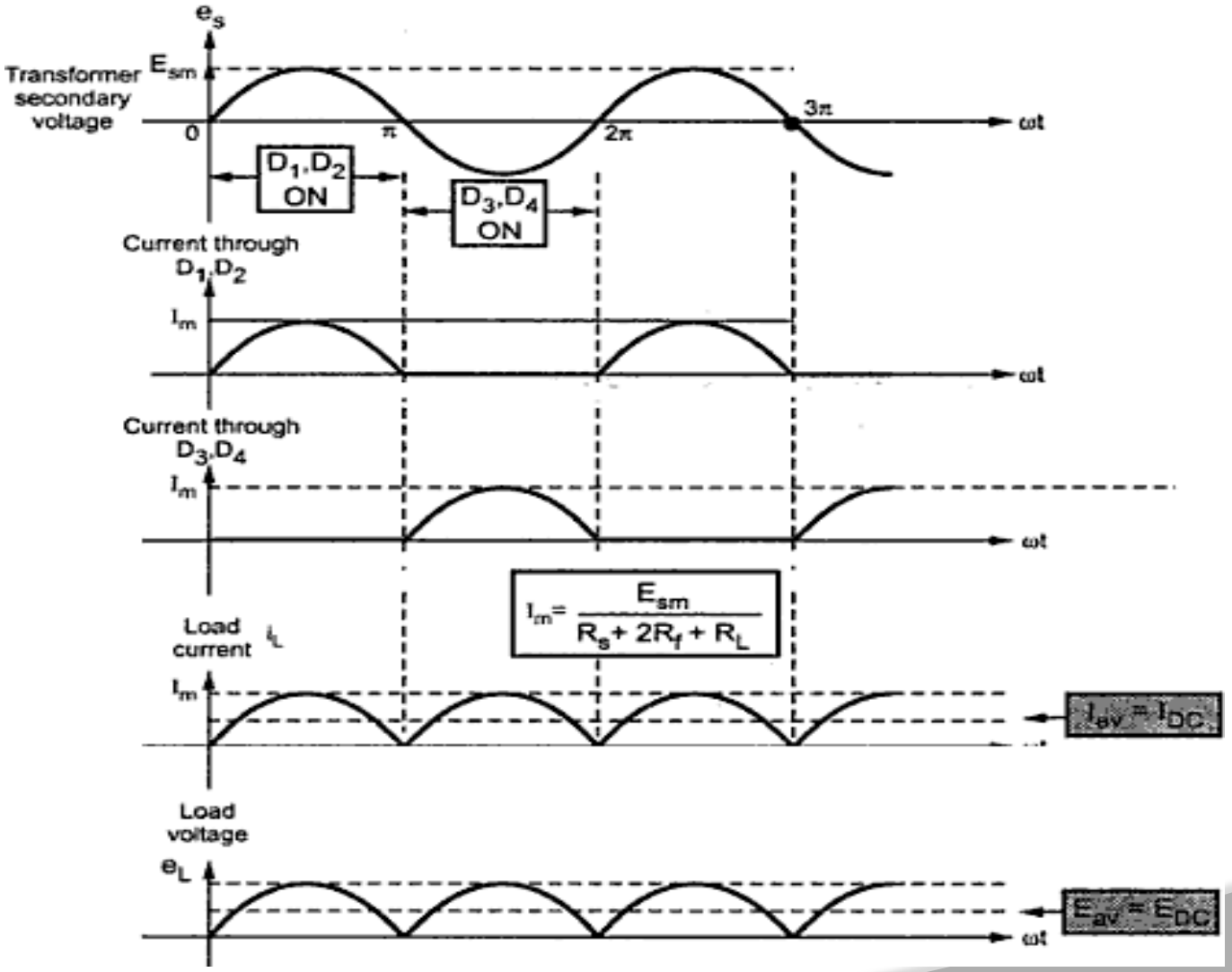

Current flow during positive half cycle




Current flow during negative half cycle

- During the positive half cycle of secondary voltage, the diodes D1 and D2 are forward-biased, but diodes D3 and D4 do no conduct. The current is through D1, R, D2 and secondary winding.
- During the negative half cycle, the diodes D3 and D4 are forward-biased, but diodes D1 and D2 do not conduct. The current is through D3, secondary winding, D4 and R.

# BRIDGE RECTIFIER WAVEFORMS



# BRIDGE RECTIFIER PARAMETERS

$$I_{DC} = \frac{2I_m}{\pi} \quad \text{and} \quad I_{RMS} = \frac{I_m}{\sqrt{2}}$$

$$E_{DC} = I_{DC} R_L = \frac{2E_{sm}}{\pi}$$

$$P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L) = \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

$$\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}, \quad \% \eta_{max} = 81.2\%$$

$$\gamma = 0.48$$

# RECTIFIERS WITH CAPACITIVE FILTER

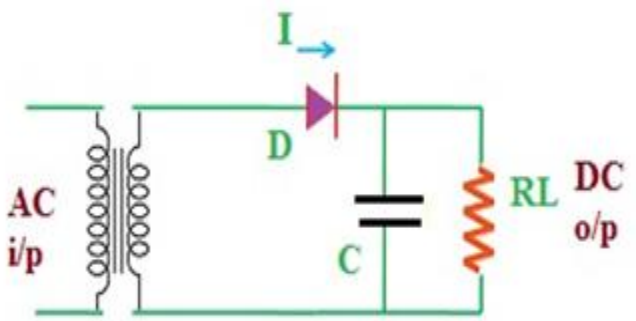



Fig: H/W rectifier with filter

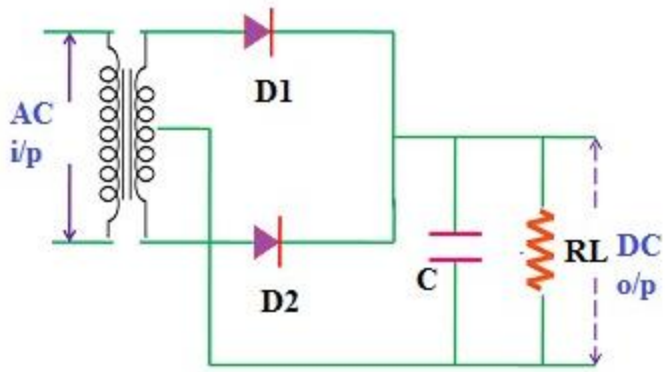
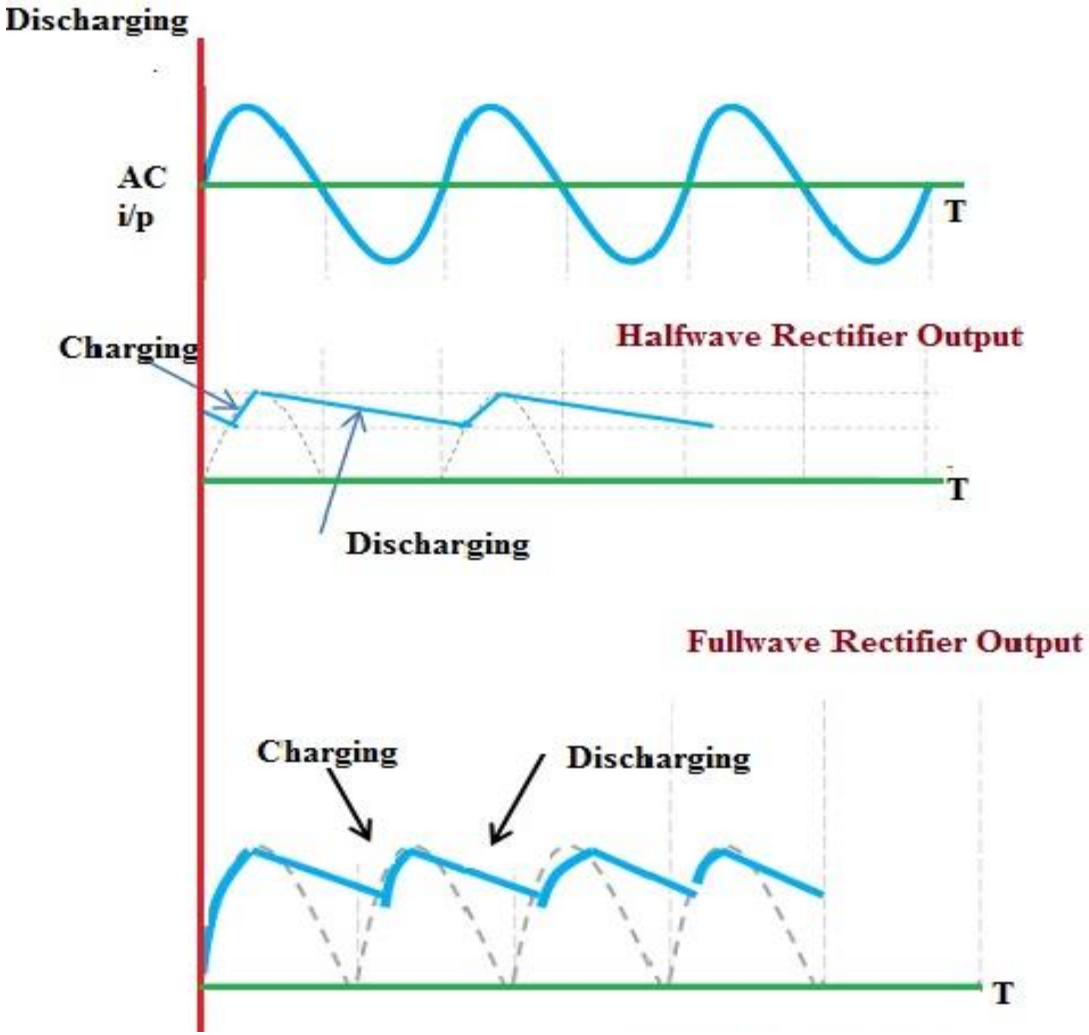



Fig: F/W rectifier with filter

- In full wave rectifier circuit using a capacitor filter, the capacitor C is located across the RL load resistor. The working of this rectifier is almost the same as a half wave rectifier.

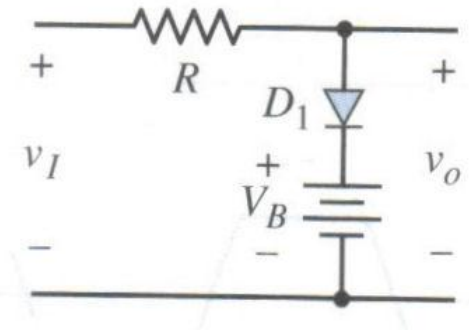
- Once the i/p AC voltage is applied throughout the positive half cycle, then the D1 diode gets forward biased and permits flow of current while the D2 diode gets reverse biased & blocks the flow of current.

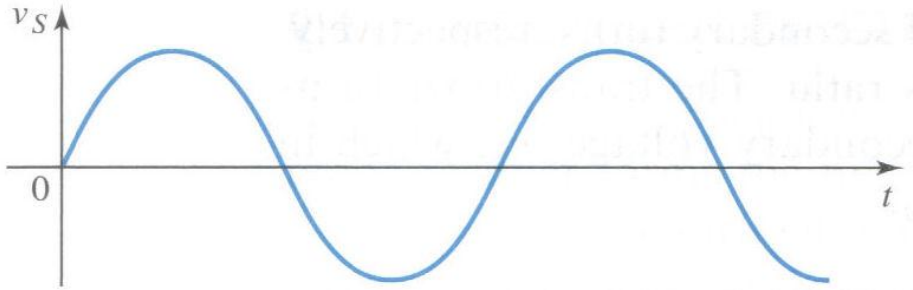
# RECTIFIERS WITH CAPACITIVE FILTER WAVEFORM



# CLIPPERS

- Clipper circuits, also called **limiter circuits**, are used to eliminate portion of a signal that are above or below a specified level – clip value.
- The purpose of the diode is that when it is turn on, it provides the clip value
- Clip value = V'. To find V', use KVL at L1
- The equation is : $V' - V_B - V\gamma = 0 \rightarrow V' = V_B + V\gamma$



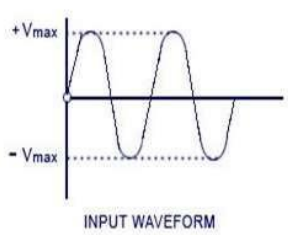



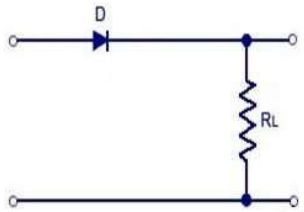

- Then, set the conditions
  - If **Vi > V'**, what happens? → diode conducts, hence Vo = V'
  - If **Vi < V'**, what happens? → diode off, open circuit, no current flow, Vo = Vi

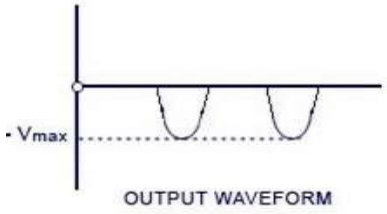
# CLIPPER CIRCUITS

**positive clipper:**

In a positive clipper, the positive half cycles of the input voltage will be removed.

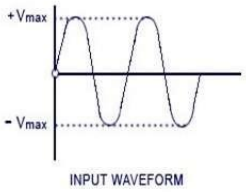


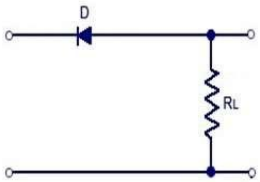



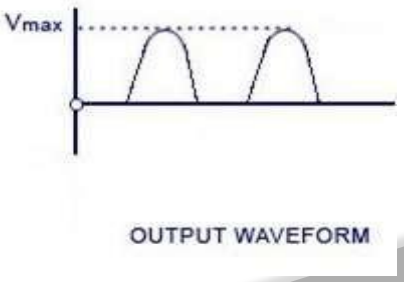




**Negative clipper:**

In a Negative clipper, the negative half cycles of the input voltage will be removed.



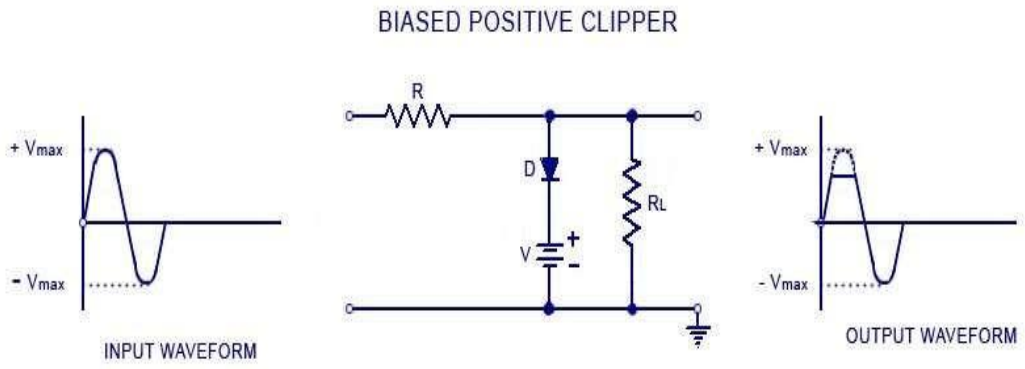



# CLIPPER CIRCUITS

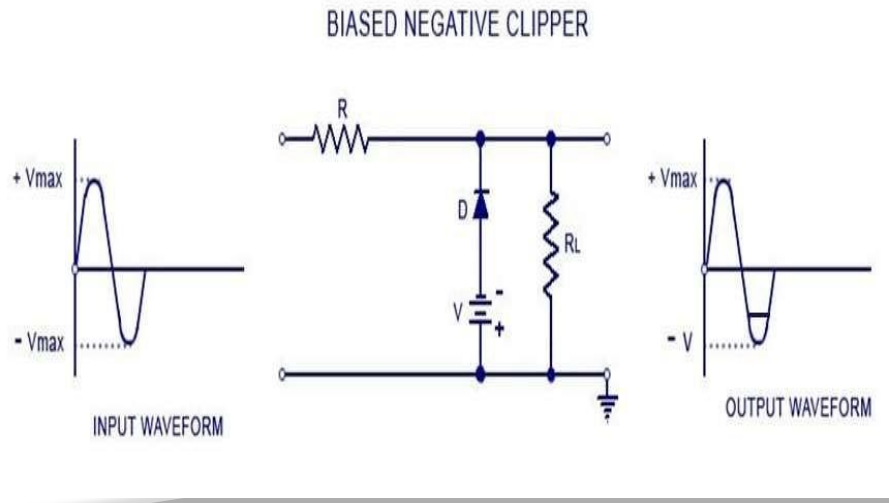
## Biased Positive Clipper:

- When the input signal voltage is positive, the diode 'D' is reverse-biased. This causes it to act as an open-switch.



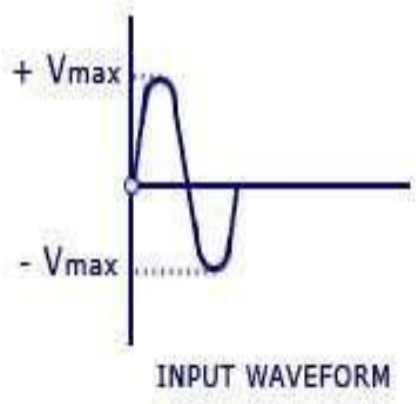

## Biased Negative Clipper:

When the input signal voltage is negative its also reverse biased but in this case battery voltage is more than the input voltage so its acts like an close switch.

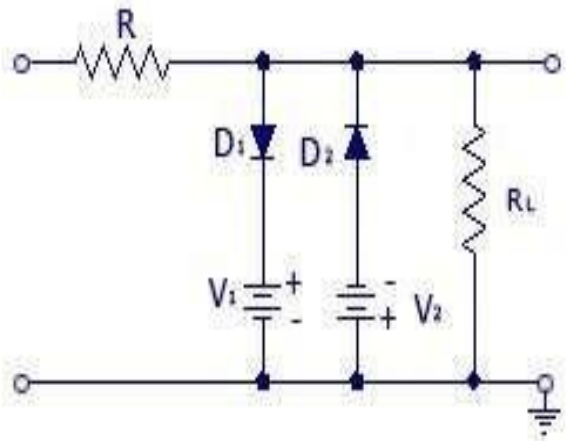


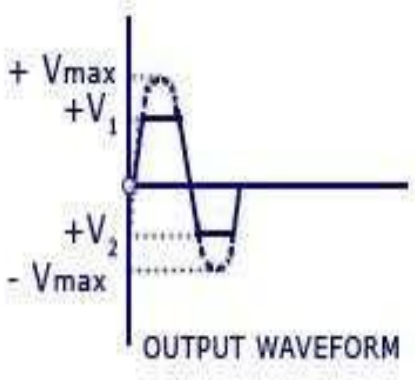
# TWO LEVEL-CLIPPER

- When a portion of both positive and negative of each half cycle of the input voltage is to be clipped (or removed), combination clipper is employed.



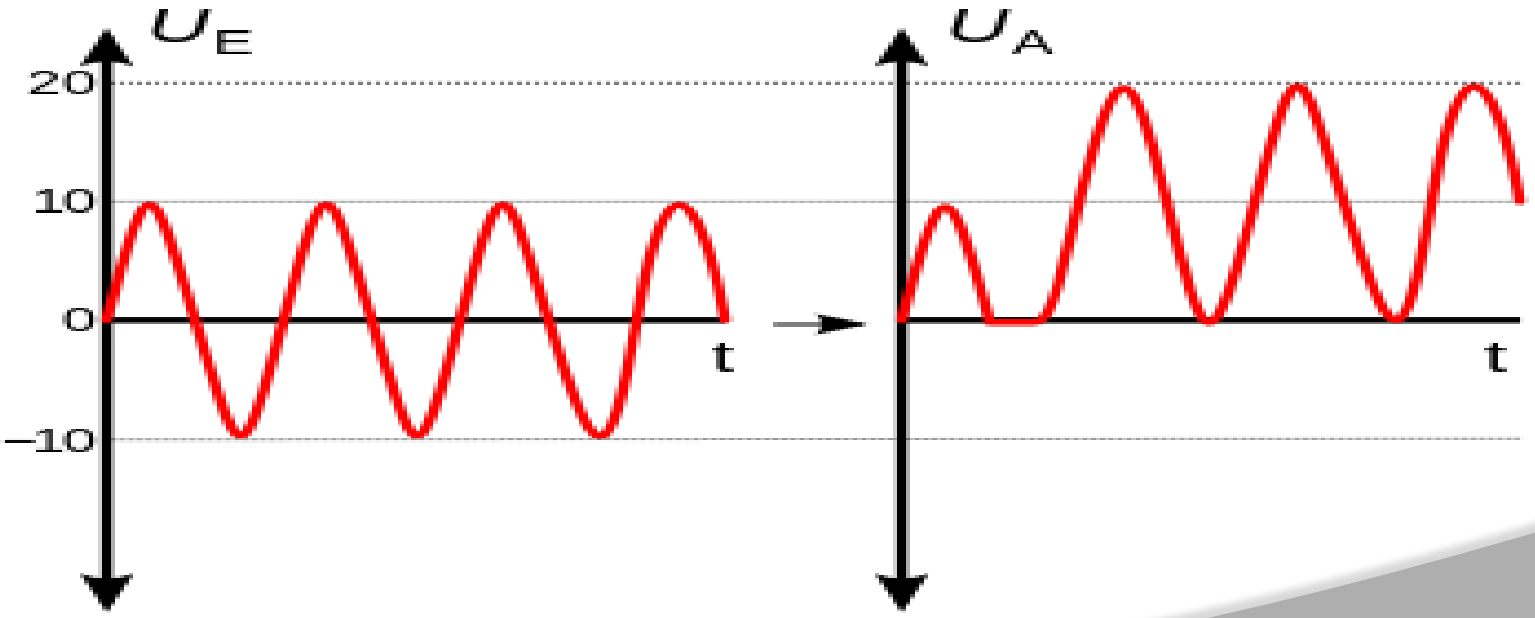

COMBINATION CLIPPER



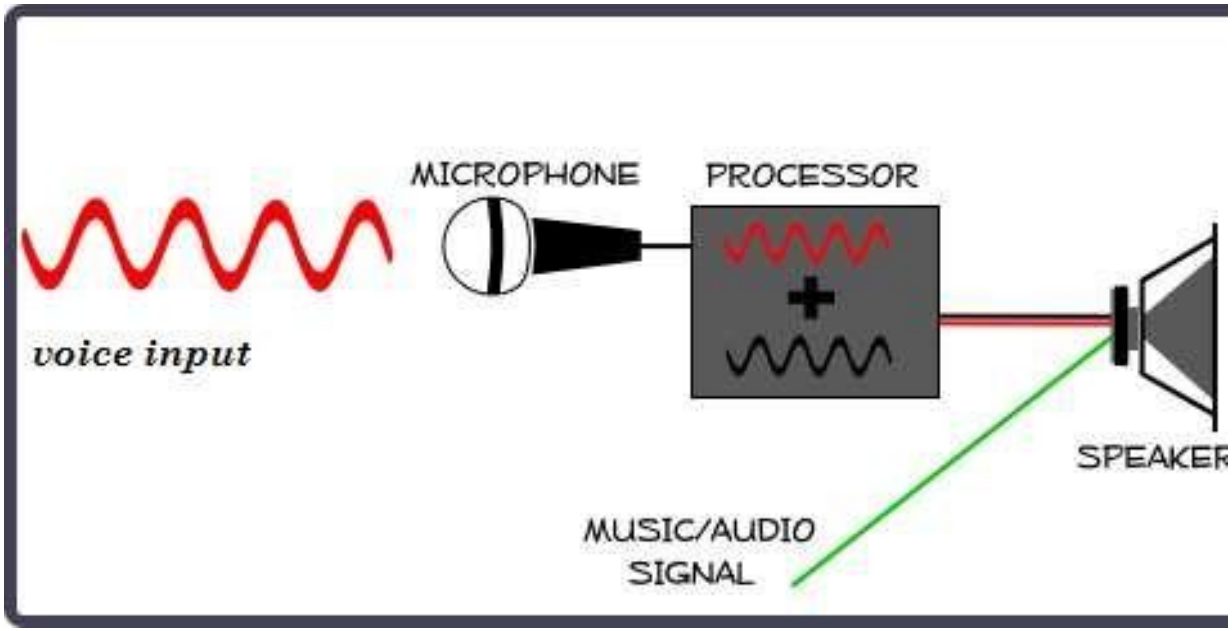
# CLAMPERS

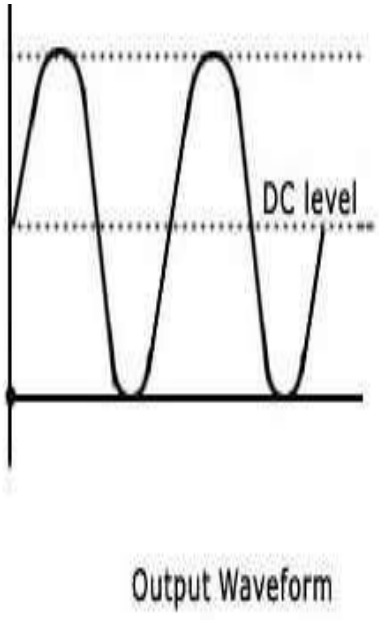
- A circuit which adds DC value to an AC wave form without changing its waveform.
- In this circuit we use a diode and a capacitor and a resistor for measure voltage in our circuit.



# WHY CLAMPER USE?

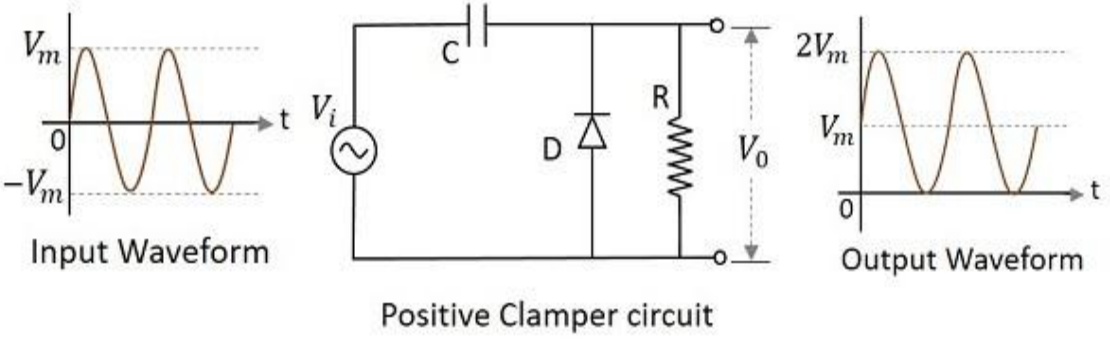
- Clamper use to increase the wavelength of input wave.
- Like an sound system amplifier.



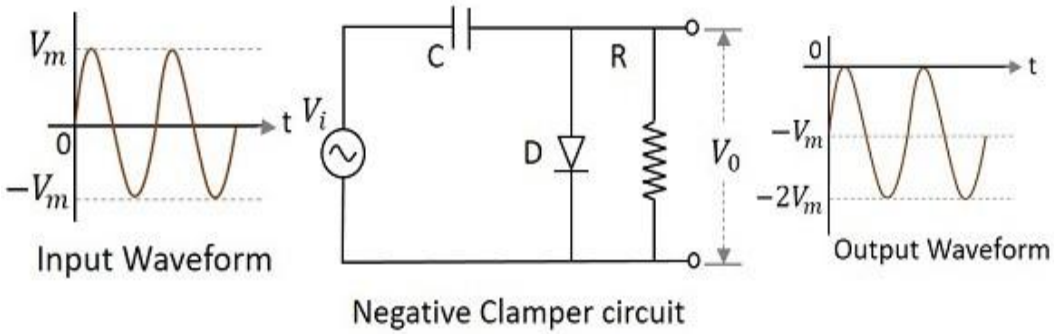



# CLAMPERS

In positive clamper diode is forward biased and current flow is maximum.
Due to the presence of the capacitor it will double the wavelength on positive side.

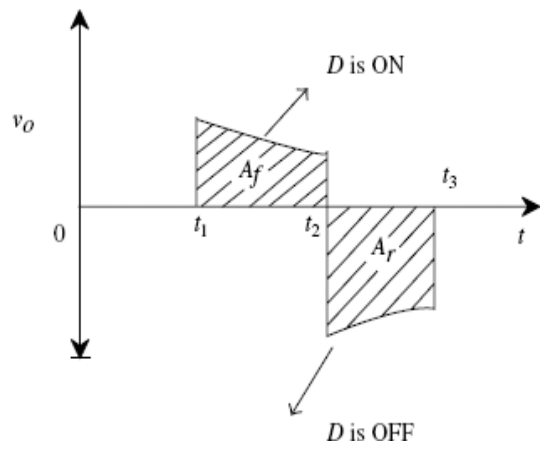



In this capacitor negatively charged and the output is double of the input of the negative side.



# CLAMPING CIRCUIT THEOREM

The clamping circuit theorem states that under steady-state conditions, for any input waveform, the ratio of the area under the output voltage curve in the forward direction to that in the reverse direction is equal to the ratio $R_f/R$.




In the time interval $t_1$ to $t_2$, $D$ is ON. Hence, during this period, the charge builds up on the capacitor $C$. If $i_f$ is the diode current, the charge gained by the capacitor during the interval $t_1$ to $t_2$ is:

$$q_1 = \int_{t_1}^{t_2} i_f \, dt$$

# CLAMPING CIRCUIT THEOREM

However, $i_f = V_f/R_f$, where $V_f$ is the diode forward voltage:

$$q_1 = \frac{1}{R_f}\int_{t_1}^{t_2} V_f\, dt$$

During the interval $t_2$ to $t_3$, $D$ is OFF. Hence, the capacitor discharges and the charge lost by $C$ is:

$$q_2 = \int_{t_2}^{t_3} i_r\, dt$$

Put $i_r = V_r/R$, where $V_r$ is the diode reverse voltage:

$$q_2 = \frac{1}{R}\int_{t_2}^{t_3} V_r\, dt$$

# CLAMPING CIRCUIT THEOREM

At steady state, the charge gained is equal to the charge lost. In other words, $q_1 = q_2$.

$$\frac{1}{R_f}\int_{t_1}^{t_2} V_f\,dt = \frac{1}{R}\int_{t_2}^{t_3} V_r\,dt$$

$$A_f = \int_{t_1}^{t_2} V_f\,dt \quad \text{and} \quad A_r = \int_{t_2}^{t_3} V_r\,dt$$

Here, $A_f$ is the area with $D$ in the ON state and $A_r$ is the area under the output curve with $D$ in the OFF state.

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{or} \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$

# COMPARATORS

- An amplitude comparator is a circuit that tells the time instant at which the input amplitude has reached a reference level.

  $v_o = 0$ for $t < t_1$

  $v_o = V$ for $t \geq t_1$

- The distinction between comparator circuits and the clipping circuits is that, in a comparator there is no interest in reproducing any part of the signal waveform, whereas in a clipping circuit, part of the signal waveform is needed to be reproduced without any distortion.

# COMPARATORS

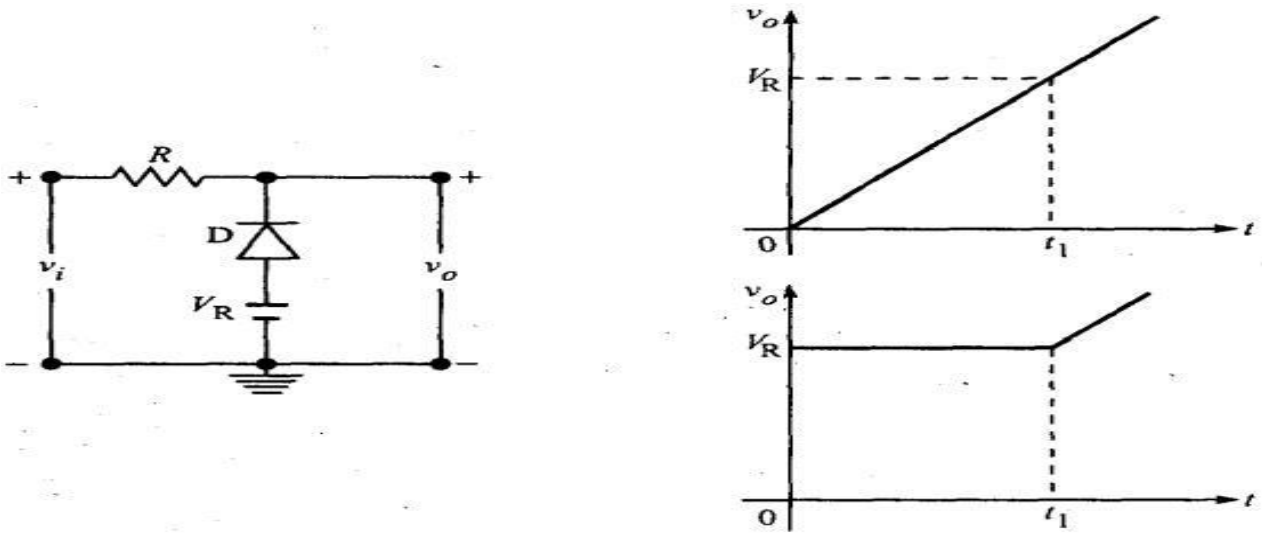



**Figure 2.70** Diode comparator.

- Comparators may be non-regenerative or regenerative.
- Clipping circuits are non-regenerative comparators.
- Schmitt trigger and oscillators are regenerative comparators.


# UNIT-II
# BIPOLAR JUNCTION TRANSISTOR (BJT)


# UNIT-II
# BIPOLAR JUNCTION TRANSISTOR (BJT)

# Outline

- Principle of Operation and characteristics
- Common Emitter Configuration
- Common Base Configuration
- Common Collector Configuration
- Operating point
- DC & AC load lines
- Transistor Hybrid parameter model
- Determination of h-parameters from transistor characteristics
- Conversion of h-parameters
- Problems

# Principle of Operation and characteristics

# Principle of Operation and characteristics

- The basic of electronic system nowadays is semiconductor device.
- The famous and commonly use of this device is BJTs (Bipolar Junction Transistors).
- It can be use as amplifier and logic switches.
- BJT consists of three terminal:
  - → collector : C
  - → base : B
  - →emitter : E
- Two types of BJT : pnp and npn

# Principle of Operation and characteristics

- 3 layer semiconductor device consisting:
  - 2 n- and 1 p-type layers of material → npn transistor
  - 2 p- and 1 n-type layers of material →pnp transistor
- The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material
- A single pn junction has two different types of bias:
  - forward bias
  - reverse bias
- Thus, a two-pn-junction device has four types of bias.

# Principle of Operation and characteristics

- Base is located at the middle and more thin from the level of collector and emitter
- The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material

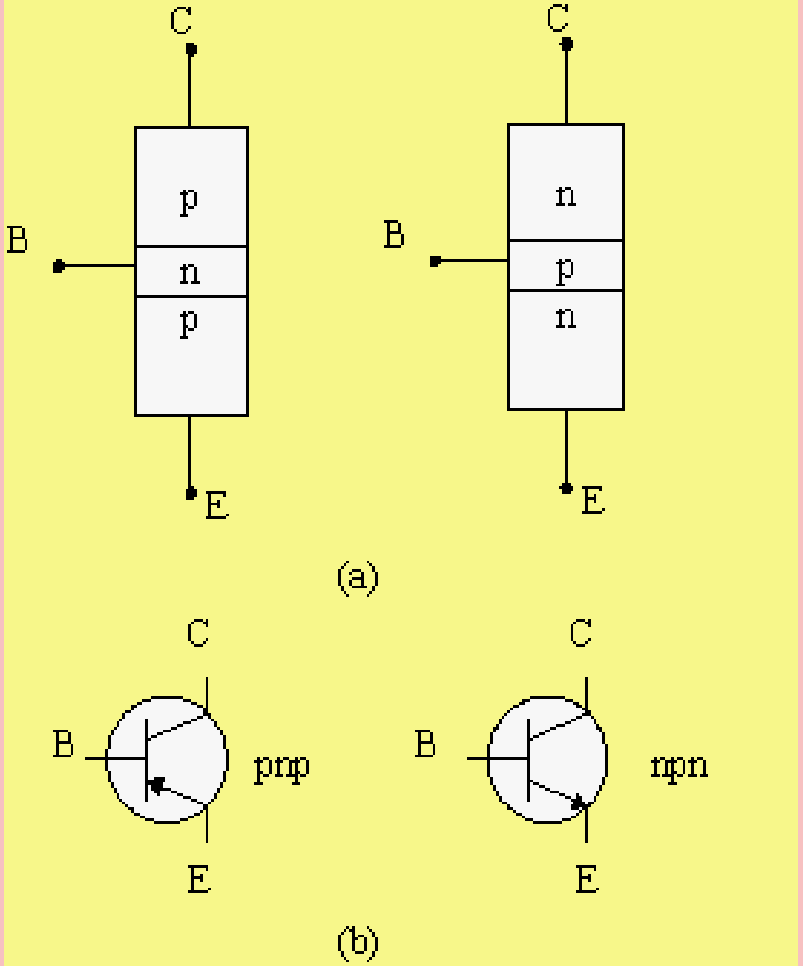



Fig. 4.1: (a) Position of terminals (b) Type of BJT

# Principle of Operation and characteristics

-The arrow is always drawn on the emitter

-The arrow always point toward the n-type

-The arrow indicates the direction of the emitter current:

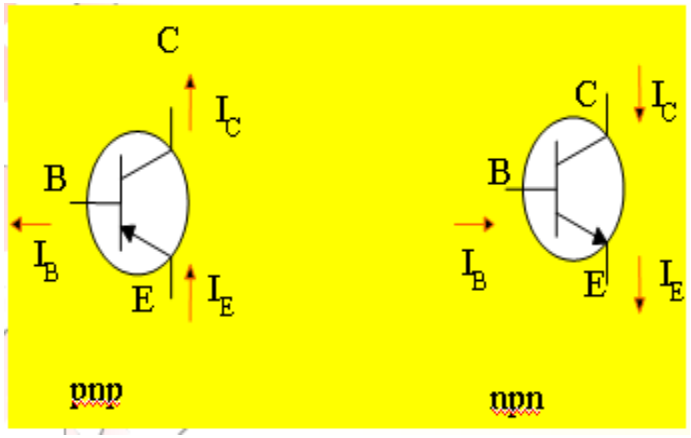
pnp:E→ B

npn: B→ E

$I_C$=the collector current

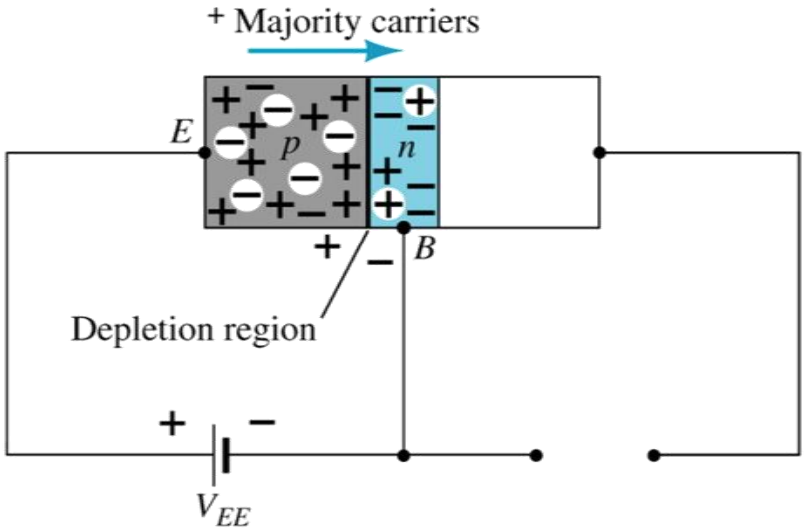
$I_B$= the base current

$I_E$= the emitter current

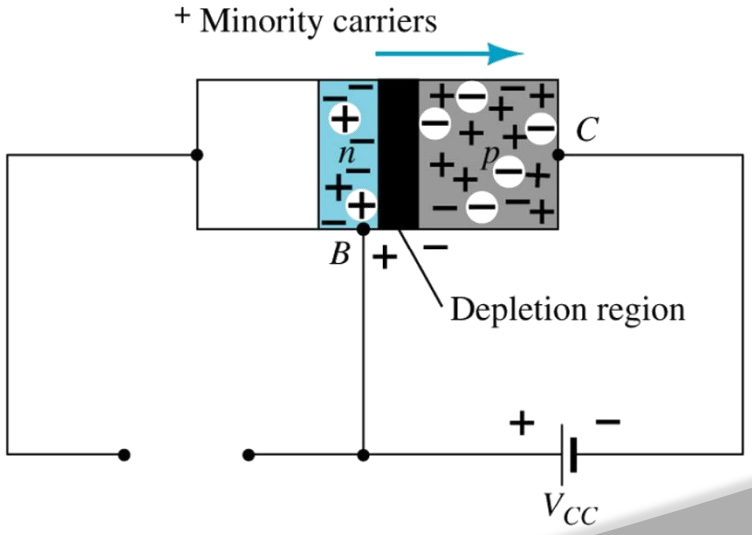


# Principle of Operation and characteristics

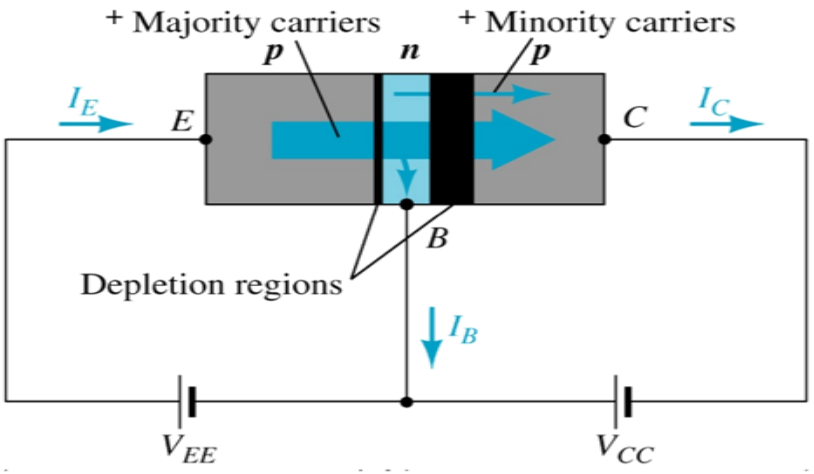
- The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.
- One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.




Forward-biased junction of a pnp transistor




Reverse-biased junction of a pnp transistor




- **Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.**
- **Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.**
- **A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.**
- **The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.**

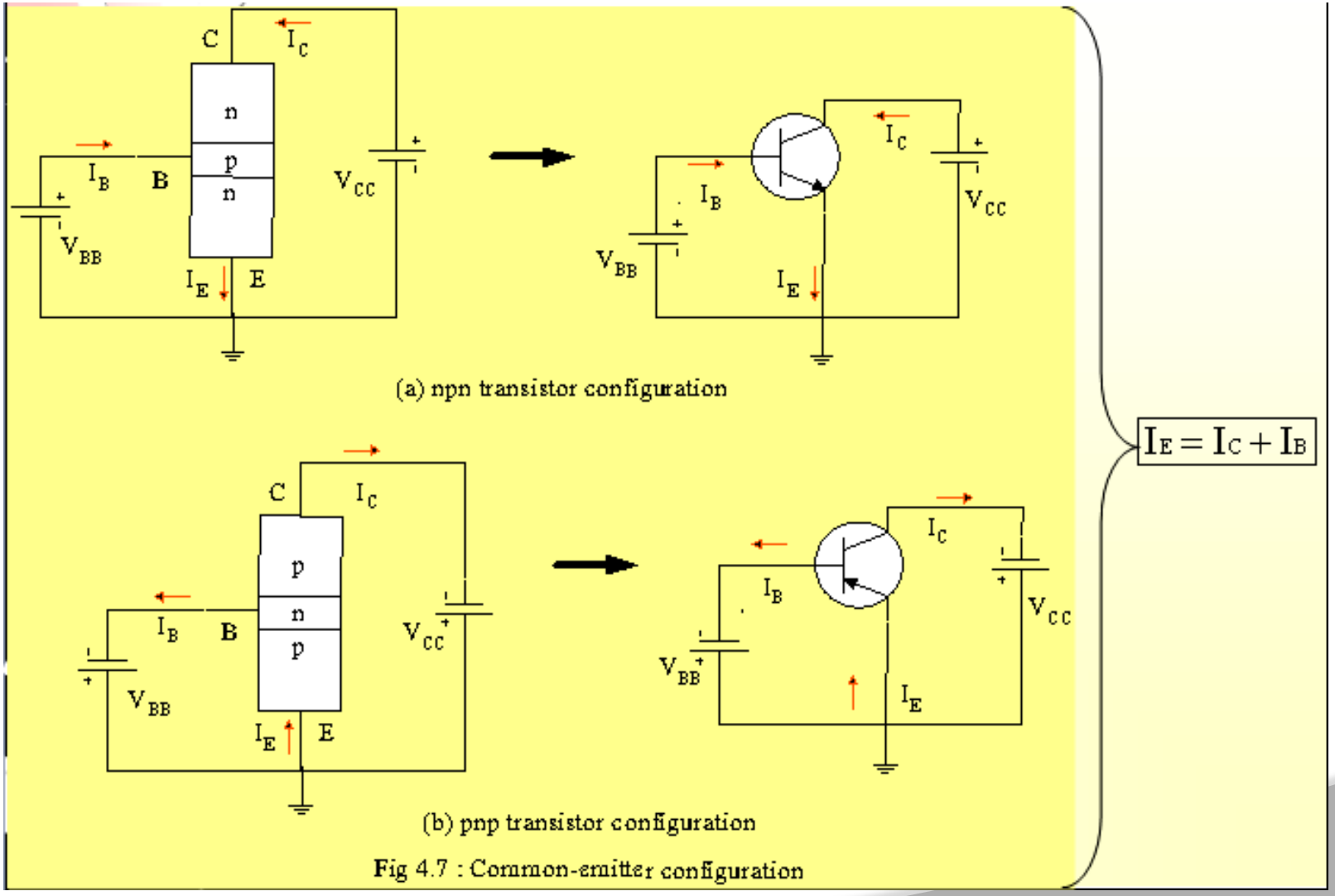
- Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material.
- Applying KCL to the transistor :
- $$I_E = I_C + I_B$$
- The  comprises of two components – the majority and minority carriers
- $$I_C = I_{Cmajority} + I_{COminority}$$
- $I_{CO}$ – $I_C$ current with emitter terminal open and is called leakage current.

# Common Emitter Configuration

# Common Emitter Configuration

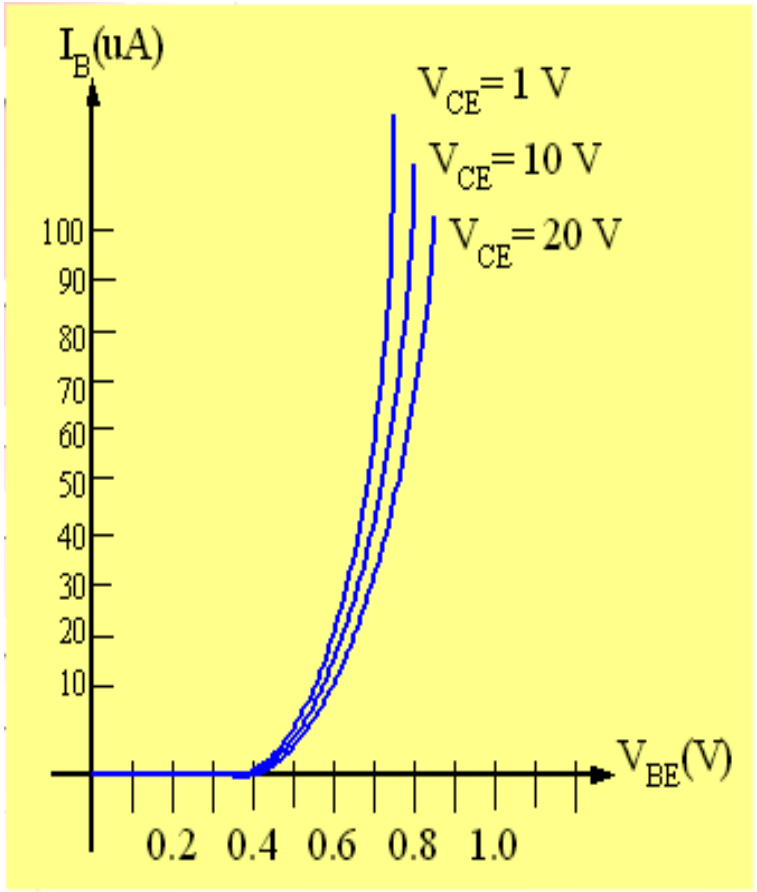
- It is called common-emitter configuration since :
  - emitter is common or reference to both input and output terminals.
  - emitter is usually the terminal closest to or at ground potential.
- Almost amplifier design is using connection of CE due to the high gain for current and voltage.
- Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters

# Common Emitter Configuration



# Common Emitter Configuration

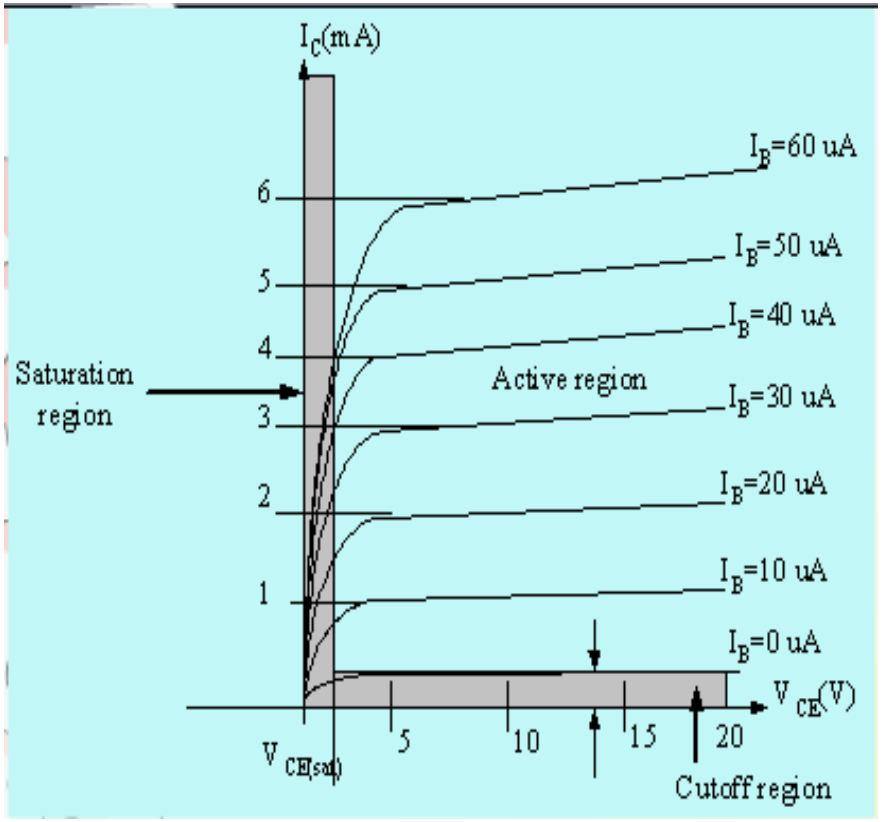
- $I_B$ is microamperes compared to miliamperes of $I_C$.
- $I_B$ will flow when $V_{BE}$ > 0.7V for silicon and 0.3V for germanium
- Before this value $I_B$ is very small and no $I_B$.
- Base-emitter junction is forward bias
- Increasing $V_{CE}$ will reduce $I_B$ for different values.




**Input characteristics for a common-emitter NPN transistor**

# Common Emitter Configuration

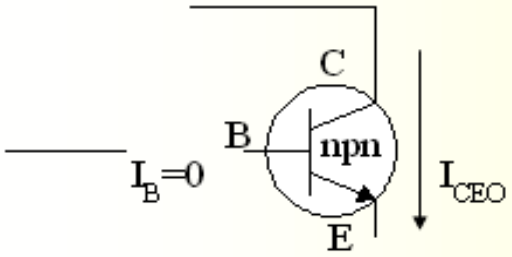
- For small $V_{CE}$ ($V_{CE} < V_{CESAT}$, $I_C$ increase linearly with increasing of $V_{CE}$
- $V_{CE} > V_{CESAT}$ $I_C$ not totally depends on $V_{CE}$ → constant $I_C$
- $I_B$(uA) is very small compare to $I_C$ (mA). Small increase in $I_B$ cause big increase in $I_C$
- $I_B$=0 A → $I_{CEO}$ occur.
- Noticing the value when $I_C$=0A. There is still some value of current flows.

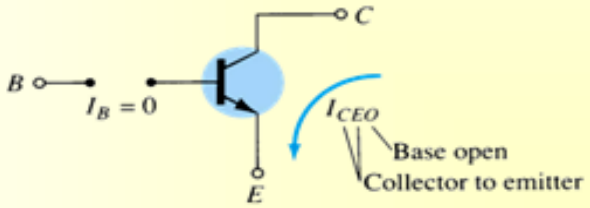



**Output characteristics for a common-emitter npn transistor**

# Common Emitter Configuration

| Active region | Saturation region | Cut-off region |
|---|---|---|
| • B-E junction is forward bias<br>• C-B junction is reverse bias<br>• can be employed for voltage, current and power amplification | • B-E and C-B junction is forward bias, thus the values of $I_B$ and $I_C$ is too big.<br>• The value of $V_{CE}$ is so small.<br>• Suitable region when the transistor as a logic switch.<br>• NOT and avoid this region when the transistor as an amplifier. | • region below $I_B=0\mu A$ is to be avoided if an undistorted o/p signal is required<br>• B-E junction and C-B junction is reverse bias<br>• $I_B=0$, $I_C$ not zero, during this condition $I_C=I_{CEO}$ where is this current flow when B-E is reverse bias. |



# Common Emitter Configuration

## Transistor parameters

- **Dynamic input resistance ($r_i$)**

  **Dynamic input resistance is defined as the ratio of change in input voltage or base voltage ($V_{BE}$) to the corresponding change in input current or base current ($I_B$), with the output voltage or collector voltage ($V_{CE}$) kept at constant. In CE configuration, the input resistance is very low.**

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B}, \qquad V_{CE} = \text{constant}$$

# Common Emitter Configuration

## Dynamic output resistance ($r_o$)

**Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage ($V_{CE}$) to the corresponding change in output current or collector current ($I_C$), with the input current or base current ($I_B$) kept at constant. In CE configuration, the output resistance is high.**

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}, \qquad I_B = \text{constant}$$

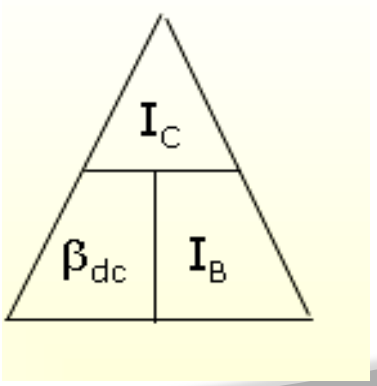
# Common Emitter Configuration

## Beta (β) or amplification factor

- The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (βdc ) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point).
- It's define by the following equation:

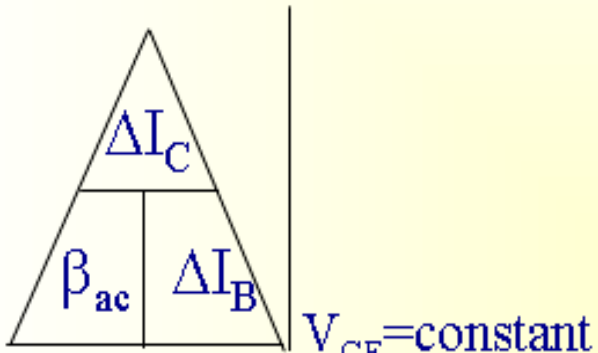
$$30 < \beta_{dc} < 300 \rightarrow 2N3904$$

- On data sheet, $\beta_{dc}$=*hfe* with *h* is derived from ac hybrid equivalent circuit. FE are derived from forward-current amplification and common-emitter configuration respectively.



# Common Emitter Configuration

- For ac conditions an ac beta has been defined as the changes of collector current ($I_C$) compared to the changes of base current ($I_B$) where $I_C$ and $I_B$ are determined at operating point.
- On data sheet, $\beta_{ac}$=*hfe*
- It can defined by the following equation:



# Common Base Configuration

# Common Base Configuration

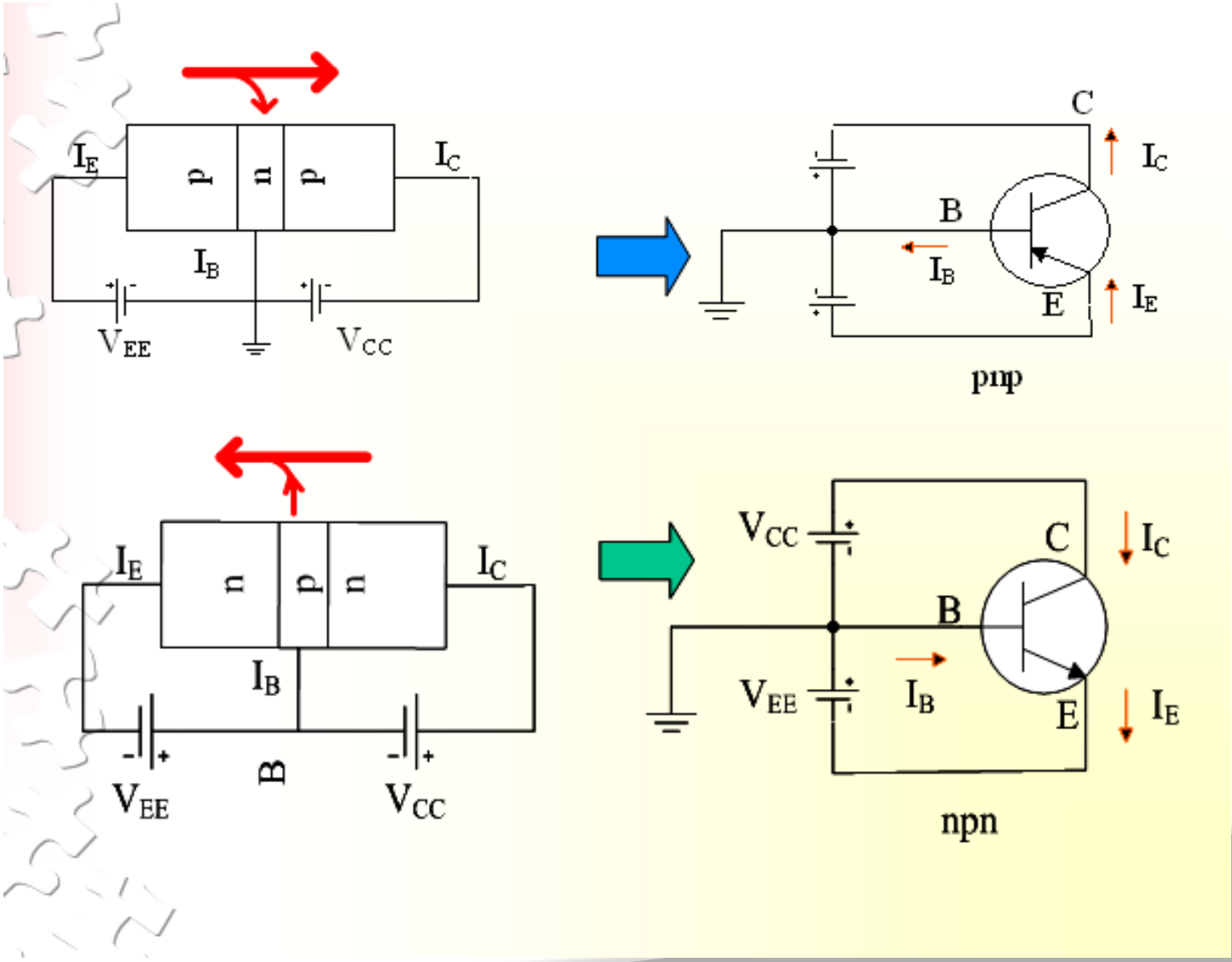
•Common-base terminology is derived from the fact that the :- base is common to both input and output of the configuration.

• base is usually the terminal closest to or at ground potential.

•All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

•Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

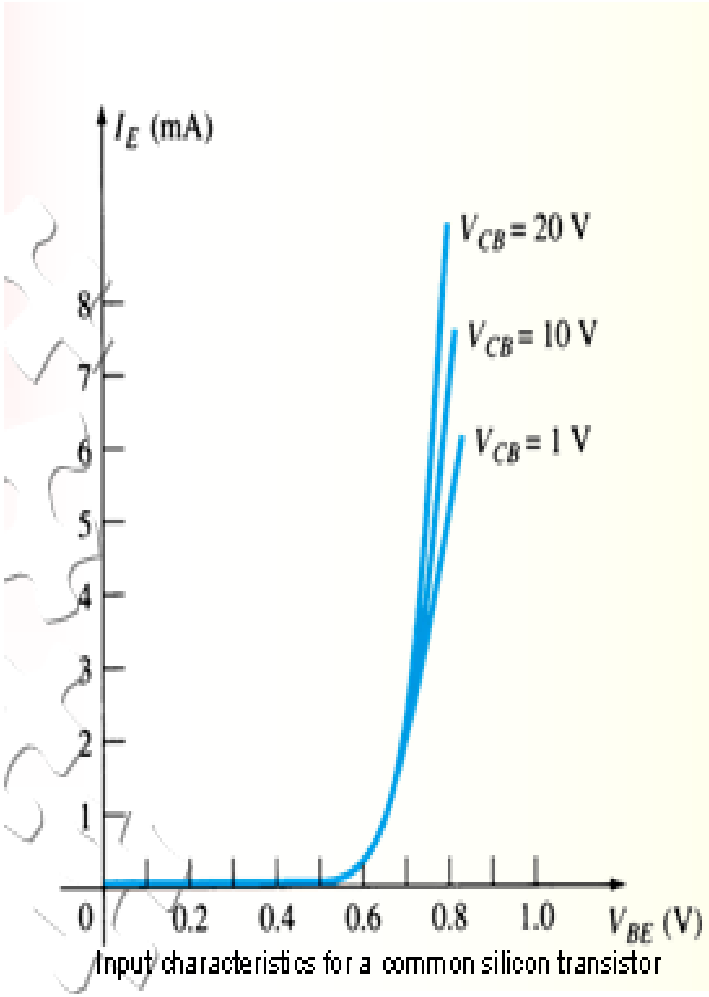
# Common Base Configuration



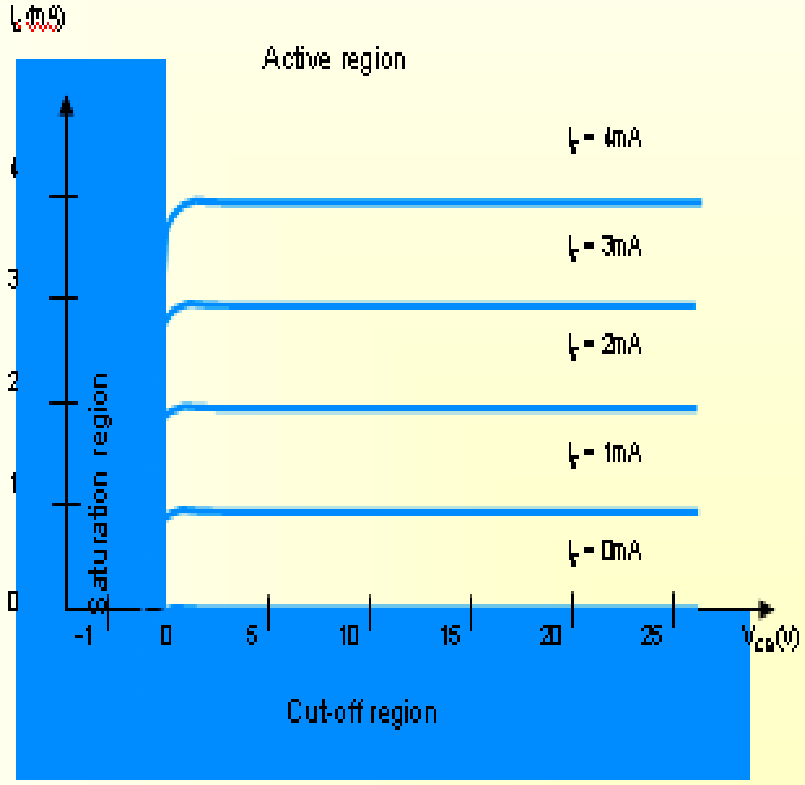
# Common Base Configuration

- To describe the behavior of common-base amplifiers requires two set of characteristics:
  - Input or driving point characteristics.
  - Output or collector characteristics
- The output characteristics has 3 basic regions:
  - Active region –defined by the biasing arrangements
  - Cutoff region – region where the collector current is 0A
  - Saturation region- region of the characteristics to the left of $V_{CB}$ = 0V

# Common Base Configuration




Input characteristics for a common silicon transistor




Output of collector characteristics for common-base transistor amplifier

# Common Base Configuration

| Active region | Saturation region | Cut-off region |
|---|---|---|
| • $I_E$ increased, Ic increased<br>• BE junction forward bias and CB junction reverse bias<br>• Refer to the graf, $Ic \approx I_E$<br>• Ic not depends on $V_{CB}$<br>• Suitable region for the transistor working as amplifier | • BE and CB junction is forward bias<br>• Small changes in $V_{CB}$ will cause big different to Ic<br>• The allocation for this region is to the left of $V_{CB} = 0$ V. | • Region below the line of $I_E = 0$ A<br>• BE and CB is reverse bias<br>• no current flow at collector, only leakage current |

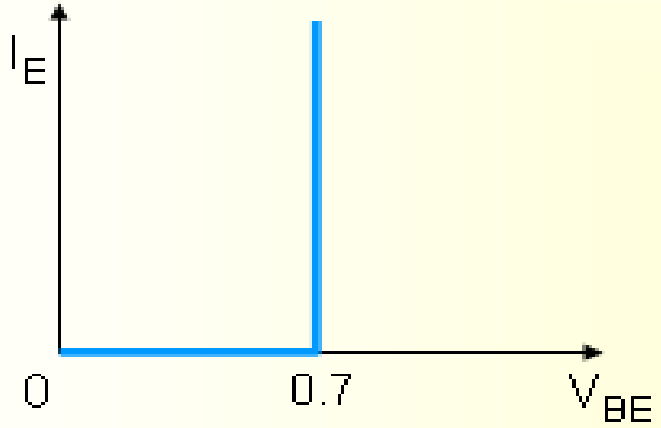
# Common Base Configuration

- The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$$I_C \approx IE$$

- Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be

$$V_{BE} = 0.7V$$



# Common Base Configuration

- **Early effect**
- **Due to forward bias, the base-emitter junction $J_E$ acts as a forward biased diode and due to reverse bias, the collector-base junction $J_C$ acts as a reverse biased diode.**
- **Therefore, the width of the depletion region at the base-emitter junction $J_E$ is very small whereas the width of the depletion region at the collector-base junction $J_C$ is very large.**
- **If the output voltage $V_{CB}$ applied to the collector-base junction $J_C$ is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases. This dependency of base width on the output voltage ($V_{CB}$) is known as an early effect.**
- **If the output voltage $V_{CB}$ applied to the collector-base junction $J_C$ is highly increased, the base width may be reduced to zero and causes a voltage breakdown in the transistor. This phenomenon is known as punch through.**

# Common Base Configuration

## Transistor parameters

- **Dynamic input resistance ($r_i$)**

  **Dynamic input resistance is defined as the ratio of change in input voltage or emitter voltage ($V_{BE}$) to the corresponding change in input current or emitter current ($I_E$), with the output voltage or collector voltage ($V_{CB}$) kept at constant.**

- **The input resistance of common base amplifier is very low.**

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}, \qquad V_{CB} = \text{constant}$$

# Common Base Configuration

## Dynamic output resistance (ro)

**Dynamic output resistance is defined as the ratio of change in output voltage or collector voltage (VCB) to the corresponding change in output current or collector current (IC), with the input current or emitter current (IE) kept at constant. The output resistance of common base amplifier is very high.**

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}, \qquad I_E = \text{constant}$$

# Common Base Configuration

- In the dc mode the level of $I_C$ and $I_E$ due to the majority carriers are related by a quantity called alpha

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

- It can then be summarize to $I_C = \alpha I_E$ (ignore $I_{CBO}$ due to small value)
- For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

- Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of $\alpha$ is typical from 0.9 ~ 0.998.

# Common – Collector Configuration

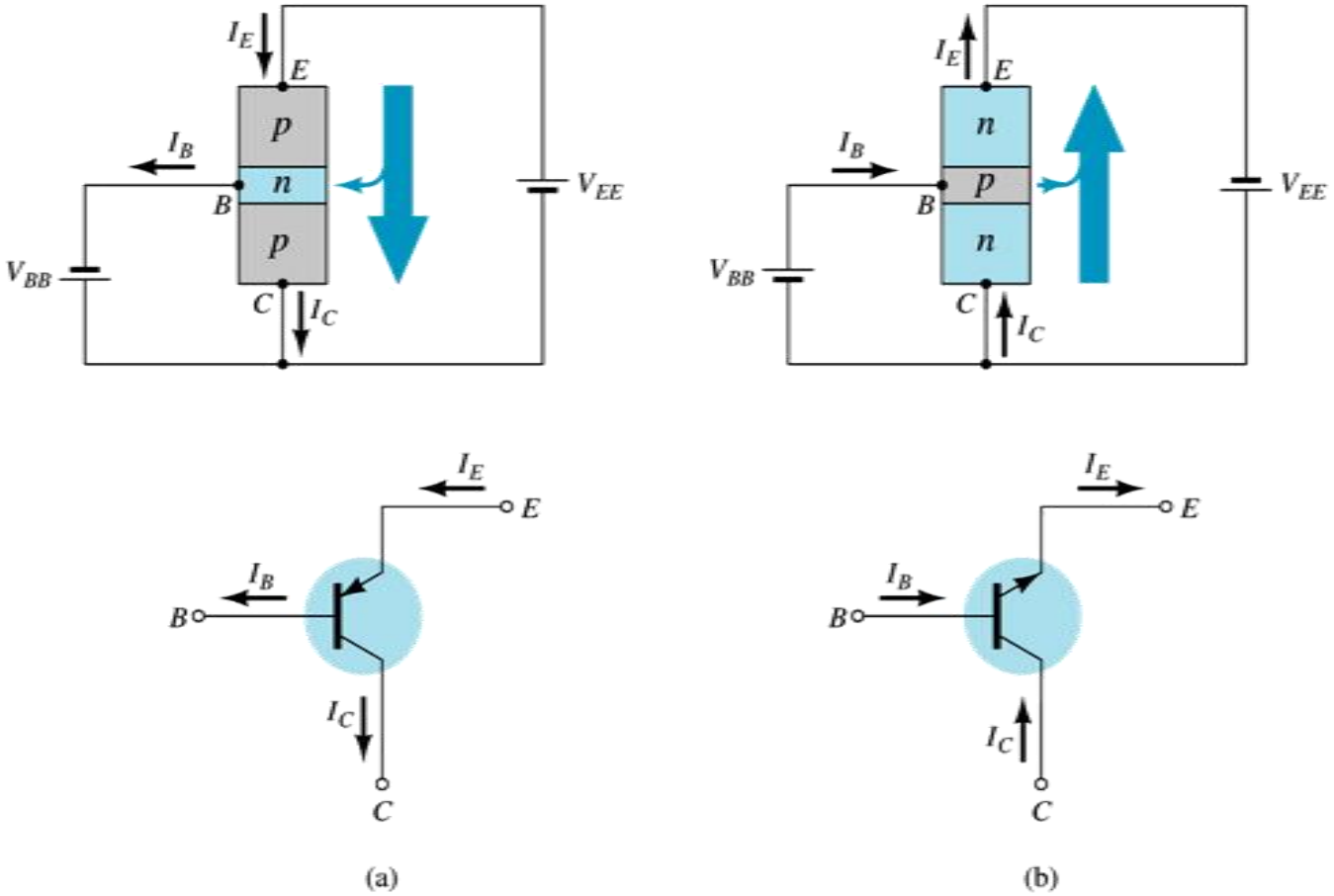
# Common – Collector Configuration

- In this configuration, the base terminal of the transistor serves as the input, the emitter terminal is the output and the collector terminal is common for both input and output.
- Hence, it is named as common collector configuration. The input is applied between the base and collector while the output is taken from the emitter and collector.

# Common – Collector Configuration

- Also called emitter-follower (EF).
- It is called common-collector configuration since both the signal source and the load share the collector terminal as a common connection point.
- The output voltage is obtained at emitter terminal.
- The input characteristic of common-collector configuration is similar with common-emitter configuration.
- Common-collector circuit configuration is provided with the load resistor connected from emitter to ground.
- It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

# Common – Collector Configuration




**Notation and symbols used with the common-collector configuration:**
**(a) pnp transistor ; (b) npn transistor.**

# Common – Collector Configuration

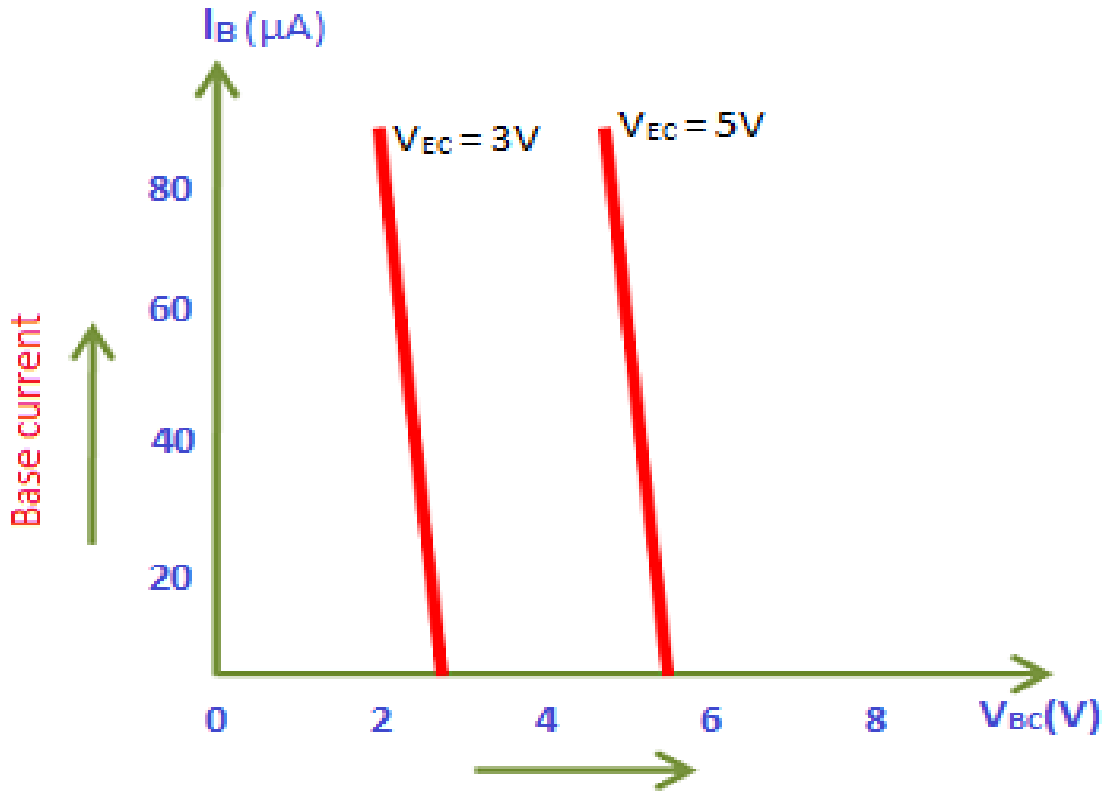
- **Input characteristics**

- The input characteristics describe the relationship between input current or base current ($I_B$) and input voltage or base-collector voltage ($V_{BC}$).
- To determine the input characteristics, the output voltage $V_{EC}$ is kept constant at 3V and the input voltage $V_{BC}$ is increased from zero volts to different voltage levels. For each level of input voltage $V_{BC,}$ the corresponding input current $I_B$ is noted. A curve is then drawn between input current $I_B$ and input voltage $V_{BC}$ at constant output voltage $V_{EC}$(3V).

Next, the output voltage $V_{EC}$ is increased from 3V to different voltage level, say for example 5V and then kept constant at 5V. While increasing the output voltage $V_{EC}$, the input voltage $V_{BC}$ is kept constant at zero volts.

This process is repeated for higher fixed values of output voltage ($V_{EC}$).

# Common – Collector Configuration



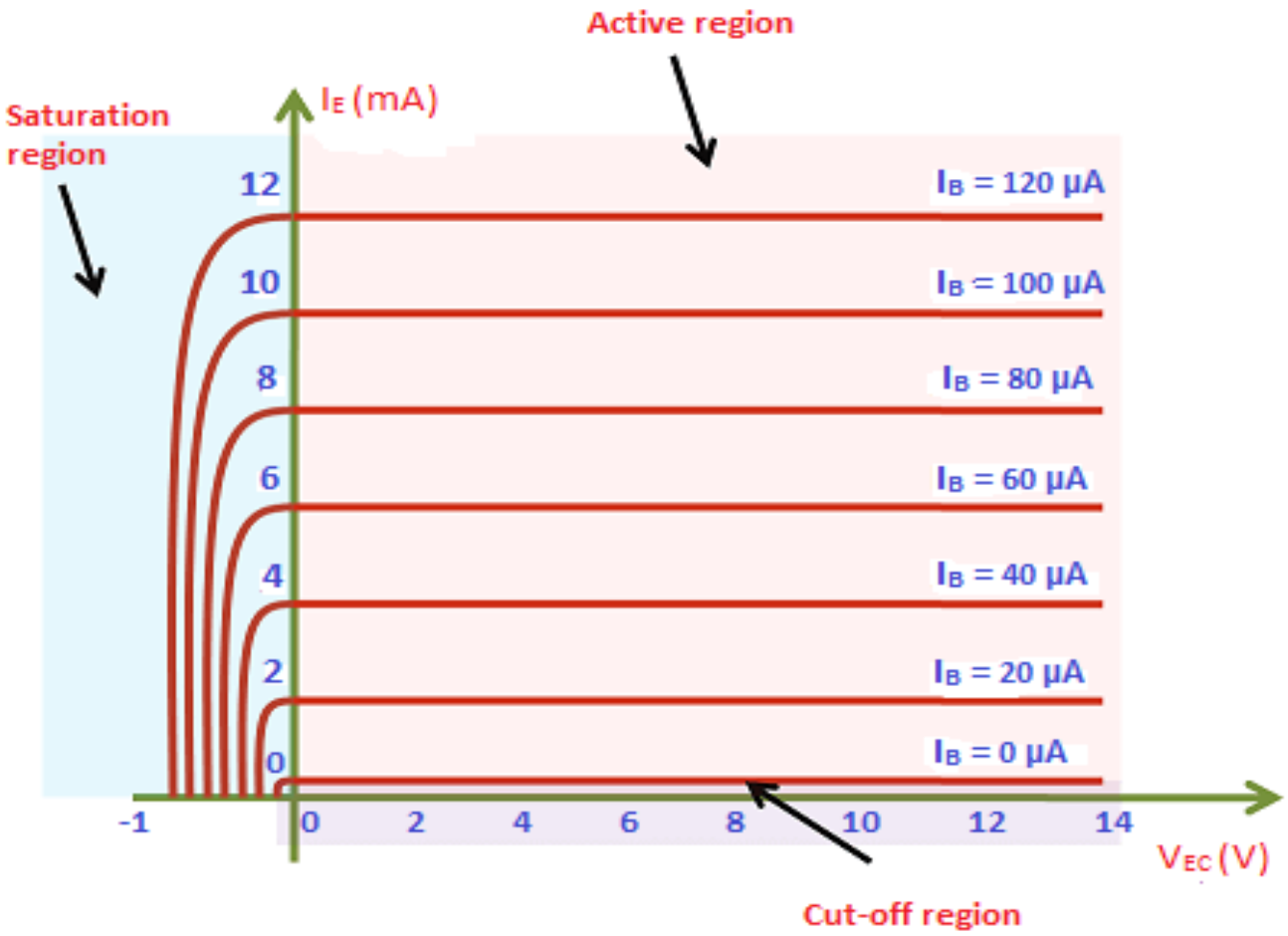

**Input characteristics**

# Common – Collector Configuration

- **Output characteristics**
- **The output characteristics describe the relationship between output current or emitter current ($I_E$) and output voltage or emitter-collector voltage ($V_{EC}$).**
- **To determine the output characteristics, the input current $I_B$ is kept constant at zero micro amperes and the output voltage $V_{EC}$ is increased from zero volts to different voltage levels. For each level of output voltage $V_{EC}$, the corresponding output current $I_E$ is noted. A curve is then drawn between output current $I_E$ and output voltage $V_{EC}$ at constant input current $I_B$ (0 µA).**

- **In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So the transistor will be in the cutoff region. If the base current is slightly increased then the output current or emitter current also increases. So the transistor falls into the active region. If the base current is heavily increased then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region.**

# Common – Collector Configuration




**Output characteristics**

# Common – Collector Configuration

## Transistor parameters

- **Dynamic input resistance ($r_i$)**

**Dynamic input resistance is defined as the ratio of change in input voltage or base voltage ($V_{BC}$) to the corresponding change in input current or base current ($I_B$), with the output voltage or emitter voltage ($V_{EC}$) kept at constant.**

**The input resistance of common collector amplifier is high.**

$$r_i = \frac{\Delta V_{BC}}{\Delta I_B}, \qquad V_{EC} = \text{constant}$$

# Common – Collector Configuration

- **Dynamic output resistance ($r_o$)**

  **Dynamic output resistance is defined as the ratio of change in output voltage or emitter voltage ($V_{EC}$) to the corresponding change in output current or emitter current ($I_E$), with the input current or base current ($I_B$) kept at constant. The output resistance of common collector amplifier is low.**

$$r_o = \frac{\Delta V_{EC}}{\Delta I_E}, \qquad I_B = \text{constant}$$

- **Current amplification factor (γ)**

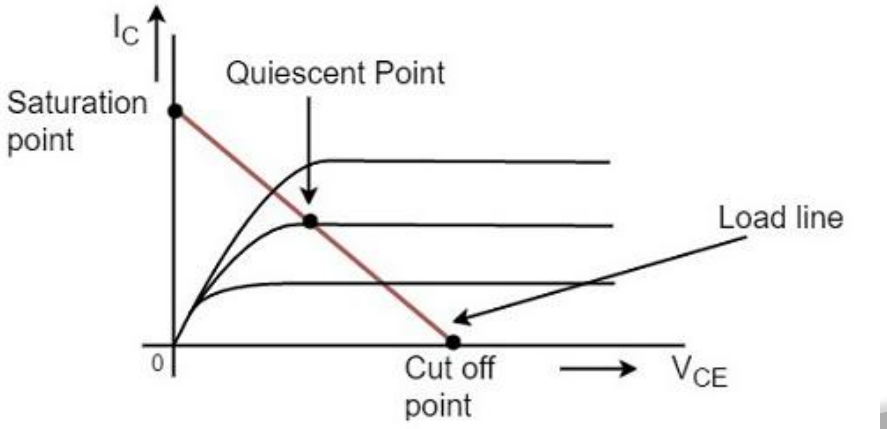
  **The current amplification factor is defined as the ratio of change in output current or emitter current $I_E$ to the change in input current or base current $I_B$. It is expressed by γ. The current gain of a common collector amplifier is high.**

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

# Q point or quiescent or operating point of BJT

# Q point or quiescent or operating point of BJT

- Q-point is an acronym for quiescent point. Q-point is the operating point of the transistor ($I_{CQ}$,$V_{CEQ}$) at which it is biased.
- The concept of Q-point is used when transistor act as an amplifying device and hence is operated in active region of input output characteristics.
- To operate the BJT at a point it is necessary to provide voltages and currents through external sources.
- When a line is drawn joining the saturation and cut off points, such a line can be called as Load line. This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.



# Q point or quiescent or operating point of BJT

- **Importance of q point in transistor**
- **Normally whatever signals we want to amplify will be of the order milli volts or less.**
- **If we directly input these signals to the amplifier they will not get amplified as transistor needs voltages greater than cut in voltages for it to be in active region.**
- **Only in active region of operation transistor acts as amplifier. So we can establish appropriate DC voltages and currents through BJT by external sources so that BJT operates in active region and superimpose the AC signals to be amplified.**
- **The DC voltage and current are so chosen that the transistor remains in active region for entire AC signal excursion. All the input AC signals variations happen around Q-point.**

# DC and AC load line

# DC load line

- The dc load line is the locus of $I_C$ and $V_{CE}$ at which BJT remains in active region i.e. it represents all the possible combinations of $I_C$ and $V_{CE}$ for a given amplifier.

**Procedure to draw DC load line**

- To draw DC load line of a transistor we need to find the saturation current and cutoff voltage.
- Saturation point : The saturation current is the maximum possible current through the transistor and occurs at the point where the voltage across the collector is minimum. To find the saturation point equate the collector voltage to zero.
- Cutoff point : The cutoff voltage is the maximum possible voltage across the collector and occurs at zero collector current. To find the cutoff point equate the collector current to zero.

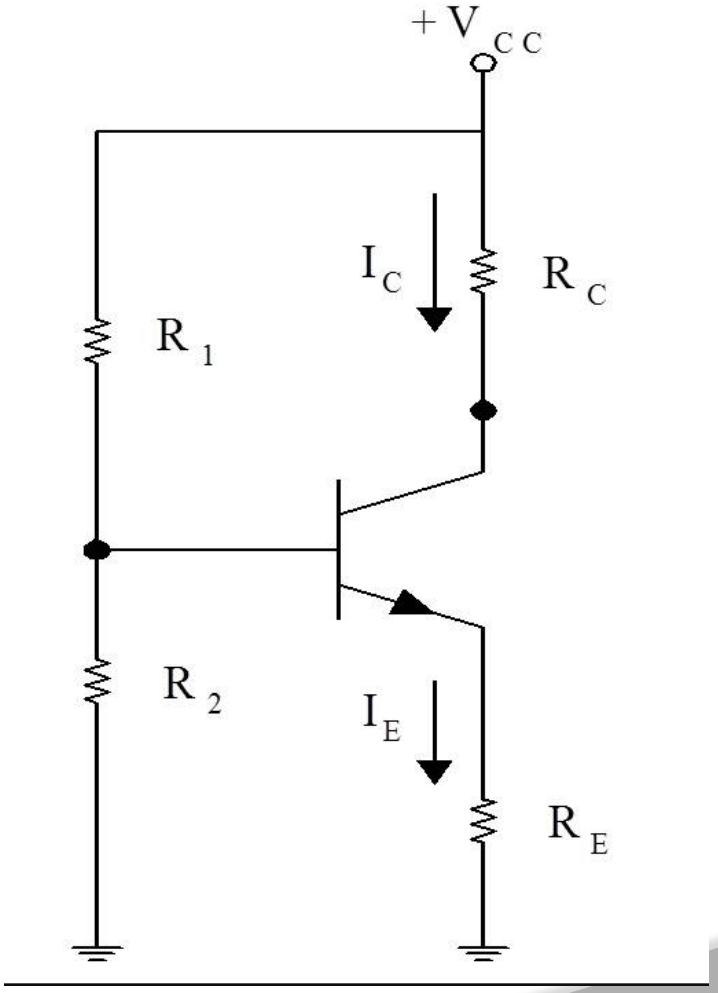
# DC load line

From the DC equivalent circuit by applying Kirchoff's voltage Law in collector loop in

$$V_{ce} = V_{cc} - R_c * I_c \quad \text{(Equation 1)}$$

In equation 1 equating $I_c$ to zero the cutoff point is ($V_{cc}$, 0).

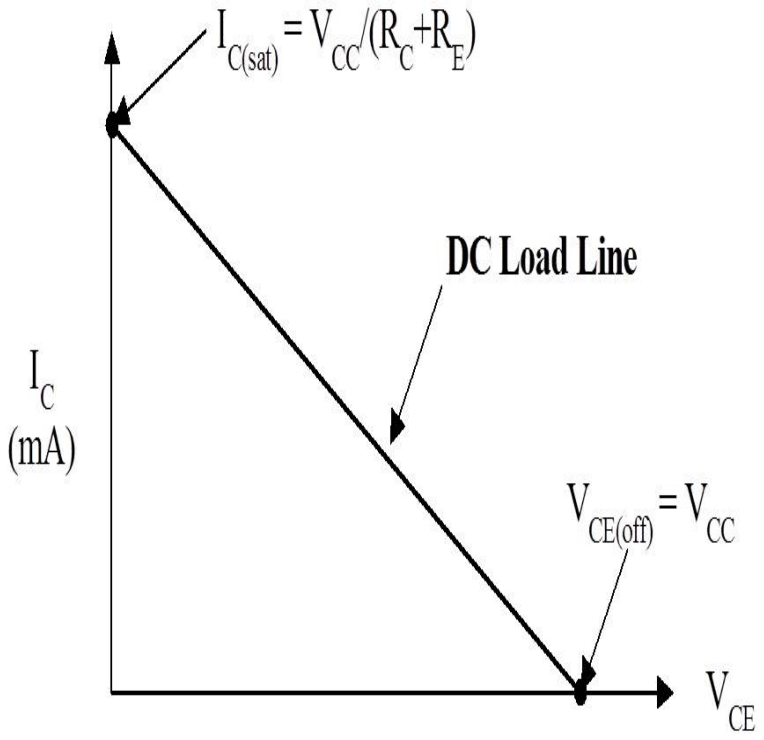
In equation 1 equating $V_{ce}$ to zero the cutoff point is (0, $V_{cc}/R_c$).




DC equivalent circuit of CE amplifier

# DC load line

**($V_{cc}$, 0) is cut off point where transistor enters in to cut off region from active region and (0, $V_{cc}/R_c$) is saturation point where the transistor enters saturation region.**



# AC load line

- **DC load line analysis gives the variation of collector currents and voltage for static situation of Zero AC voltage.**
- **The ac load line tells you the maximum possible output voltage swing for a given common-emitter amplifier i.e. the ac load line will tell you the maximum possible peak-to-peak output voltage $V_{ce(cut\ off)}$ from a given amplifier.**
- **For AC input signal frequencies the biasing capacitors are chosen such that they acts as short circuits and as open circuits for DC voltages.**

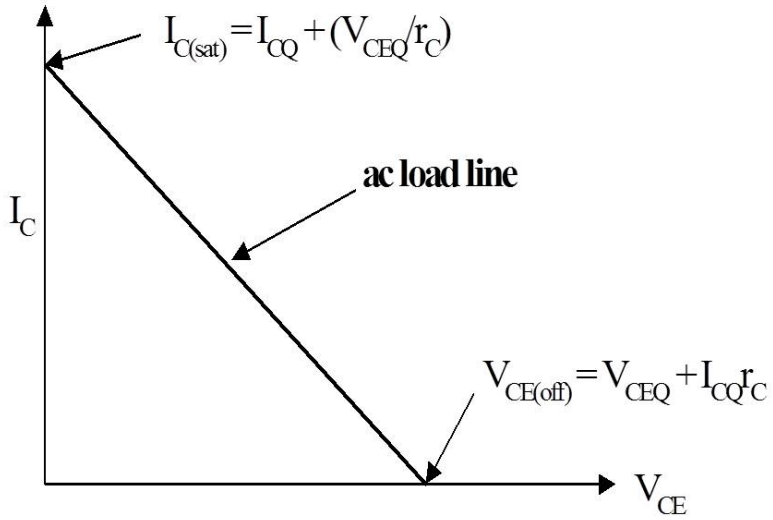
# AC load line

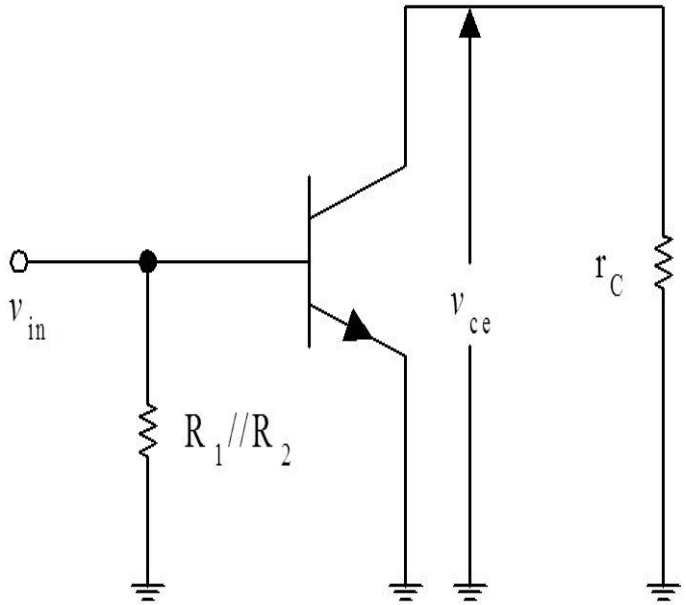
**The current IC at the saturation point is**

**IC(sat)=ICQ+(VCEQ/rc)**

**The voltage $V_{CE}$ at the cutoff point is**

**VCE(off)=VCEQ+ICQ*rC**

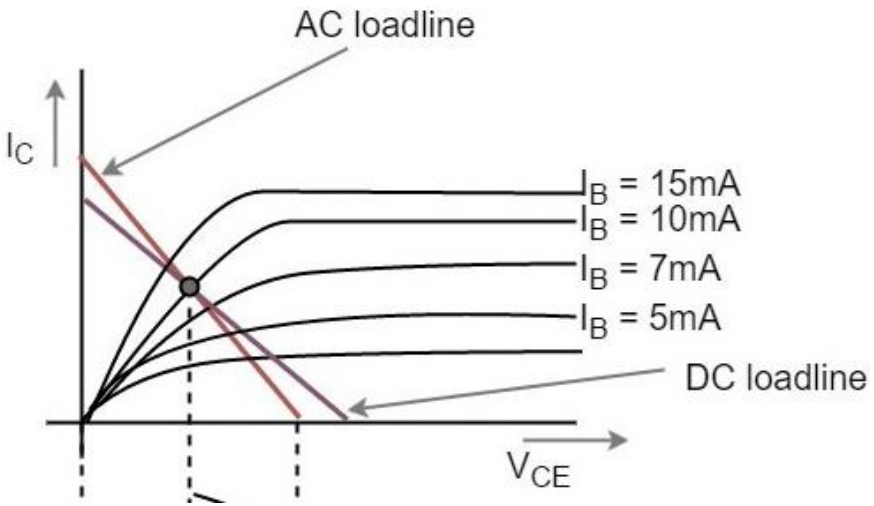



**AC equivalent circuit of CE amplifier**

# DC & AC load line

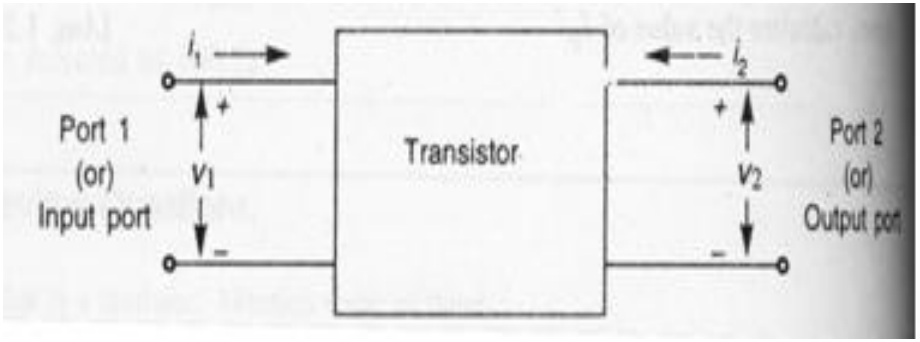
- **When AC and DC Load lines are represented in a graph, it can be understood that they are not identical. Both of these lines intersect at the Q-point or quiescent point.**



# Transistor Hybrid parameter model

# Transistor Hybrid parameter model

- A transistor can be treated as a two part network. The terminal behavior of any two part network can be specified by the terminal voltages $V_1$ & $V_2$ at parts 1 & 2 respectively and current $i_1$ and $i_2$, entering parts 1 & 2, respectively, as shown in figure.




If the input current $i_1$ and output Voltage $V_2$ are takes as independent variables, the input voltage $V_1$ and output current $i_2$ can be written as

$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$
$$i_2 = h_{21}\, i_1 + h_{22}\, V_2$$

# Transistor Hybrid parameter model

The four hybrid parameters $h_{11}$, $h_{12}$, $h_{21}$ and $h_{22}$ are defined as follows.

- $h_{11} = [V_1 / i_1]$ with $V_2 = 0$
  = Input Impedance with output voltage short circuited.

- $h_{22} = [i_2 / V_2]$ with $i_1 = 0$
  = Output admittance with input current open circuited.

- $h_{12} = [V_1 / V_2]$ with $i_1 = 0$
  = reverse voltage transfer ratio with input current open circuited.

- $h_{21} = [i_2 / i_1]$ with $V_2 = 0$
  = Forward current gain with output voltage short circuited.

# Transistor Hybrid parameter model

- **The dimensions of h – parameters are as follows:**

**$h_{11}$ - Ω**

**$h_{22}$ – mhos**

**h12, h21 – dimension less.**

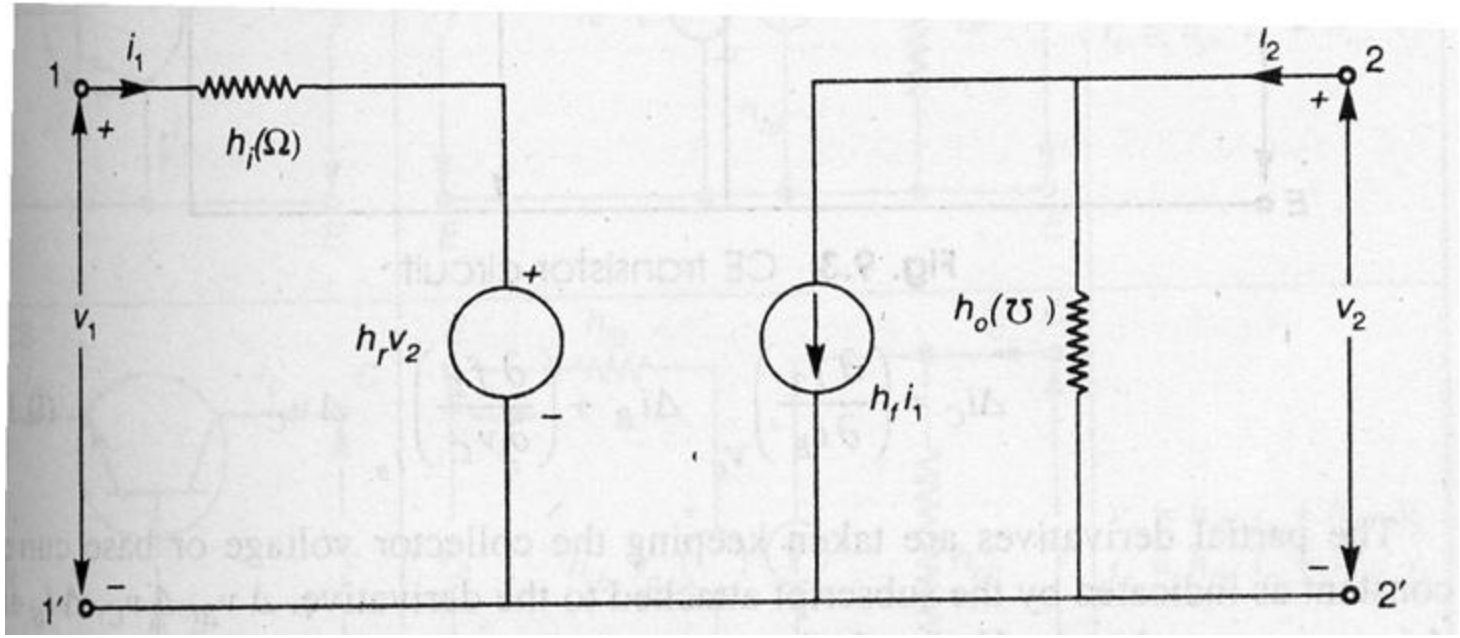
**→ as the dimensions are not alike, (ie) they are hybrid in nature, and these parameters are called as hybrid parameters.**

**i= 11 = input ; o= 22 = output ;**

**f = 21 = forward transfer ; r = 12 = Reverse transfer.**

# Transistor Hybrid parameter model

**The Hybrid Model for Two-port Network**

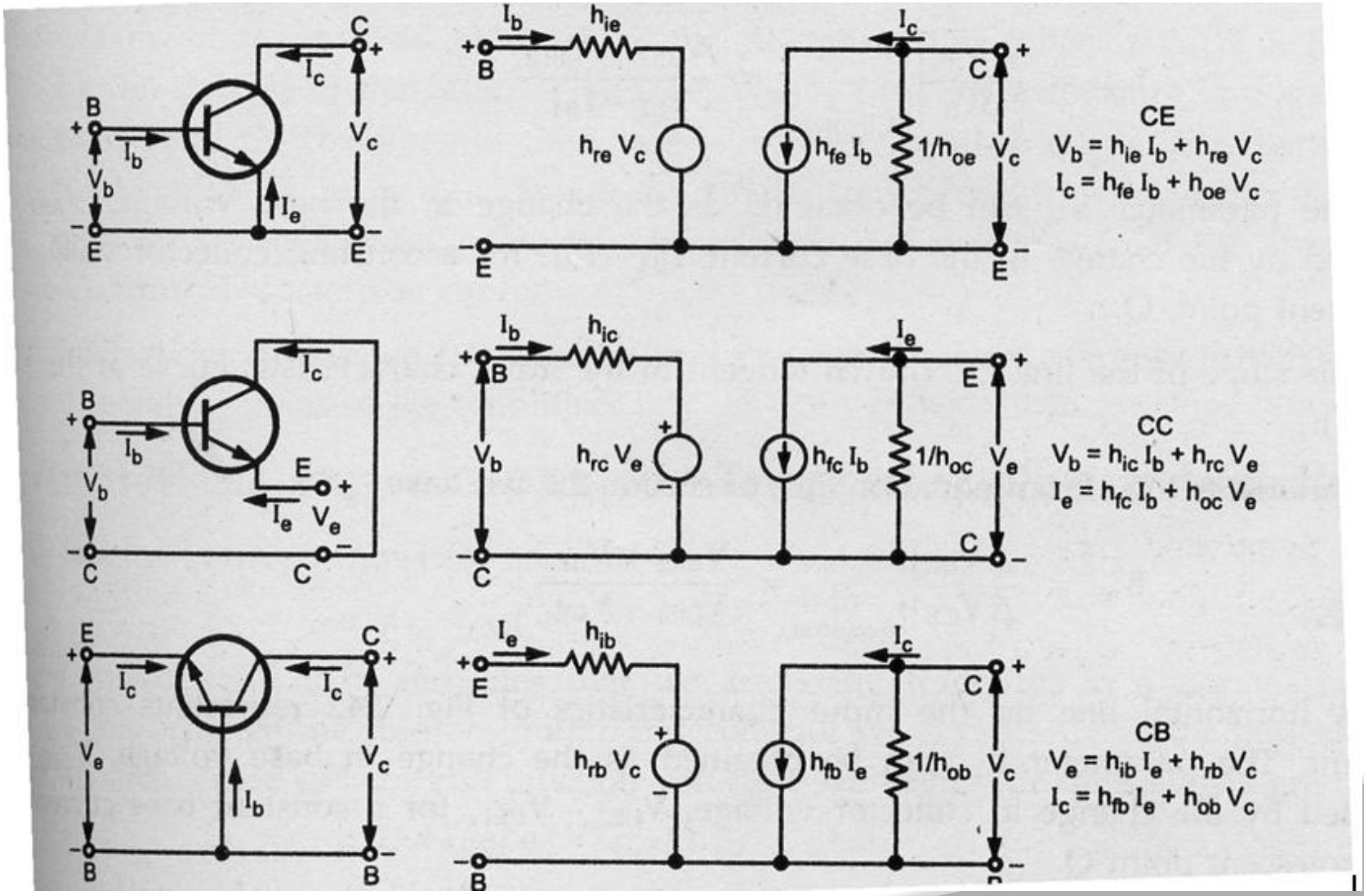


# Transistor Hybrid parameter model

**Use of h – parameters to describe a transistor has the following advantages.**

- **h – Parameters are real numbers up to radio frequencies.**
- **They are easy to measure**
- **They can be determined from the transistor static characteristics curves.**
- **They are convenient to use in circuit analysis and design.**
- **Easily convert able from one configuration to other.**
- **Readily supplied by manufactories.**

# Transistor Hybrid parameter model



# Determination of h-parameters from transistor characteristics

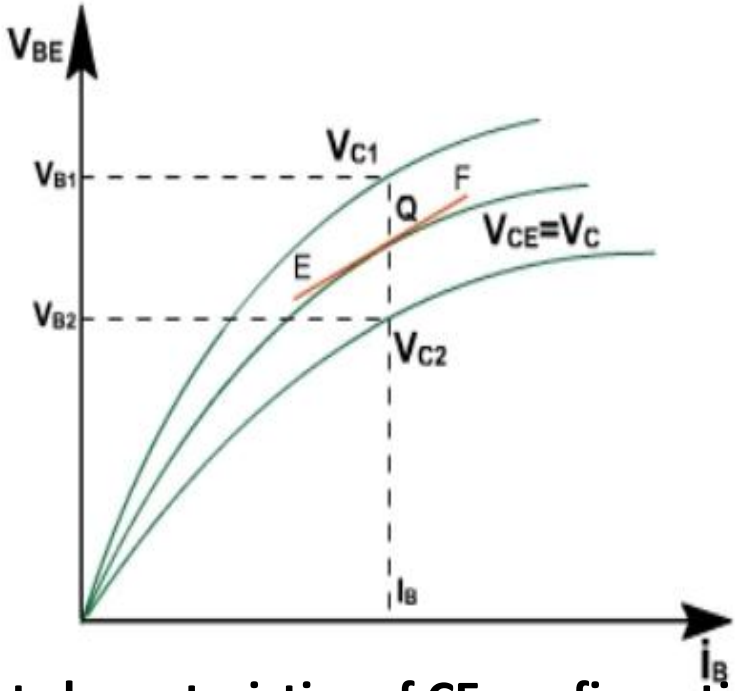
# Determination of h-parameters from transistor characteristics

- To determine the four h-parameters of transistor amplifier, input and output characteristic are used.
- Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter.
- The output characteristic depicts the relationship between output voltage and output current with input current as parameter.

# Determination of h-parameters from transistor characteristics

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

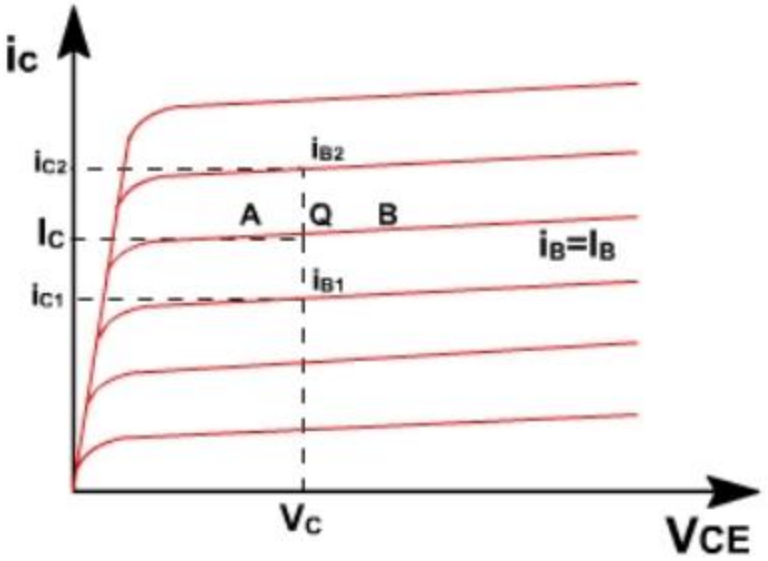



**input characteristics of CE configuration**

# Determination of h-parameters from transistor characteristics

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$




**output characteristics of CE configuration**

# Conversion of h-parameters

# Value of h-parameters of a Typical Transistor

| S.N. | Parameter | CE | CB | CC |
|---|---|---|---|---|
| 1. | $h_i$ | 1100Ω | 22Ω | 1100Ω |
| 2. | $h_r$ | $2.5\times10^{-4}$ | $3\times10^{-4}$ | 1 |
| 3. | $h_f$ | 50 | -0.98 | -51 |
| 4. | $h_0$ | $25\mu S$ | $0.5\mu S$ | $25\mu S$ |
| 5. | $1/h_0$ | 40 kΩ | 2 MΩ | 40 kΩ |

# Approximate Conversion Formulas for h-parameter

| | |
|---|---|
| $h_{ic} = h_{ie}$ | $h_{ib} = \dfrac{h_{ie}}{1 + h_{fe}}$ |
| $h_{fc} = (1 + h_{fe})$ | $h_{fb} = -\dfrac{h_{fe}}{1 + h_{fe}}$ |
| $h_{rc} = 1$ | $h_{rb} = \dfrac{h_{ie} \times h_{oe}}{1 + h_{fe}} - h_{re}$ |
| $h_{oc} = h_{oe}$ | $h_{ob} = \dfrac{h_{oe}}{1 + h_{fe}}$ |

# PROBLEMS

# PROBLEMS

1. **The reverse leakage current of the transistor when in CB configuration is 0.3μA while it is 16μA when the same transistor is connected in CE configuration. Determine α, β and γ.**

2. **The common base d.c current gain of transistor is 0.967. If the emitter current is 10mA, what is the value of the base current?**

3. **(a)A transistor has α=0.975. What is the value of β and γ.**

   **(b) If β=200, What is the value of α and γ.**

# PROBLEMS

4. A transistor has β=150. Calculate the approximate collector and base currents if the emitter current is 10mA.

5. A transistor has IB=105 μA and IC=2.05mA. Find

   (a)β of the transistor

   (b)α of the transistor

   (c)emitter current IE

   (d)Now, if IB changes by 27 μA and IC changes by 0.65mA,find the new value of β.

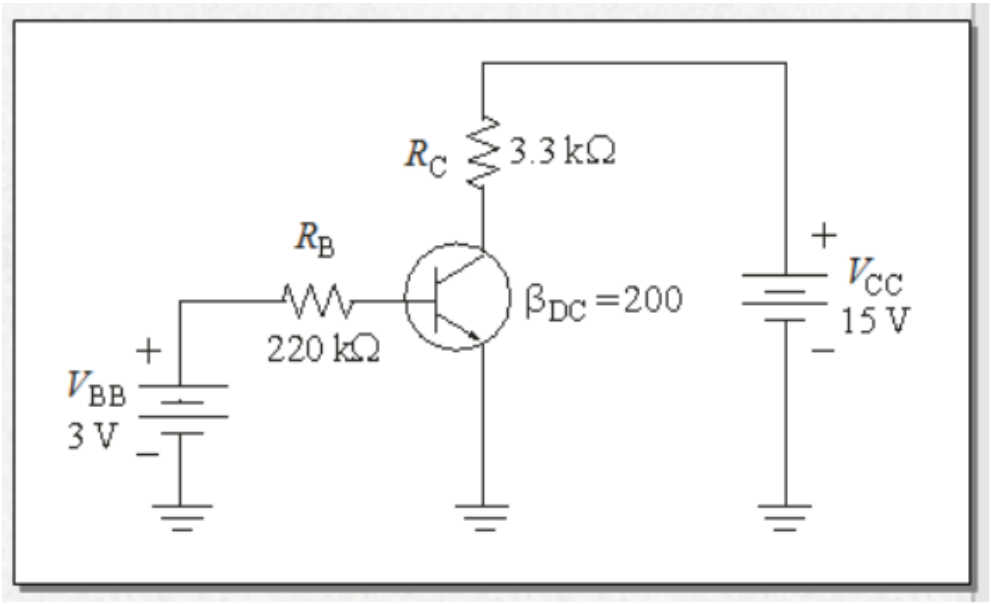
# PROBLEMS

6. A certain transistor has α=0.98,IC0= 5 μA and IB=100 μA. Find the values of collector and emitter currents.

7. A certain transistor has α of 0.98 and a collector leakage current IC0 of 1 μA. Calculate the collector and base currents, when IE= 1 mA.

# PROBLEMS

1. **What is the saturation current and the cut-off for this circuit? Assume VCE=0.2V in saturation.**
2. **Is the transistor saturated?**



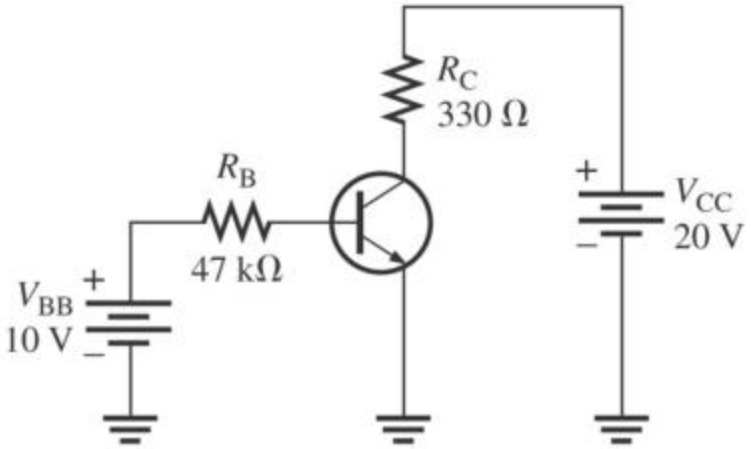

$$I_{BQ} = \frac{V_{BB} - 0.7\,\text{V}}{R_B}$$

$$I_{CQ} = \beta_{DC} I_{BQ}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

# PROBLEMS

**Determine Q point and draw the dc load line. Assume βDC = 200.**




# UNIT-III
# TRANSISTOR BIASING AND STABILIZATION

# Outline

- Bias Stability
- Fixed Bias
- Collector to Base bias
- Self Bias
- Bias Compensation using Diodes and Transistors
- Analysis of CE, CC, CB Amplifiers
- Analysis of CE Amplifier with emitter resistance
- low frequency response of BJT Amplifiers
- effect of coupling and bypass capacitors on CE Amplifier
- Problems

# Bias Stability

# Transistor Biasing

**Biasing**

**The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as Transistor Biasing. The circuit which provides transistor biasing is called as Biasing Circuit.**

**Need for DC biasing**

- **If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.**
- **The input voltage should exceed cut-in voltage for the transistor to be ON.**
- **The BJT should be in the active region, to be operated as an amplifier.**

# Factors affecting the operating point

- The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.
- As temperature increases, the values of $I_{CE}$, β, $V_{BE}$ gets affected.
- $I_{CBO}$ gets doubled (for every $10^o$ rise)
- $V_{BE}$ decreases by 2.5mv (for every $1^o$ rise)
- So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

# Bias Stability

- A transistor can work as amplifier, only if the dc/ac voltages and currents in the circuit are suitably fixed. The operating point or bias point or quiescent point(or simply Q-point) is the voltage or current which, when applied to a device, causes it to operate in a certain desired fashion. Need for bias stabilization.

**Need for BIAS STABILIZATION**

- After fixing the operating point suitably, it should remains there only. But there are two reasons for the operating point to shift.
- The transistor parameters such as VBE & β changes from device to device
- Transistor parameters are also temperature dependent. Since the collector current is $I_C = \beta I_B + (1+\beta) I_{CO}$ (β, IB and Ico are temperature dependent)
- β of a transistor is strongly dependent on temperature. As temp. increases, β increases

# Stabilization Factors

**Stability Factor**

- **It is understood that $I_C$ should be kept constant in spite of variations of $I_{CBO}$or $I_{CO}$. The extent to which a biasing circuit is successful in maintaining this is measured by Stability factor. It denoted by S.**

- **By definition, the rate of change of collector current $I_C$ with respect to the collector leakage current $I_{CO}$ at constant β and $I_B$ is called Stability factor.**

- **S=dIc/dIco at constant $I_B$ and β**

- **Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. S=1 is the ideal value.**

# Stabilization Factor(contd.)

- **The general expression of stability factor for a CE configuration can be obtained as under.**

$$I_c = \beta I_B + (1+\beta) I_{c0}$$

- **Differentiating above expression with respect to $I_C$, we get**

$$S = \frac{1+\beta}{1-\beta \dfrac{dIB}{dIc}}$$

- **Hence the stability factor S depends on β, $I_B$ and $I_C$.**

# Stabilization Factor(contd.)

**Stability factor S' and S":**

The Stability factor S' is defined as the rate of change of $I_C$ with $V_BE$, keeping $I_CO$ and β constant.

$$S' = \frac{\partial I_C}{\partial V_BE} = \frac{\Delta I_C}{\Delta V_BE}$$

The stability factor S" is defined as the rate of change of $I_C$ with respect to β, keeping $I_CO$ and $V_BE$ constant.

$$S' = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\Delta \beta}$$

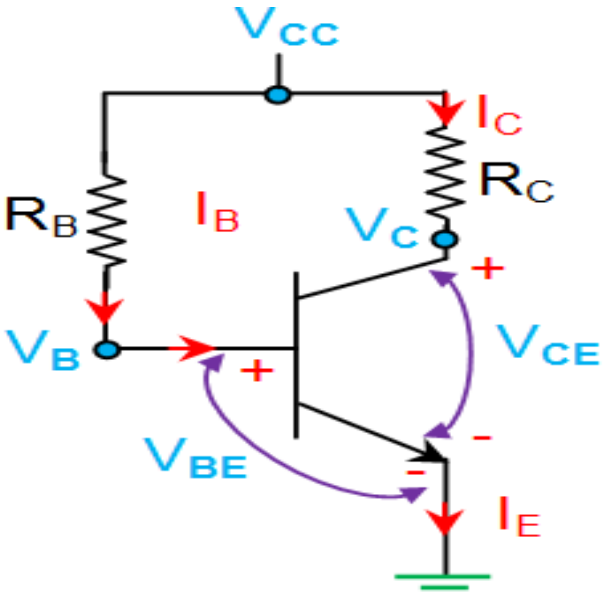
The small value of stability factor indicates good bias stability whereas large value of stability factor indicates poor bias stability. Ideal value of stability factor is zero.

# Fixed Bias

# Fixed Base Bias or Fixed Resistance Bias

- The biasing circuit shown by below Figure has a base resistor $R_B$ connected between the base and the $V_{CC}$.
- Here the base-emitter junction of the transistor is forward biased by the voltage drop across $R_B$ which is the result of $I_B$ flowing through it. From the figure, the mathematical expression for $I_B$ is obtained as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$




Fixed Base Bias Circuit

$V_C = V_{CC} - (I_C R_C)$

$V_{CE} = V_C - V_E$

$V_E = 0v$

$V_B = V_{BE}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$I_C = \beta_{(DC)} I_B$

$I_E = (I_C + I_B) \cong I_C$

# Stability in fixed bias

- Take general equation for stability factor.

$$S = \frac{1+\beta}{1-\beta\dfrac{dIB}{dIc}}$$

From equation

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$S = 1+\beta$$

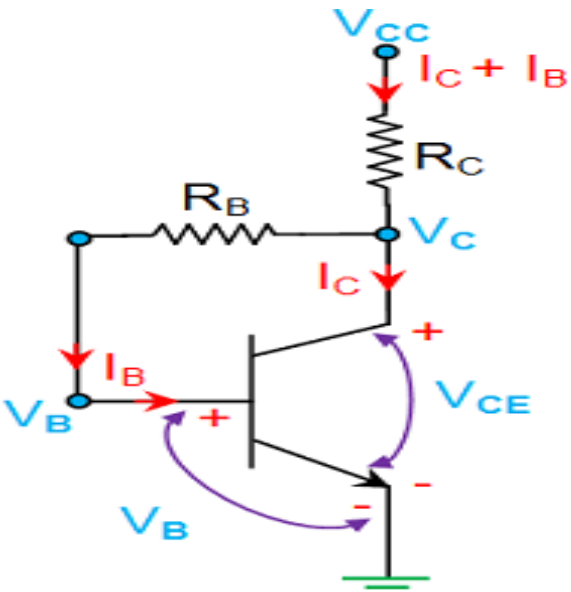
# Collector to Base bias

# Collector Feedback Bias

- In this circuit , the base resistor $R_B$ is connected across the collector and the base terminals of the transistor. This means that the base voltage, $V_B$ and the collector voltage, $V_C$ are inter-dependent due to the fact that

$$V_B = V_C - I_B R_B$$

$$V_C = V_{CC} - (I_B + I_C) R_C$$




Collector Feedback Bias Circuit

# Collector Feedback Bias

- From these equations, it is seen that an increase in $I_C$ decreases $V_C$ which results in a reduced $I_B$, automatically reducing $I_C$. This indicates that, for this type of biasing network, the Q-point (operating point) remains fixed irrespective of the variations in the load current causing the transistor to always be in its active region regardless of β value.
- Further this circuit is also referred to as self-biasing negative feedback circuit as the feedback is from output to input via $R_B$. This kind of relatively simple bias has a stability factor which is less than (β+1), which results in a better stability when compared to fixed bias. However the action of reducing the collector current by base current leads to a reduced amplifier gain. Here,
- other voltages and currents are expressed as

$$V_B = V_{BE}$$
$$I_C = \beta I_B$$
$$I_E \approx I_C$$

# Stability factor for collector-to-base bias.

**Take general equation for stability factor**

$$S = \frac{1+\beta}{1-\beta\dfrac{dIB}{dIc}}$$

**In the above equation only variable is $dI_B/dIc$. Let us find an equation for it from the above circuit.**

From the circuit, $Vcc = (Ic + I_B)Rc + I_B R_B + V_{BE}$

Therefore, $I_B = \dfrac{Vcc - V_{BE} - IcRc}{R_B + Rc}$ differentiate with respect to Ic.(Vcc and $V_{BE}$ are constants)

$$\frac{dI_B}{dIc} = \frac{-Rc}{R_B + Rc}$$ substitute this in equation for stability factor S.

$$S = \frac{1+\beta}{1+\beta\dfrac{Rc}{R_B+Rc}}$$ ---(2) This is the equation for stability factor for collector-to-base bias.

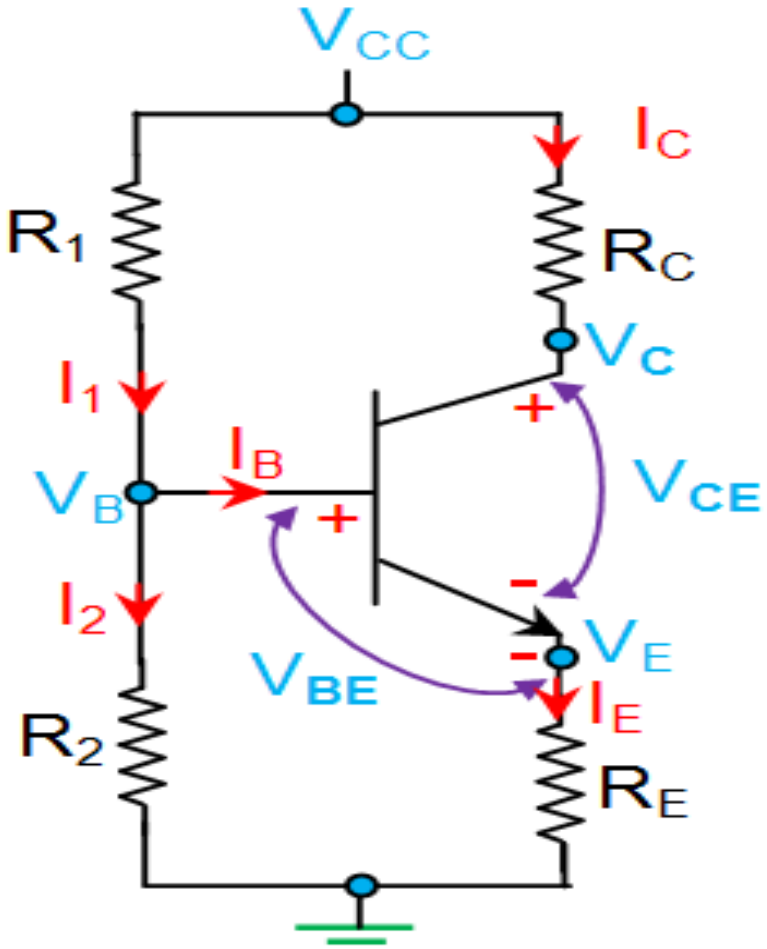
# Self Bias

# Voltage Divider Bias

- A simple circuit used to establish a stable operating point is the self-biasing configuration. The self bias, also called as emitter bias that can be used for low collector resistance.
- The current in the emitter resistor causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased.
- This type of biasing network employs a voltage divider formed by the resistors $R_1$ and $R_2$ to bias the transistor. This means that here the voltage developed across $R_2$ will be the base voltage of the transistor which forward biases its base-emitter junction.

- In general, the current through $R_2$ will be fixed to be 10 times required base current, $I_B$ (i.e. $I_2 = 10I_B$). This is done to avoid its effect on the voltage divider current or on the changes in β.

# Voltage Divider Bias




Voltage Divider Bias Circuit

# Voltage Divider Bias

**To determine stability factor, S Applying Thevenin's Theorem to the circuit**

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} and R_B = \frac{R_1 R_2}{R_1 + R_2}$$

**The loop equation around the base circuit can be written as**

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

**Differentiating this equation w.r.t Ic, we get**

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

$$S = \frac{1+\beta}{1+\beta \dfrac{R_E}{R_E + R_B}}$$

# Voltage Divider Bias

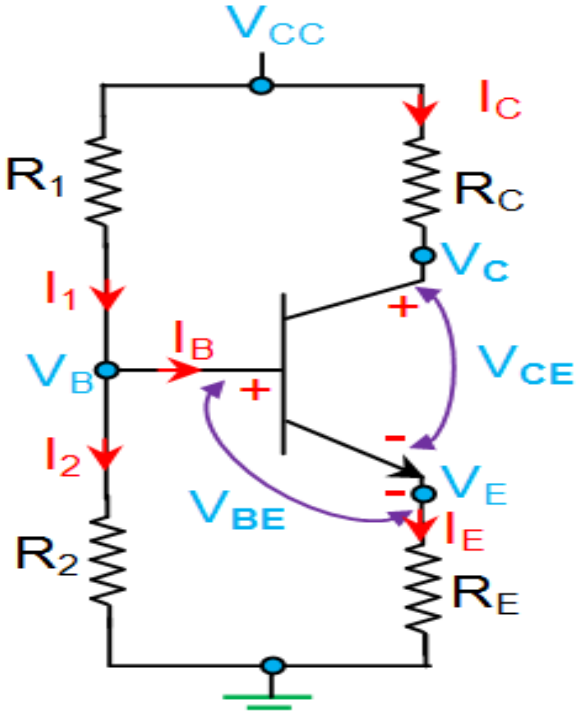
- In this kind of biasing, $I_C$ is resistant to the changes in both β as well as $V_{BE}$ which results in a stability factor of 1 (theoretically), the maximum possible thermal stability.

- This is because, as $I_C$ increases due to a rise in temperature, IE also increases causing an increase in the emitter voltage $V_E$ which in turn reduces the base-emitter voltage, $V_{BE}$.

- This results in the decrease of base current $I_B$ which restores $I_C$ to its original value. The higher stability offered by this biasing circuit makes it to be most widely used in spite of providing a decreased amplifier gain due to the presence of $R_E$

# Example

In a CE ge transistor amplifier circuit, the bias is provided by bias, i.e. emitter resistor and potential divider arrangement. The various parameters are Vcc=16V, Rc=3K,Re=2K,R1=56K,R2= 20K and α=0.985. Determine (a) the coordinates of the operating point and (b) the stability factor S.




Voltage Divider Bias Circuit

**Solution: For a ge transistor Vbe=0.3v, as α=0.985**

**(a) To find coordinates of the operating point**

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$$

$$R_B = \frac{R_2}{R_1 + R_2}.V_{cc} = \frac{20X10^3}{76X10^3}.16 = 4.21V$$

$$R_B = \frac{R_2}{R_1 + R_2} = \frac{20X10^3}{76X10^3} = 14.737K\Omega$$

**The loop equation around the base circuit is**

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$3.91 = I_C [0.223 + 2.03].10^3$$

$$I_c = 1.73mA$$

$$V_{CE} = V_{CC} - I_c R_c - I_E R_E = 7.35V$$

**(b) To find the stability factor S,**

$$S = (1+\beta).\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}$$

$$S = (1+66).\frac{1+\frac{14.737}{2}}{1+66+\frac{14.737}{2}}$$

# Bias Compensation using Diodes and Transistors

# Bias Compensation techniques

**Diode Compensation for Instability:**

- **These are the circuits, as the gain of the amplifier is a very important consideration, some compensation techniques are used to maintain excellent bias and thermal stabilization.**

- **These are the circuits that implement compensation techniques using diodes to deal with biasing instability. The stabilization techniques refer to the use of resistive biasing circuits which permit $I_B$ to vary so as to keep $I_C$ relatively constant.**

**There are two types of diode compensation methods. They are –**

- **Diode compensation for instability due to $V_{BE}$ variation**

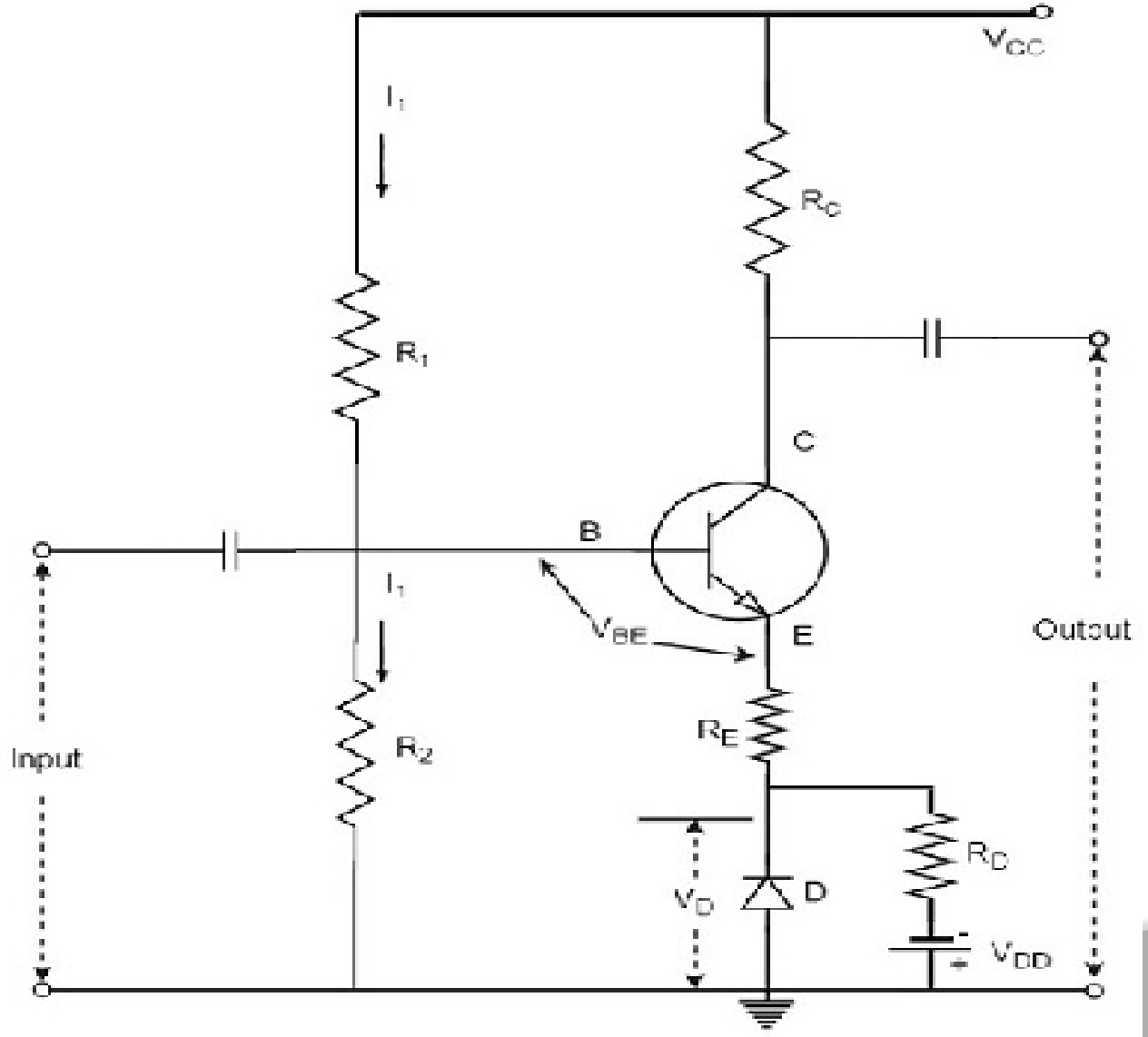
- **Diode compensation for instability due to $I_{CO}$ variation**

# Bias Compensation techniques

**Diode Compensation for Instability due to $V_{BE}$ Variation:**

- **In a Silicon transistor, the changes in the value of $V_{BE}$ results in the changes in $I_C$. A diode can be employed in the emitter circuit in order to compensate the variations in $V_{BE}$ or $I_{CO}$.**
- **As the diode and transistor used are of same material, the voltage $V_D$ across the diode has same temperature coefficient as $V_{BE}$ of the transistor.**
- **The diode D is forward biased by the source VDD and the resistor RD. The variation in VBE with temperature is same as the variation in VD with temperature, hence the quantity (VBE – VD) remains constant.**
- **So the current IC remains constant in spite of the variation in VBE.**

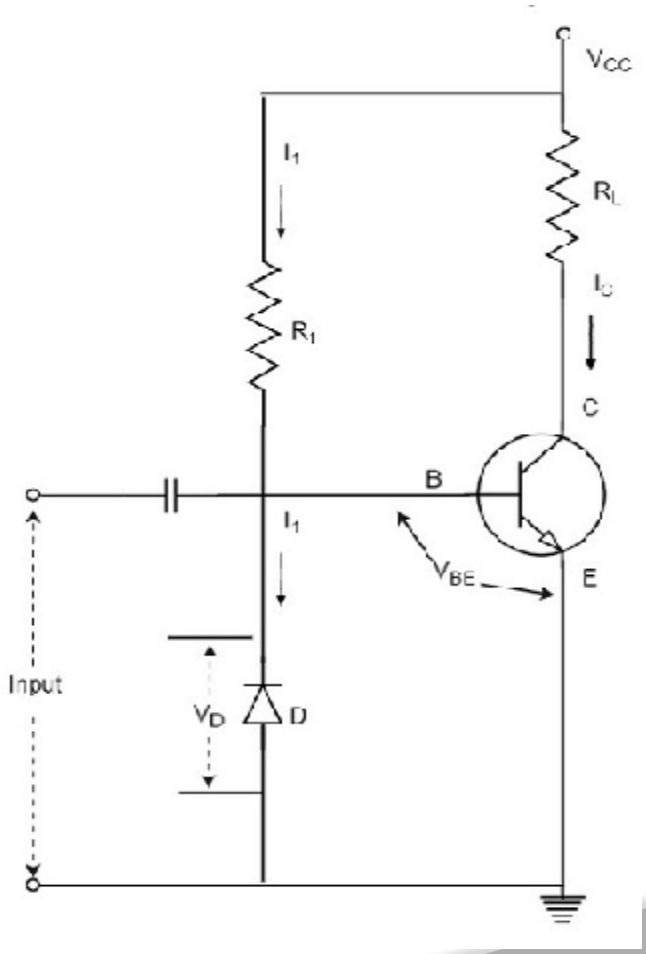
# Bias Compensation techniques



# Bias Compensation techniques(contd.)

**Diode Compensation for Instability due to ICO Variation**

**The figure shows the circuit diagram of a transistor amplifier with diode D used for compensation of variation in ICO.**



# Bias Compensation techniques

So, the reverse saturation current $I_O$ of the diode will increase with temperature at the same rate as the transistor collector saturation current $I_{CO}$.

$$I = \frac{V_{CC} - V_{BE}}{R} \cong \frac{V_{CC}}{R} = constant$$

The diode D is reverse biased by $V_{BE}$ and the current through it is the reverse saturation current $I_O$.

Now the base current is, $I_B = I - I_O$

Substituting the above value in the expression for collector current.

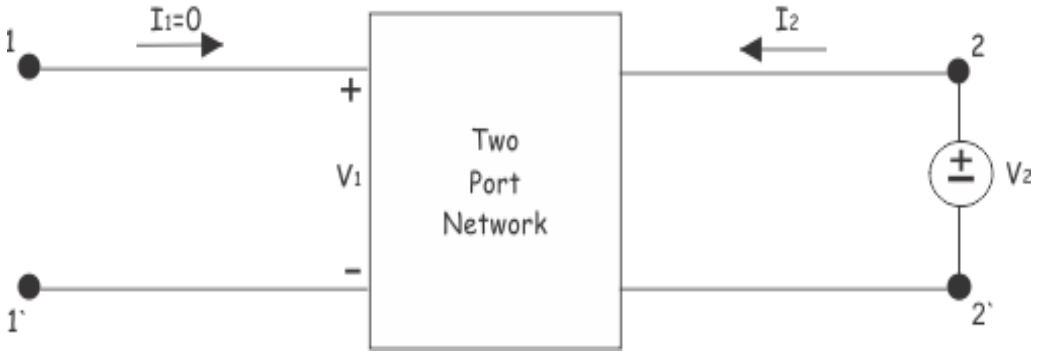
$$I_C = ß(I - I_O) + (1 + ß)I_{CO}$$

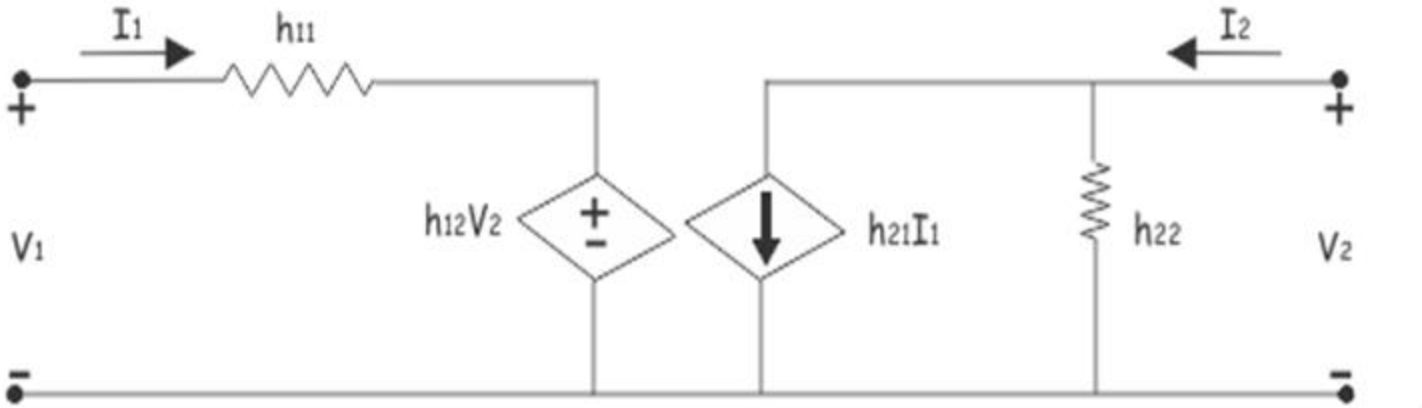
If $\beta \gg 1$, $I_C = ßI - ßI_O + ßI_{CO}$

I is almost constant and if $I_O$ of diode and $I_{CO}$ of transistor track each other over the operating temperature range, then $I_C$ remains constant.

# Analysis of CE, CC, CB Amplifiers

# General Model




h-Parameter model

# General Model

**Current gain:**

$$A_i = \frac{I_L}{I_1}$$

$$I_2 = h_f I_1 + h_o V_2$$

$$V_2 = -I_2 R_L$$

$$I_2 = h_f I_1 + h_o(-I_2 R_L)$$

$$I_2 + h_o(I_2 R_L) = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$$

# General Model

**Current gain(Ais):**

$$A_{is} = \frac{-I_2}{I_s} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_s} = A_i \cdot \frac{I_1}{I_s}$$

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$V_1 = \frac{Z_i}{R_s + Z_i} V_s$$

$$A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

**Input Resistance(Zi):**

$$Z_i = \frac{V_1}{I_1}$$

$$V_1 = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$V_2 = A_i I_1 R_L$$

$$Z_i = h_i + h_r A_i R_L$$

# General Model

**Voltage Gain(Av):**

$$A_v = \frac{V_2}{V_1}$$

$$A_v = \frac{A_i I_1 R_L}{Z_i}$$

**Voltage Gain(Avs):**

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} = \frac{V_1}{V_s}$$

$$A_p = \frac{p_2}{P_1} = A_i^{\,2} \frac{R_L}{Z_i}$$

$$A_{vs} = A_v . \frac{V_1}{V_s}$$

$$V_1 = \frac{Z_i}{R_s + Z_i} V_s$$

$$A_{vs} = \frac{A_i R_L}{R_s + R_i}$$

# General Model

**Output Resistance:**

$$Y_o = \frac{I_2}{V_2}$$

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$Y_0 = h_f \cdot \frac{-h_r}{R_s + h_i} + h_o$$

**Power gain(Ap):**

$$A_p = \frac{p_2}{P_1} = A_v A_i$$

$$A_p = \frac{p_2}{P_1} = A_i^{\,2} \frac{R_L}{Z_i}$$

# General Model

small-signal analysis of a transistor amplifier

$$A_i = -\frac{h_f}{1 + h_o R_L}$$

$$A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

$$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$$

$$A_v = \frac{A_i R_L}{Z_i}$$

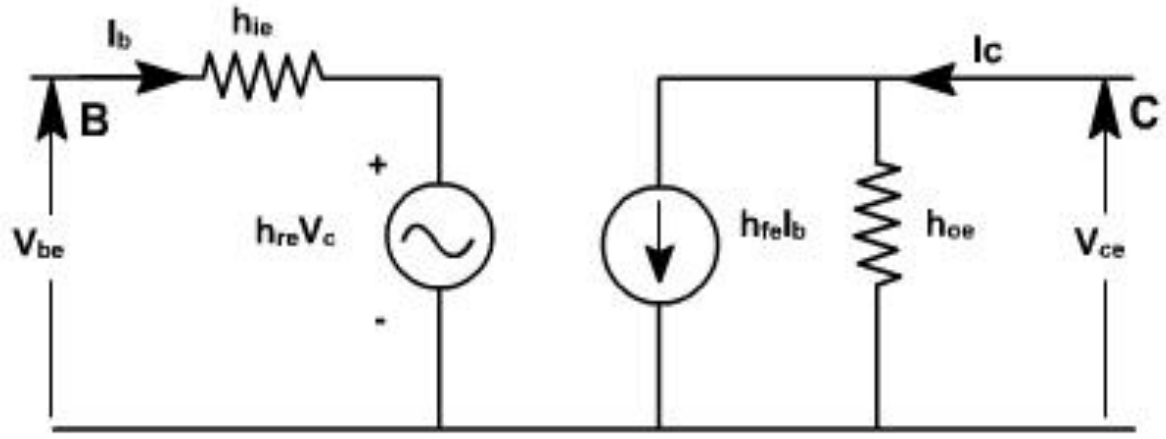
$$A_{vs} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$$

$$A_P = A_V A_i = A_i^2 \frac{R_L}{Z_i}$$

# Common Emitter Exact Analysis

**H-parameter model:**




**Current gain:** $$\frac{I_2}{I_1} = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

**Input Resistance:** $$Z_i = h_{ie} + h_{re}A_iR_L$$

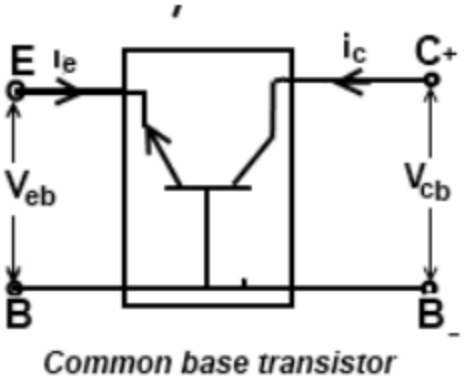
**Voltage Gain:** $$A_v = \frac{A_iI_1R_L}{Z_i}$$

**Output Resistance:** $$Y_0 = h_{fe}.\frac{-h_{re}}{R_s + h_{ie}} + h_{oe}$$

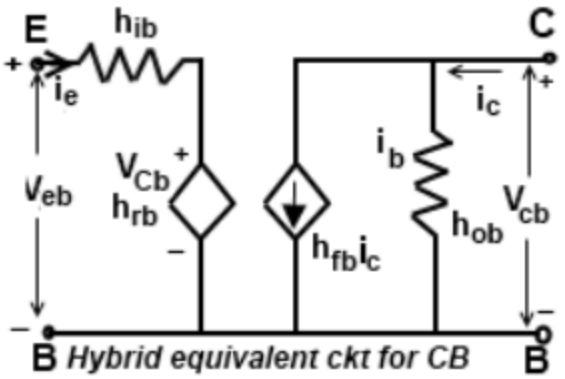
# Common Base Exact Analysis

$V_{be} = h_{ib}.i_b + h_{rb}.V_c$

$i_e = h_{fb}.i_b + h_{ob}.V_c$



Common base transistor



Hybrid equivalent ckt for CB

**Current gain:**

$A_i = -(h_{fb}/(1 + h_{ob}.r_L))$

**Input Resistance:**

$R_i = h_{ib} + h_{rb}.A_i.r_L$

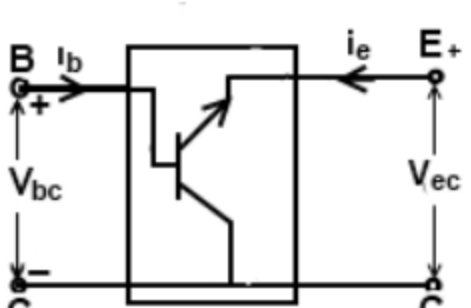
**Output Resistance:**

$$Y_0 = \frac{I_c}{V_c} = h_{ob} - \frac{h_{fb} \times h_{rb}}{h_{ib} + R_s}$$

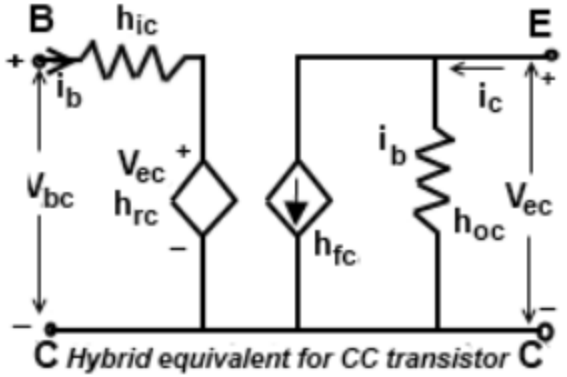
**Voltage Gain:**

$$A_V = \frac{V_c}{V_e} = \frac{A_I \times R_L}{R_i}$$

# Common Collector Exact Analysis



*Common Collector Transistor*



*Hybrid equivalent for CC transistor*

$$V_{bc} = h_{ic}.i_b + h_{re}.V_{ec}$$

$$i_e = h_{fe}.i_b + h_{oe}.V_{ec}$$

$$A_i = -(h_{fc}/(1 + h_{oc}.r_L))$$

$$R_i = h_{ie} + h_{re}.A_i.r_L = h_{ie} - ((h_{rc}.h_{fc})/(h_{oc} + (1/r_L)))$$

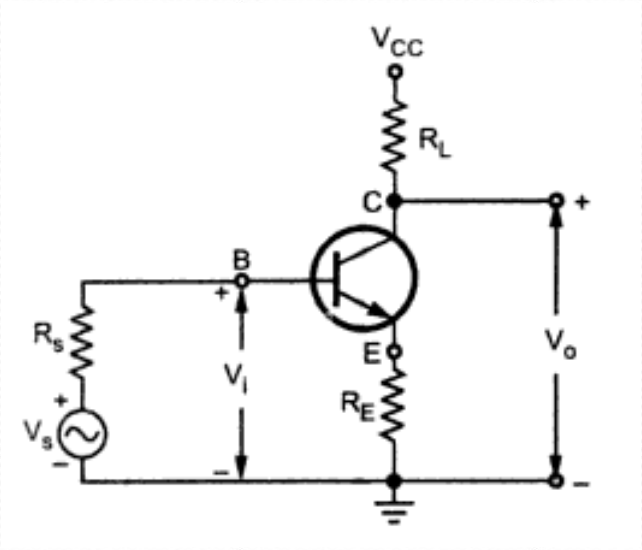
$$A_v = A_i.r_1/R_i$$

$$R_o = (R_s + h_{ic})/(R_s.h_{oc} + \Delta h)$$

$$\Delta h = h_{ic}.h_{oc} - h_{rc}.h_{fc}$$

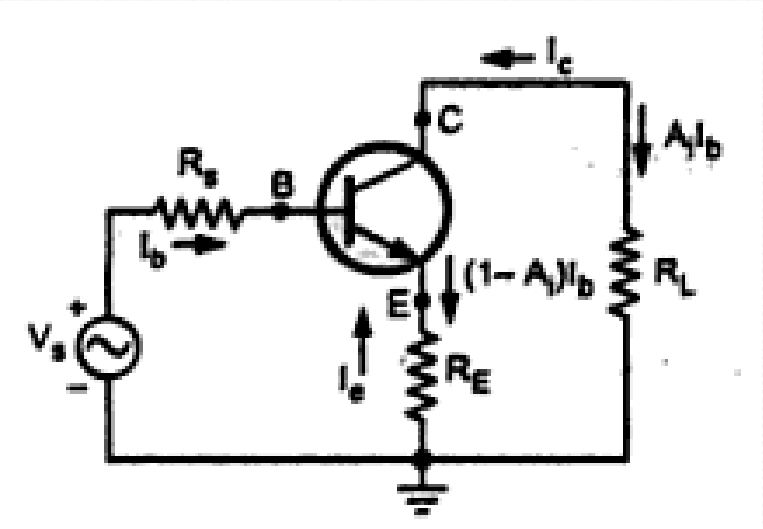
# Analysis of CE Amplifier with emitter resistance

# Analysis Of CE Amplifier With Unbypassed RE

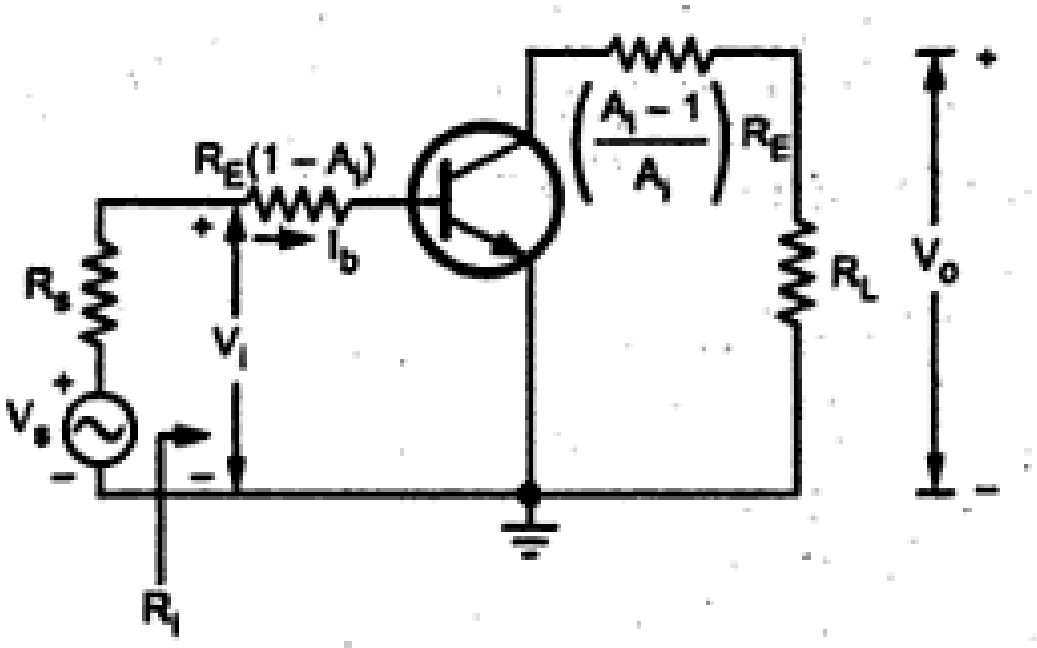



- $R_E$ is added to stabilize the gain of the amplifier
- $R_E$ acts as a feedbackresistor
- The overall gain will reduce with unbypassed $R_E$

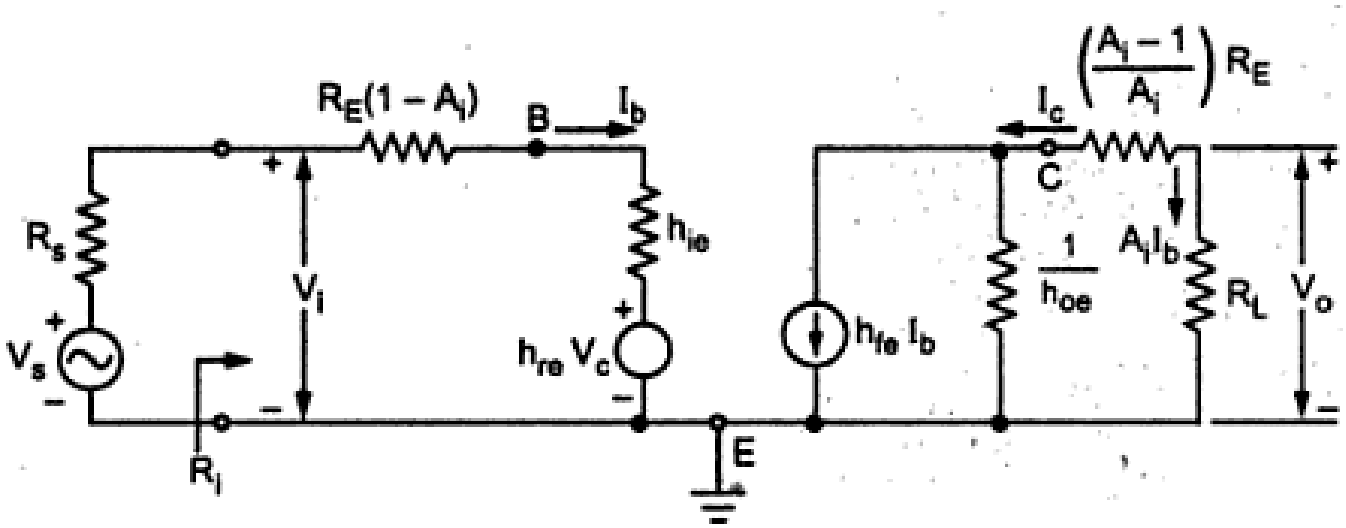
# AC Equivalent Circuit For CE Amplifier with Unbypassed RE



# AC Equivalent Circuit For CE Amplifier with RE Splitted using dual of Miller 's Theorem



# h-Parameter Equivalent Circuit (Exact Analysis)




$$A_i = \frac{-h_{fe}}{1+h_{oe}R_L'} = \frac{-h_{fe}}{1+h_{oe}\left(R_L+\frac{A_i-1}{A_i}R_E\right)}$$

# low frequency response of BJT Amplifiers

# Defining the Low Cutoff Frequency

- In the low-frequency region of the single-stage BJT or FET amplifier, it is the RC combinations formed by the network capacitors CC , CE , and Cs and the network resistive parameters that determine the cutoff frequencies

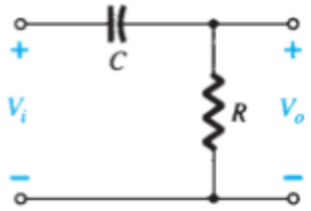
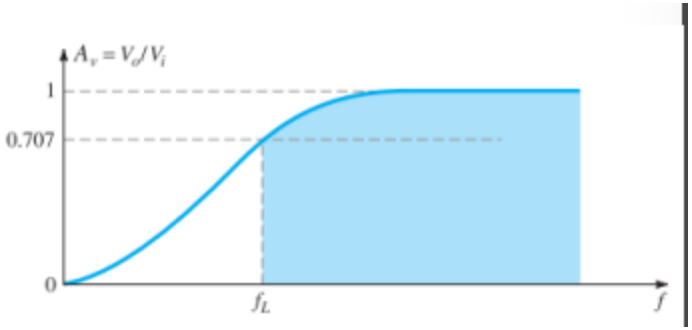
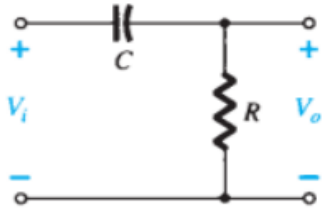



**FIG. 9.14**
*RC combination that will define a low-cutoff frequency.*



# Defining The Low Cutoff Frequency




$$\mathbf{V_o = \frac{RV_i}{R + X_C}}$$

The magnitude of $V_o$ is

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}}$$

For the special case where $X_C = R$,

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}} = \frac{RV_i}{\sqrt{R^2 + R^2}} = \frac{RV_i}{\sqrt{2R^2}} = \frac{RV_i}{\sqrt{2}R} = \frac{1}{\sqrt{2}}V_i$$

$$\boxed{|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707|_{X_C=R}}$$

$$X_C = \frac{1}{2\pi f_L C} = R$$

$$\boxed{f_L = \frac{1}{2\pi RC}}$$

$$G_v = 20\log_{10}A_v = 20\log_{10}\frac{1}{\sqrt{2}} = -3\text{ dB}$$

$A_v = V_o/V_i = 1$ or $V_o = V_i$ (the maximum value),

$$G_v = 20\log_{10}1 = 20(0) = 0\text{ dB}$$

$$A_v = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j(1/\omega CR)} = \frac{1}{1 - j(1/2\pi fCR)}$$

$$\boxed{f_L = \frac{1}{2\pi RC}} \qquad \boxed{A_v = \frac{1}{1 - j(f_L/f)}}$$

In the magnitude and phase form,

$$A_v = \frac{V_o}{V_i} = \underbrace{\frac{1}{\sqrt{1 + (f_L/f)^2}}}_{\text{magnitude of } A_v} \underbrace{\angle \tan^{-1}(f_L/f)}_{\text{phase } \measuredangle \text{ by which } V_o \text{ leads } V_i}$$

when $f = f_L$,

$$|A_v| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \Rightarrow -3\text{ dB}$$

$$\boxed{A_{v(\text{dB})} = 20\log_{10}\frac{1}{\sqrt{1 + (f_L/f)^2}}}$$

# Effect of coupling and bypass capacitors on CE Amplifier

In the voltage-divider ct.
→ the capacitors Cs, $C_C$ , and $C_E$ will determine the low-frequency response.

$$f_L = \min(f_{Ls}, f_{Lc}, f_{LE})$$

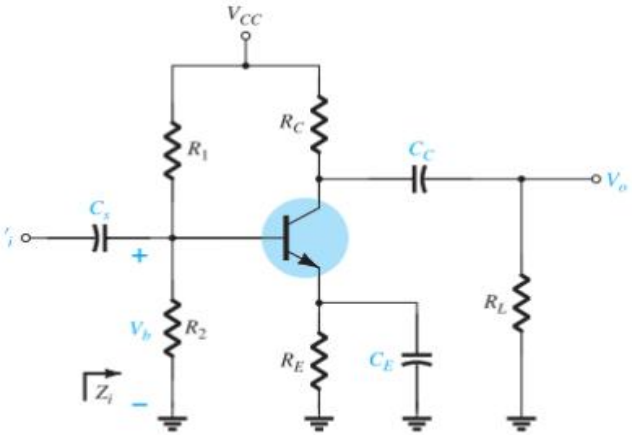



**FIG. 9.25**
*Loaded BJT amplifier with capacitors that affect the low-frequency response.*

→Cs:

$$\mathbf{V}_b = \frac{R_i \mathbf{V}_i}{R_i - jX_{C_s}}$$

$$f_{L_s} = \frac{1}{2\pi R_i C_s} \qquad R_i = R_1 \| R_2 \| \beta r_e.$$

$$\mathbf{A}_v = \frac{\mathbf{V}_b}{\mathbf{V}_i} = \frac{1}{1 - j(f_{L_s}/f)}$$

→ Cc:

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C}$$

$$R_o = R_C \| r_o$$

→ $C_E$:

$$f_{L_E} = \frac{1}{2\pi R_e C_E}$$

$$R_e = R_E \| \left( \frac{R_1 \| R_2}{\beta} + r_e \right)$$

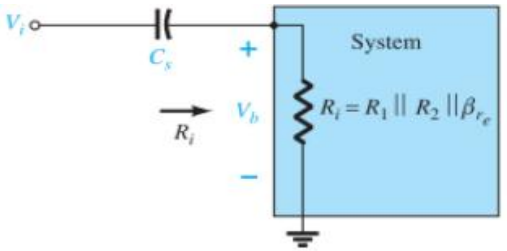



**FIG. 9.26**
*Determining the effect of $C_s$ on the low-frequency response.*

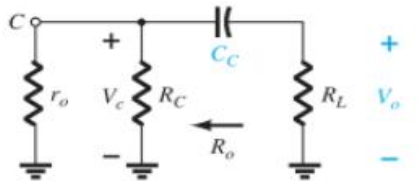



**FIG. 9.28**
*Localized ac equivalent for $C_C$ with $V_i = 0$ V.*

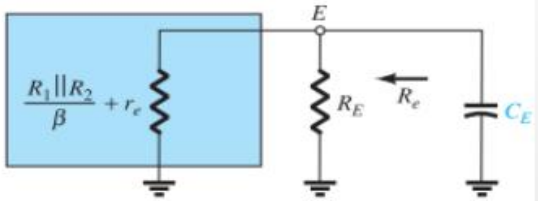
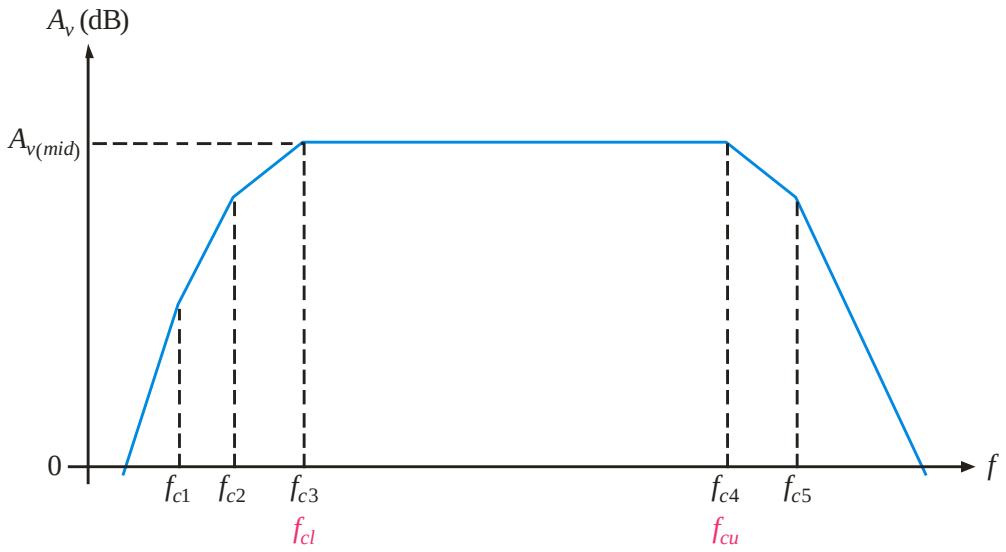



**FIG. 9.30**
*Localized ac equivalent of $C_E$.*

In general, the overall frequency response is the combination of three lower critical frequencies due to coupling and bypass capacitors and two upper critical frequencies due to internal capacitances.

The bandwidth is measured between the dominant critical frequencies.



# Problems

# Problems

1. In a Silicon transistor circuit with a fixed bias, VCC=9V, RC=3KΩ, RB=8KΩ, β = 50, VBE=0.7V. Find the operating point and Stability factor.

2. In a Silicon transistor circuit with a fixed bias, VCC=25V, RC=820Ω, RB=180KΩ, β = 80, VBE=0.7V. Determine the values of base current, emitter current and the collector to emitter voltage.

3. In a Silicon transistor circuit with a fixed bias, VCC=12V, RC=330Ω,IB=0.3mA, β = 100, VBE=0.7V. Determine the value of bias resistor RB and Stability factor.

# Problems

4. In a Silicon transistor circuit with a collector to base bias, VCC=10V, RC=10KΩ, RB=100KΩ, β = 100, VBE=0.7V. Calculate the operating point and also draw the load line and locate Q point on it.

5. An NPN transistor with β =50 is used in a common emitter circuit with Vcc=10V,Rc=2K Ω. The bias is obtained by connecting a 100K Ω resistance from collector to base. Assume VBE=0.7V. Find

   (a)The quiescent point

   (b)The stability factor S.

# Problems

6. **Determine the quiescent currents and the collector to emitter voltage for a germanium transistor with β=50 in self biasing arrangement. Draw the circuit with a given component values Vcc=20V,Rc=2K Ω,Re=100 Ω,R1=100K Ω,R2=5K Ω. Also find the stability factor.**

7. **Design a self bias circuit as per the following specifications. Vcc=12V,Vce=2V,Ic=4mA,hfe=80. Draw the complete diagram with the designed values.**

8. **The hybrid parameters for a transistor used in CE configuration are hie = 5kΩ; hfe = 180; hre = 1.25 × 10-4; hoe = 16 × 10-6 ohms. The transistor has a load resistance of 20 KΩ in the collector and is supplied from a signal source of resistance 5 KΩ. Compute the value of input impedance, output impedance, current gain and voltage gain.**


# Unit - IV
# JUNCTION FIELD EFFECT TRANSISTOR

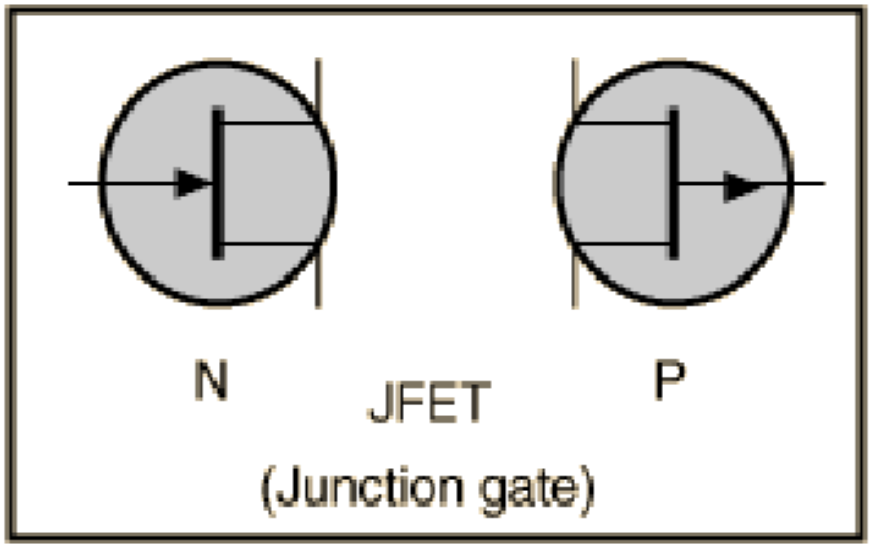
# TOPICS

- Construction
- Principle of Operation
- Pinch-Off Voltage
- Volt- Ampere Characteristic
- Comparison of BJT and FET
- Biasing of FET
- FET as Voltage Variable Resistor
- MOSFET Construction and its Characteristics in Enhancement and Depletion modes

# TYPES OF FET, FET CONSTRUCTION, SYMBOL

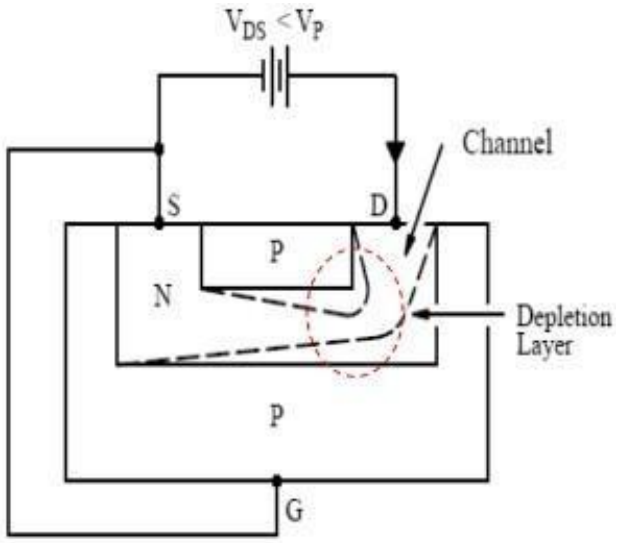
The family of FET devices may be divided into :

- Junction FET
- Depletion Mode MOSFET
- Enhancement Mode MOSFET

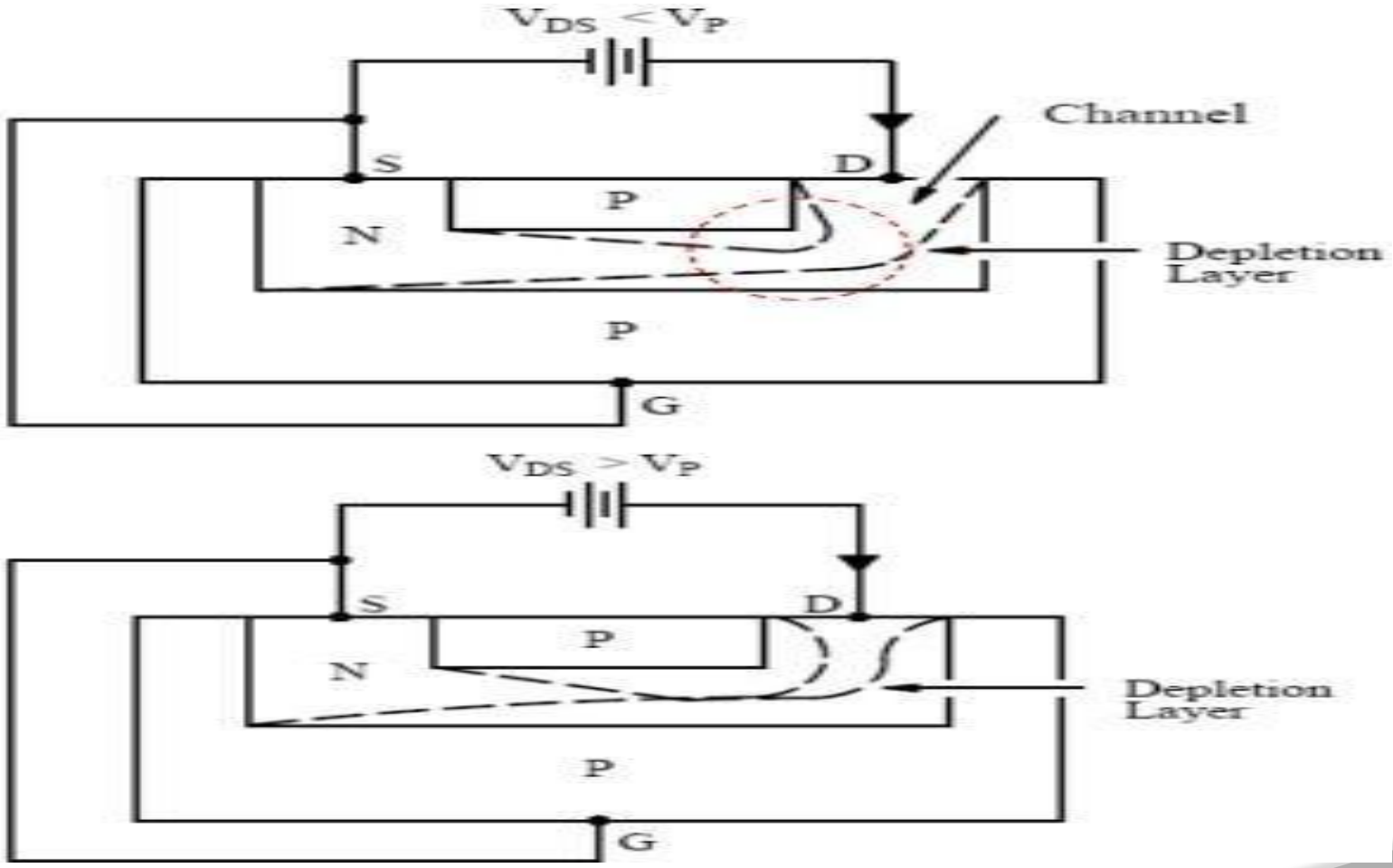


# FET PRINCIPLE OF OPERATION

- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a depletion layer, where almost all the electrons

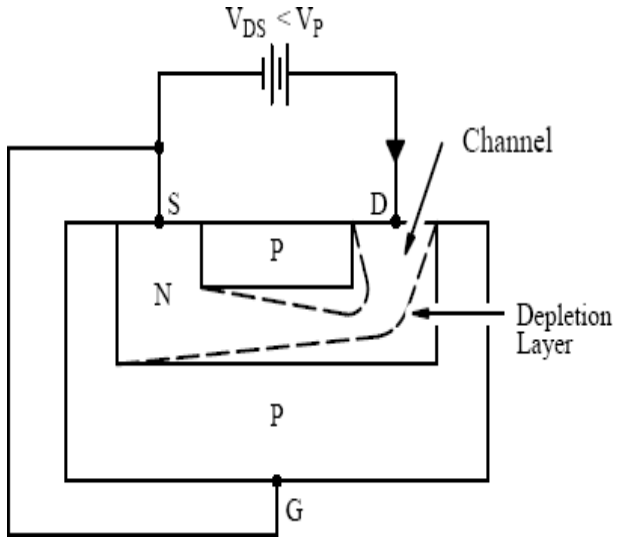


# FET PRINCIPLE OF OPERATION

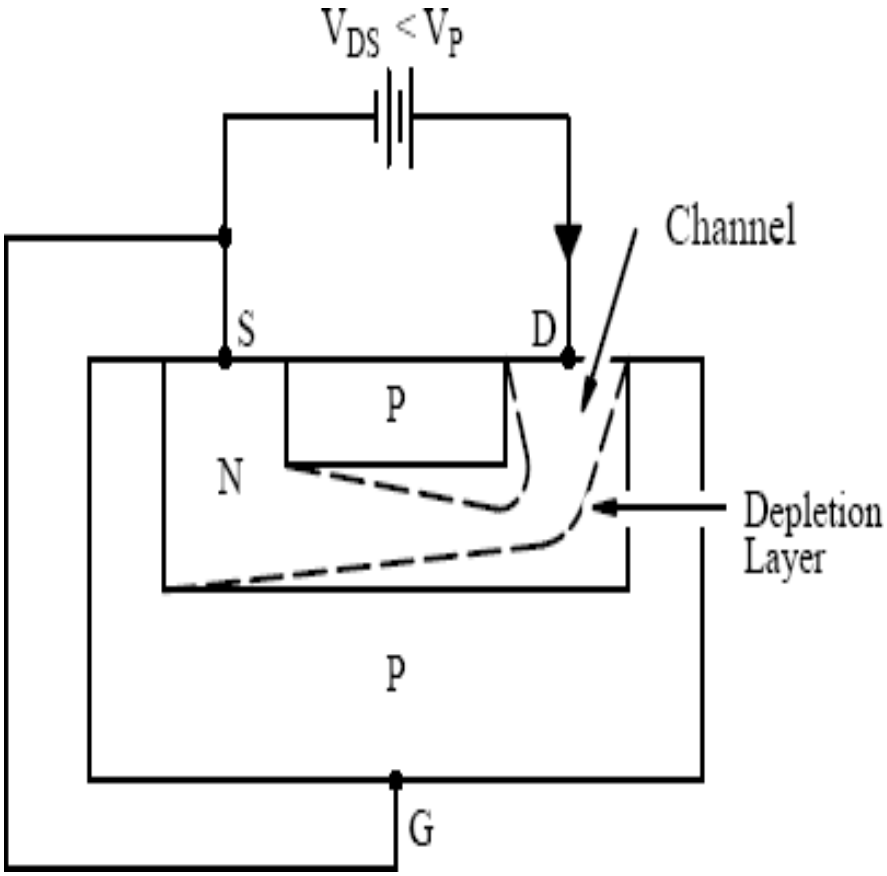


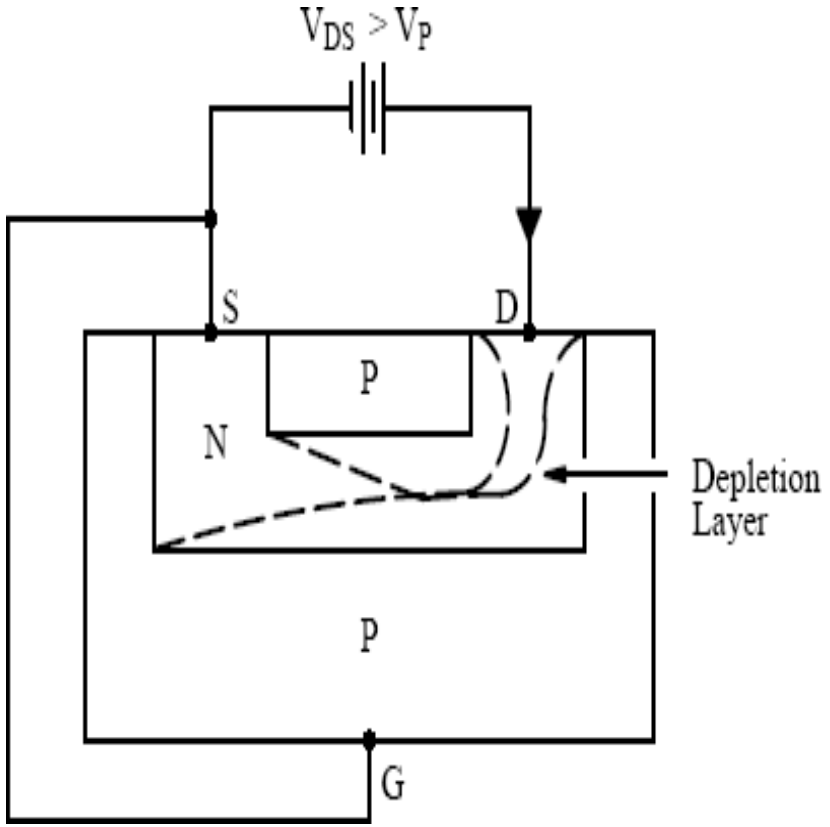
# FET PRINCIPLE OF OPERATION

- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection.
- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away.
- The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.



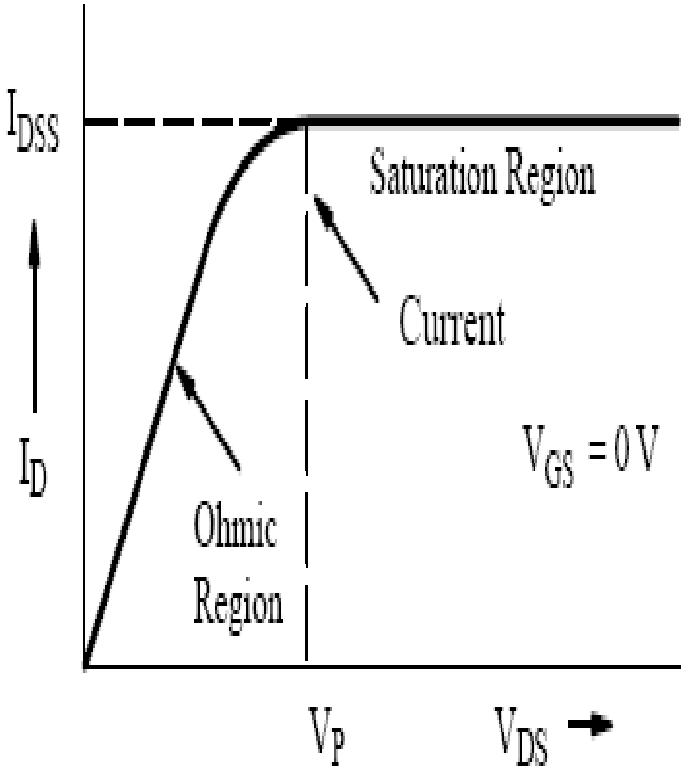
# FET PRINCIPLE OF OPERATION



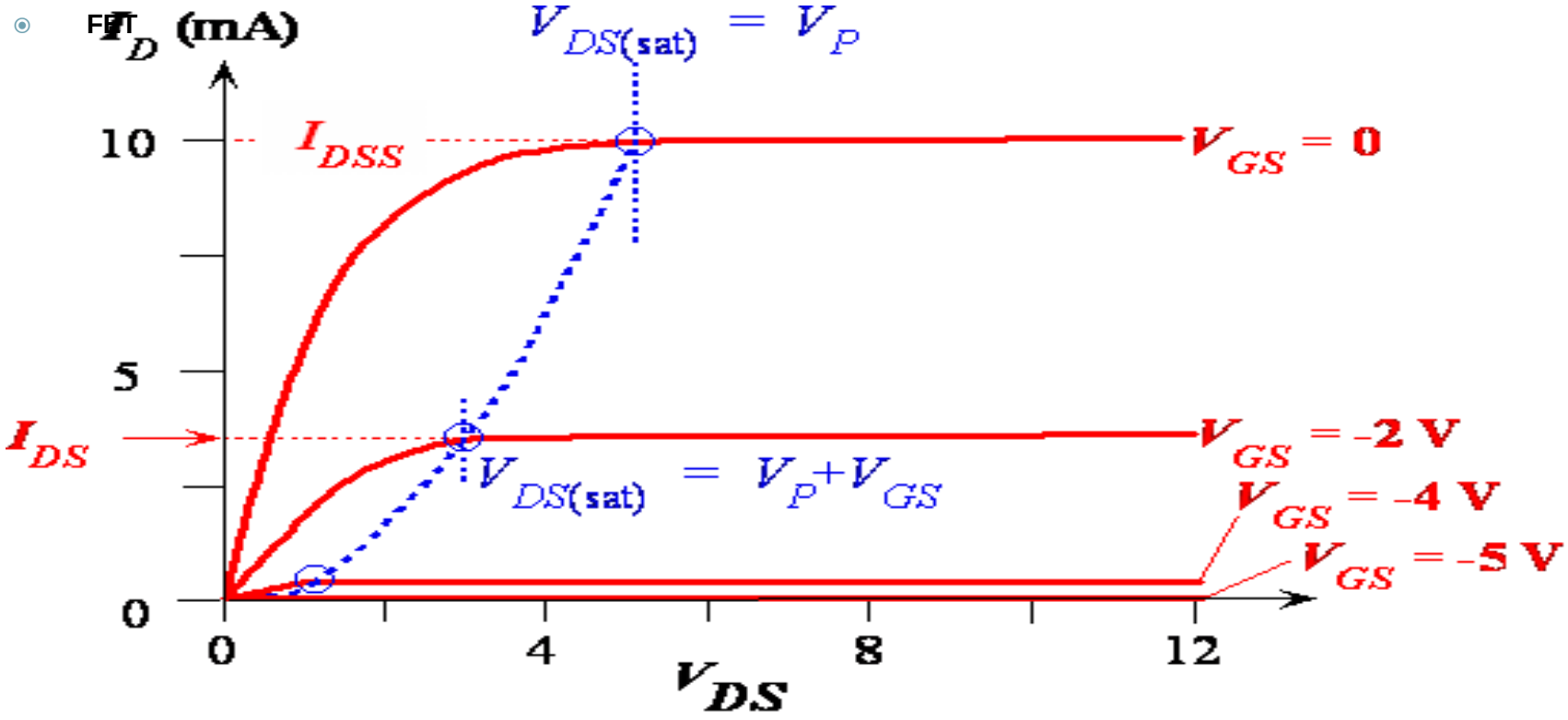
# FET V-I CHARACTERISTICS

- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in $I_D$ is related to the buildup of the depletion layer as $V_{DS}$ increases.
- The curve approaches the level of the limiting current $I_{DSS}$ when $I_D$ begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage, $V_P$, which is the value of $V_{DS}$ at which the maximum $I_{DSS}$ flows.



# FET V-I CHARACTERISTICS

- FET



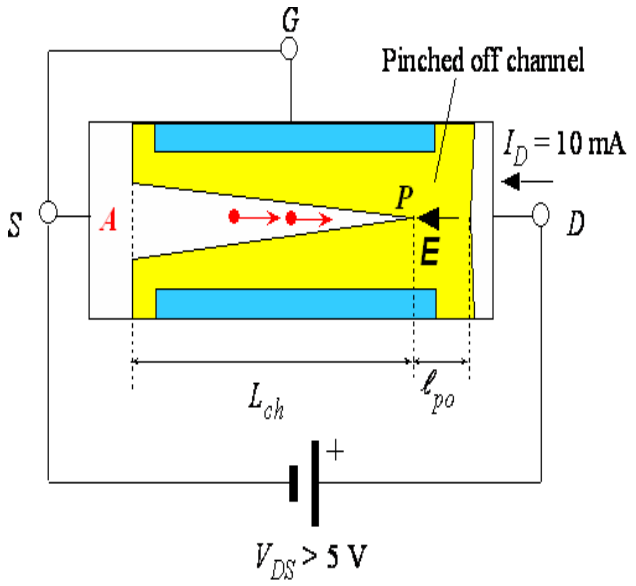

Typical $I_D$ vs $V_{DS}$ characteristics of a JFET for various fixed gate voltages $V_{GS}$.

# FET V-I CHARACTERISTICS

- Beyond $V_{DS} = V_P$, there is a short pinch- off channel of length, $\ell_{po}$.
- As $V_{DS}$ increases, most of additional voltage simply drops across as this region is depleted of carriers and hence highly resistive.
- Voltage drop across channel length, $L_{ch}$ remain as $V_P$.
- Beyond pinch-off then

$$I_D = V_P/R_{AP}$$

$(V_{DS}>V_P)$




The pinched-off channel and conduction for $V_{DS} > V_P$ (=5 V).

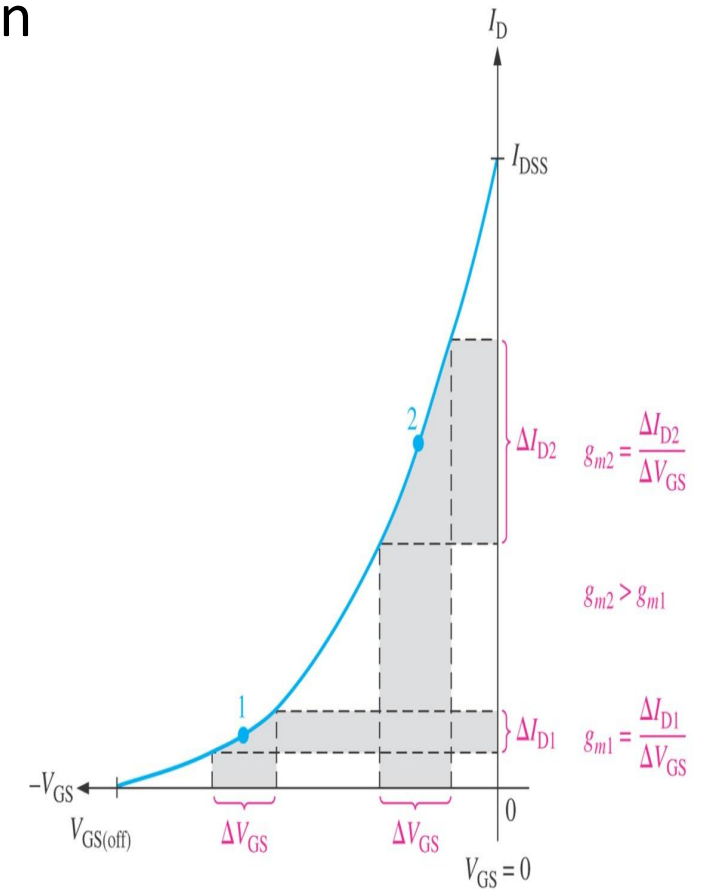
# FET PARAMETERS

**Forward transfer conductance, $g_m$** of JFETs is the changes in $I_D$ based on changes in $V_{GS}$ with $V_{DS}$ is constant.

**Forward transfer conductance** referred to as $g_m = \Delta I_D / \Delta V_{GS}$.

Unit is Siemens (s)

The value is larger at the top of the curve (near $V_{GS}$=0) but become smaller as you increase $V_{GS}$ (near $V_{GS(off)}$).



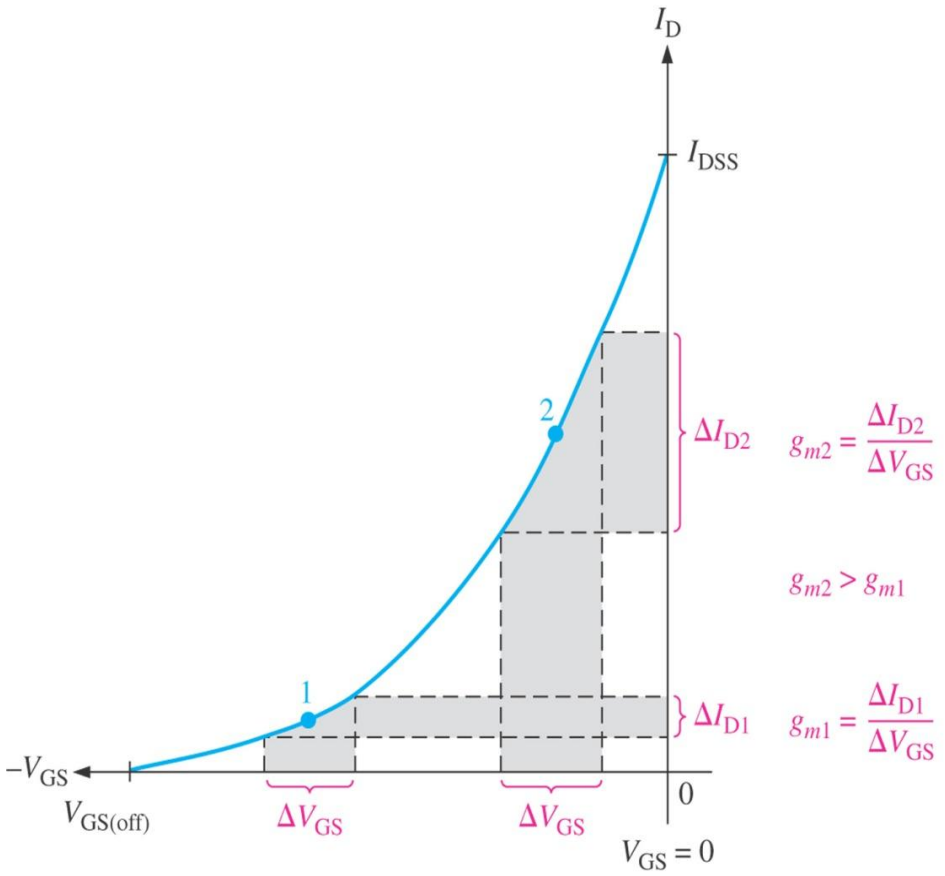
# FET PARAMETERS

At $V_{GS}$ =0, the parameter is known as minimum transfer conductance, $g_{mo}$ and can be calculated using this equation:

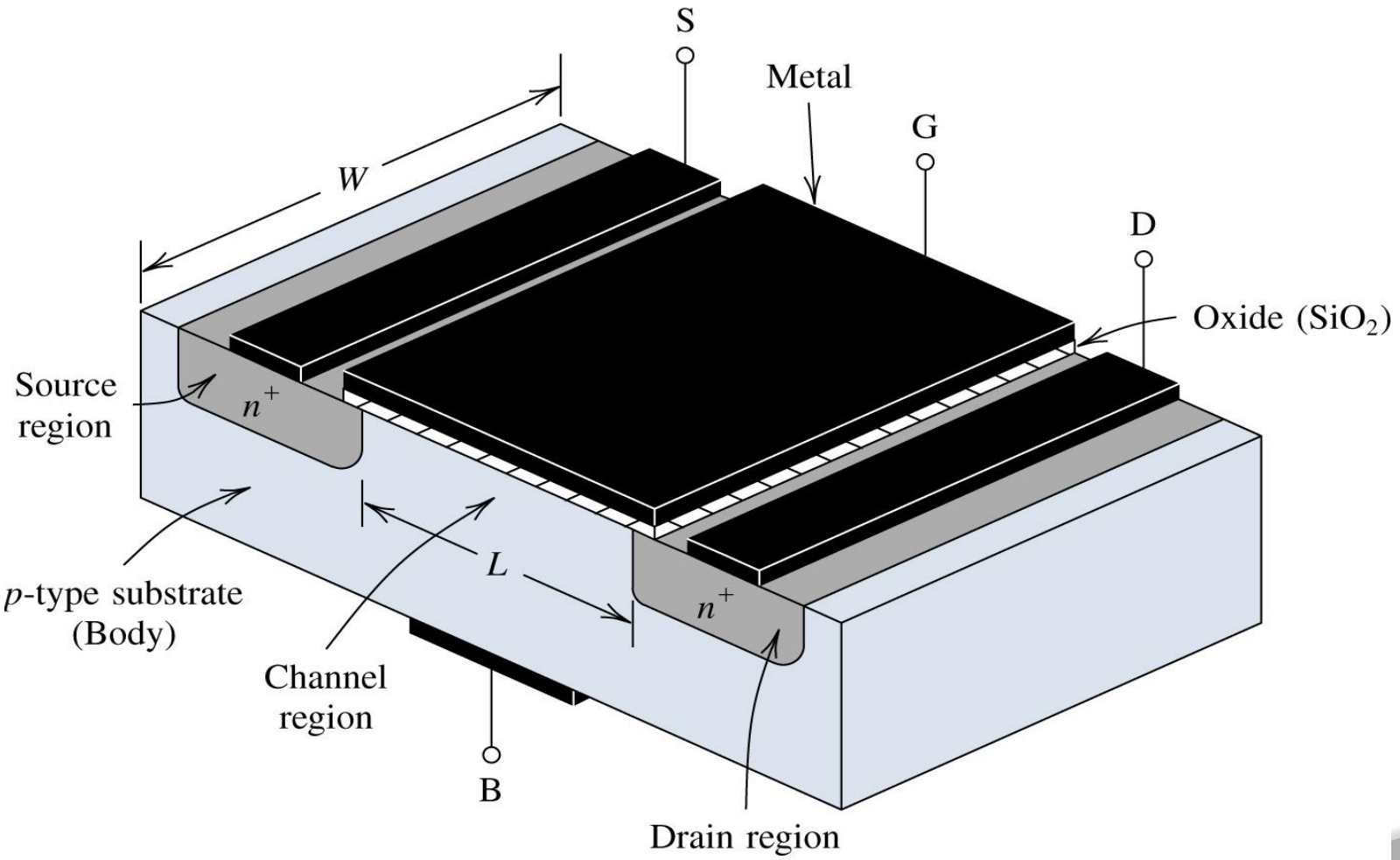
$g_{mo} = 2I_{DSS}/|V_{GS(off)}|$ and

$g_m = g_{mo}(1 - V_{GS}/V_{GS(off)})$

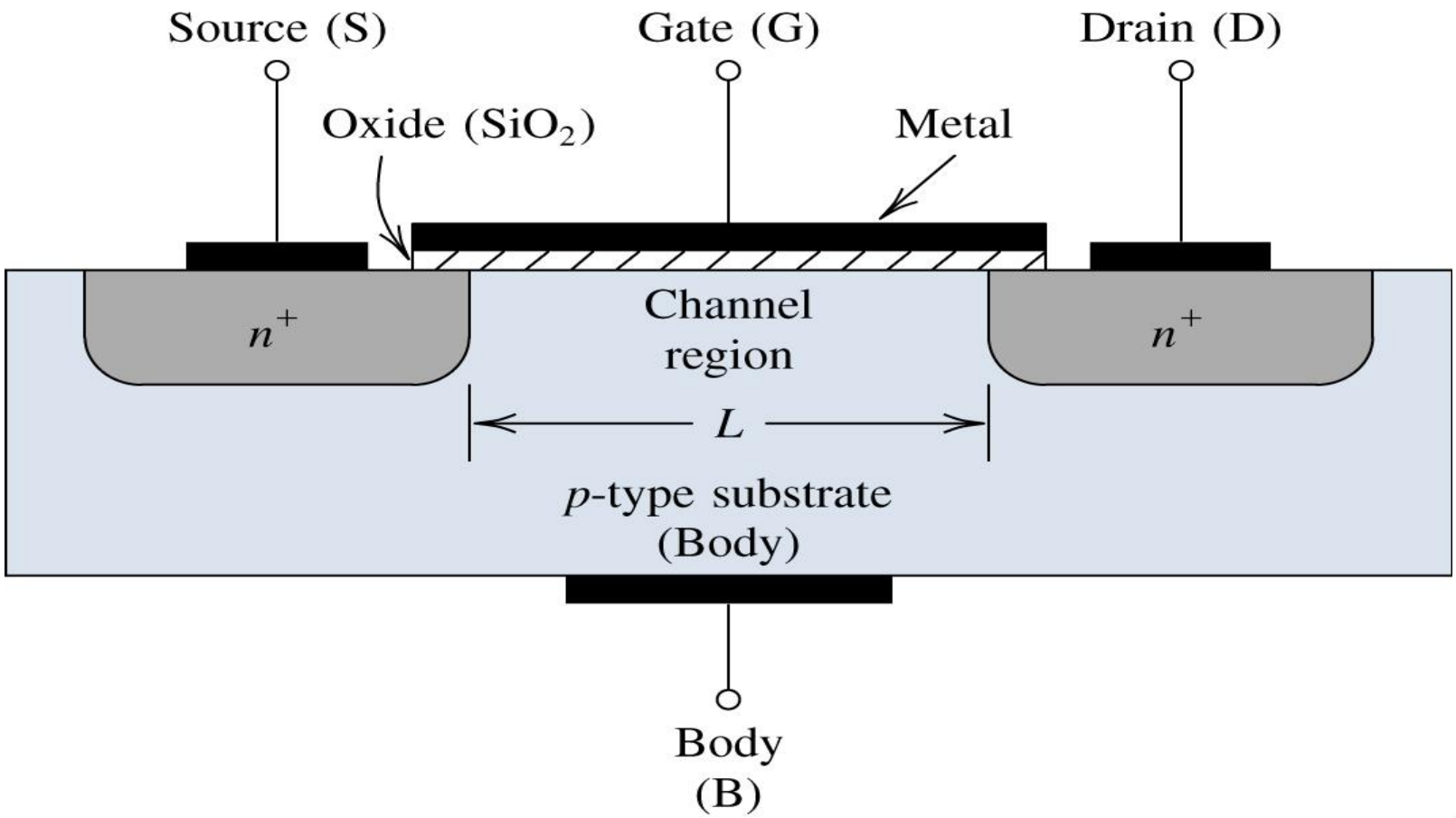
$g_{mo}$ can be read from the datasheet as $g_{fs}$ or $y_{fs}$ and sometimes written as Forward Transfer Admittance.



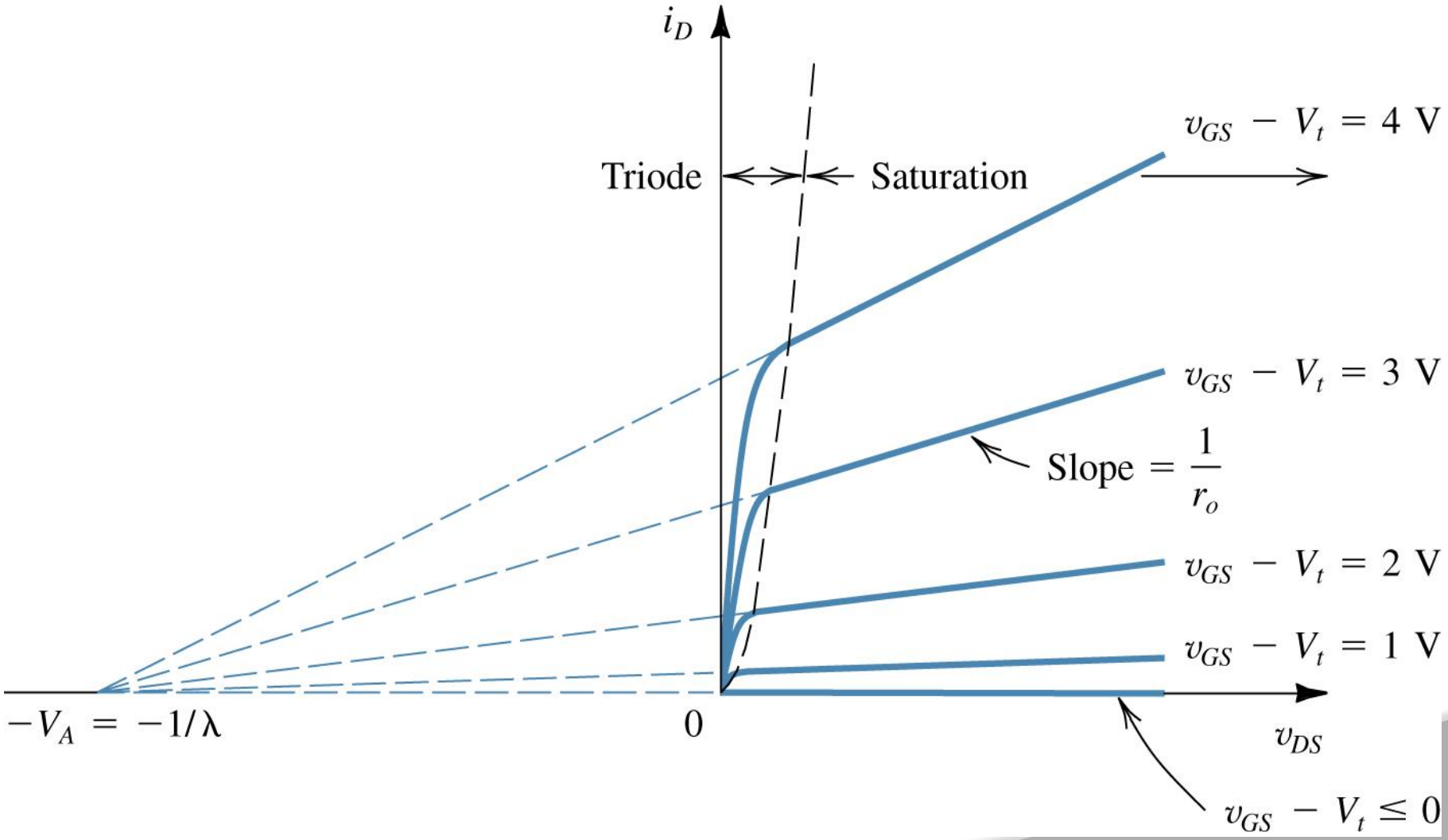
# MOSFET CONSTRUCTION AND OPERATION



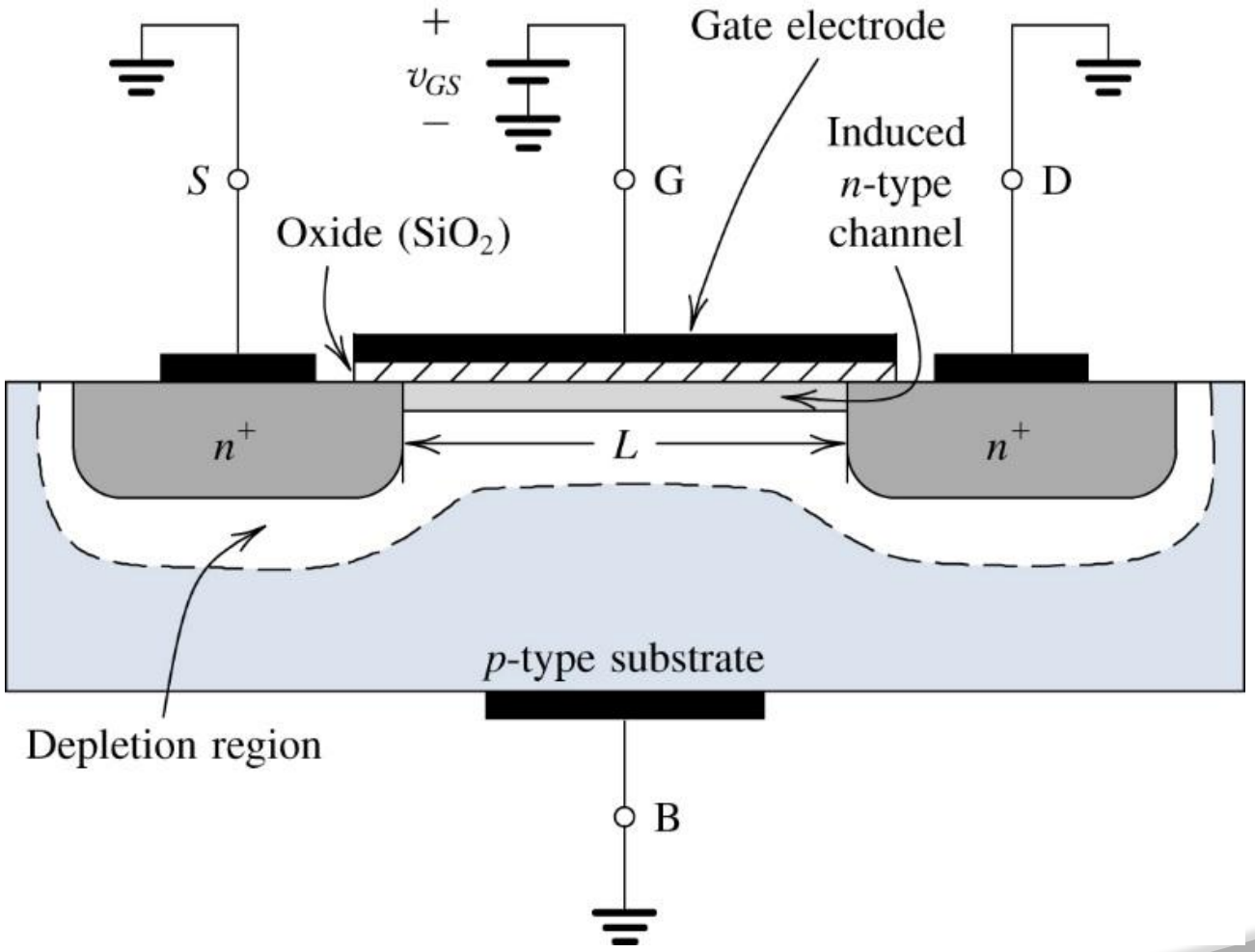
# MOSFET CONSTRUCTION AND OPERATION



# MOSFET CONSTRUCTION AND OPERATION

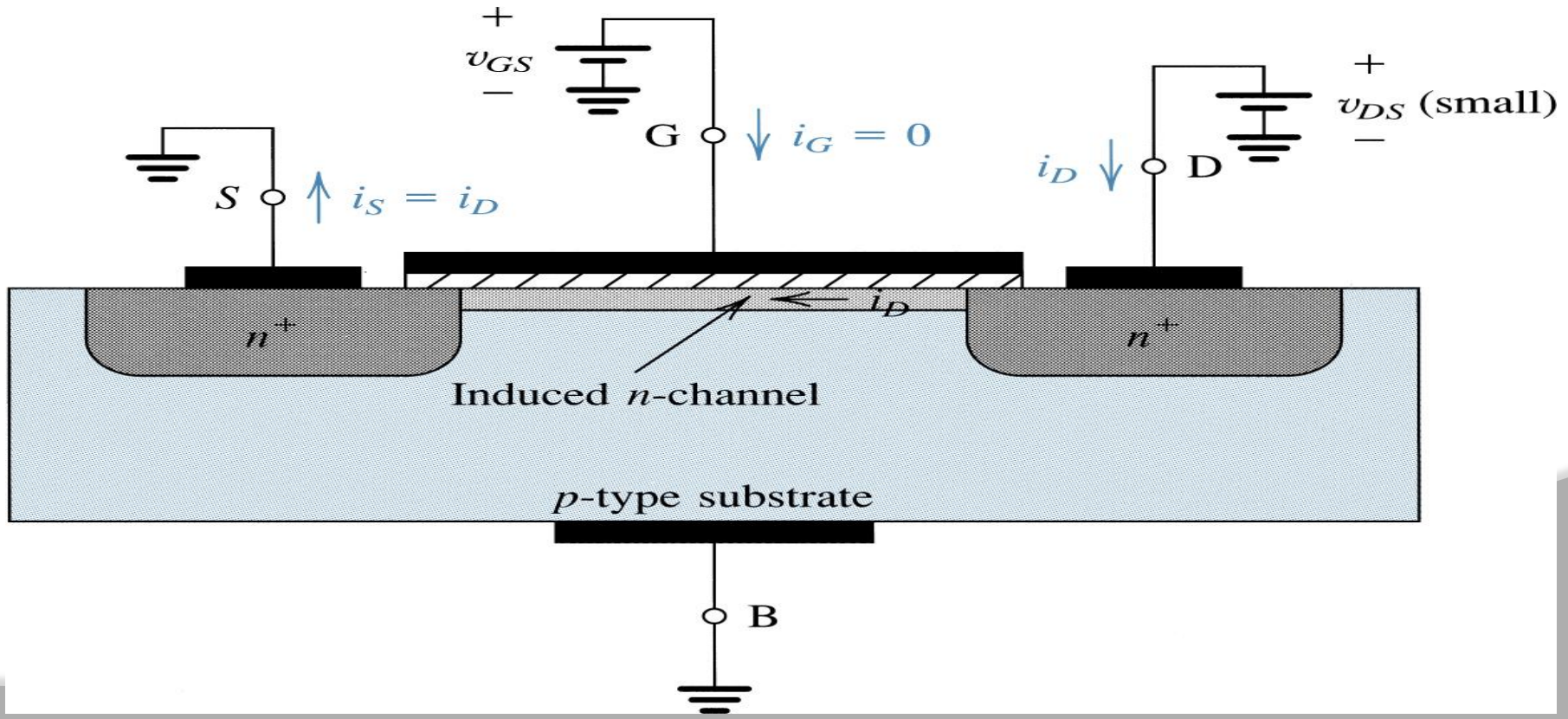


# MOSFET CONSTRUCTION AND OPERATION



# MOSFET CONSTRUCTION AND OPERATION

An NMOS transistor with $v_{GS} > V_t$ and with a small $v_{DS}$ applied. The device acts as a conductance whose value is determined by $v_{GS}$. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and this $i_D$ is proportional to $(v_{GS} - Vt)\, v_{DS}$.

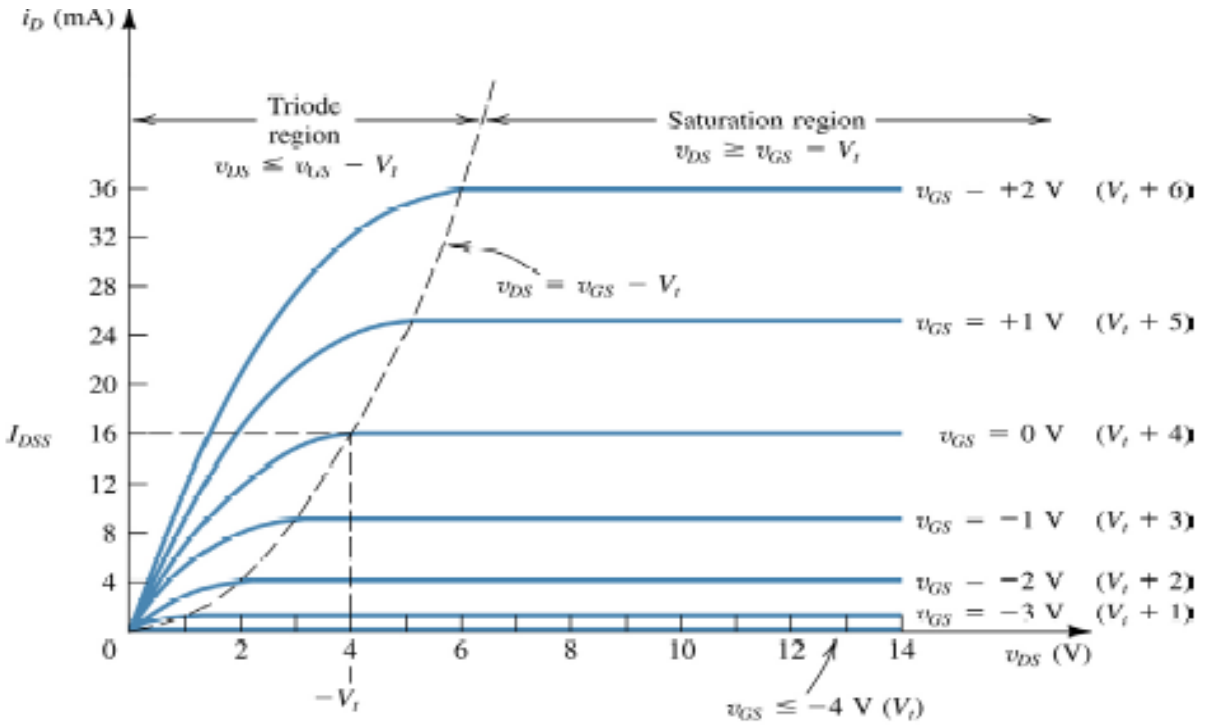


# MOSFET CONSTRUCTION AND OPERATION

For the transistor to operate in the saturation region, $v_{DS} > |Vt|$.

For $v_{GS} = 0$, the drain current is denoted as $I_{DSS}$ and is given by,

$$I_{DSS} = \frac{1}{2}k'(W/L)(V_t)^2$$




The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which $V_t = -4$ V and $k'_n(W/L) = 2$ mA/V²: the $i_D$ - $v_{GS}$ characteristic in saturation.

# BIASING THE FET AND MOSFET

- Biasing an FET amplifier circuit is similar to BJT amplifiers.
- The components are used external to the transistor and dc sources to define a predictable and stable operating point, about which the circuit may provide linear amplification.
- Bias stability in FET amplifiers means that the dc drain current (ID) stays as constant as possible with variations in operating conditions and device parameters.
- For the FET to operate as a linear amplifier, the Q-point should be in the middle of the saturation region, the instantaneous operating point must at all times be confined to the saturation region, and the input signal must be kept sufficiently small.

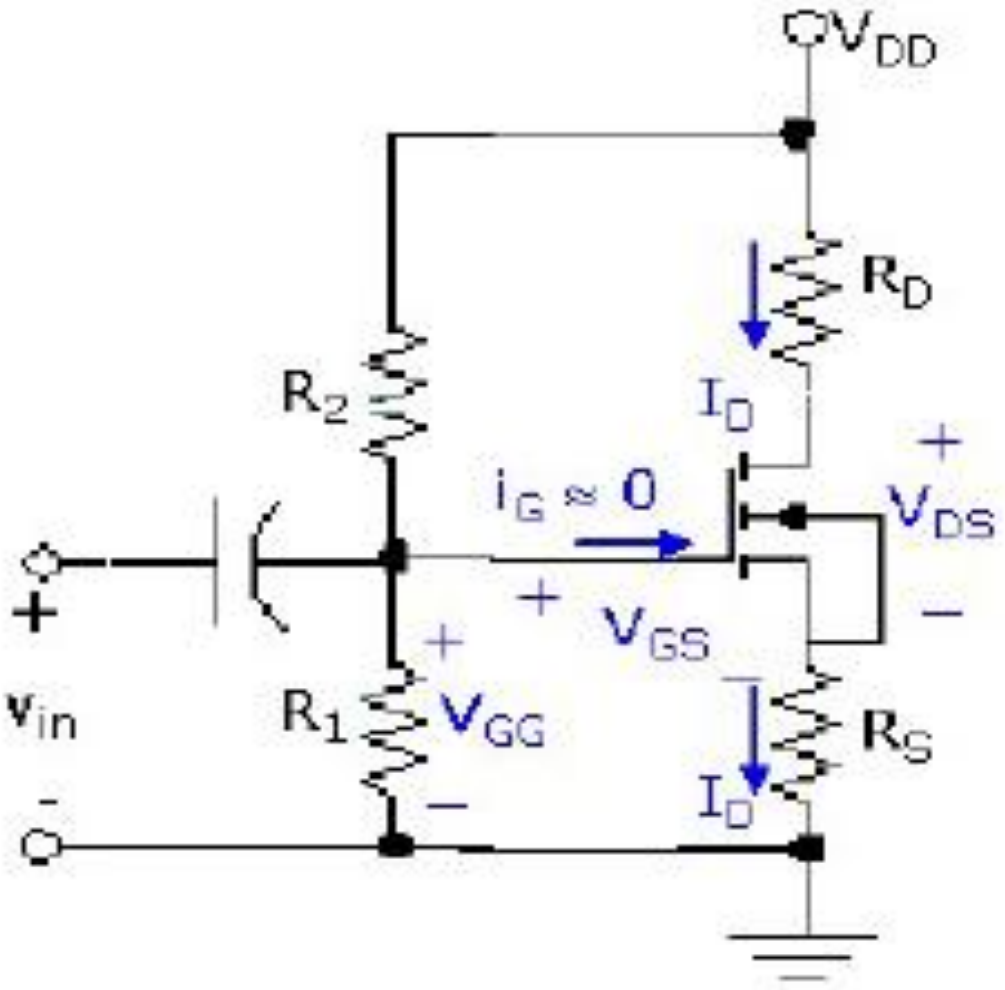
# BIASING THE FET AND MOSFET

- Discrete-component biasing using source-resistance feedback is illustrated in the figure. Although the circuit is shown with an enhancement MOSFET, this biasing arrangement works for depletion MOSFETs and JFETs.

- Note that if two supplies (VDD and –VSS) are used instead of the single-supply illustrated, all derived expressions will use VDD-VSS, rather than VDD.

- For depletion mode MOSFETs or JFET devices, R2 can be either finite or infinite (open). To start with, we are also going to use the assumption that capacitors used in the circuit are large enough to provide dc isolation and act as shorts under ac conditions (the old “infinite and ideal” ploy).

# BIASING THE FET AND MOSFET



# BIASING THE FET AND MOSFET

$$R_G = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{GG} = \frac{V_{DD} R_1}{R_1 + R_2}$$

- Looking at the figure above, we have three unknown variables to define for biasing (IDQ, VGSQ and VDSQ), so we need three dc equations. The first is found from the definition of the drain current in the saturation region, while the other two are the KVL equations obtained from the Thevenin equivalent circuit.

$$I_{DQ} = K(V_{GSQ} - V_T)^2(1 + \lambda V_{DSQ}) \cong K(V_{GSQ} - V_T)^2 = KV_T^2\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 \quad (MOSFET)$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2(1 + \lambda V_{DSQ}) \cong I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \quad (JFET)$$


# Unit - V
# FET AMPLIFIERS

# UNIT-V

Small Signal Model,
Analysis of CS, CD, CG JFET Amplifiers
Basic Concepts of MOSFET Amplifiers
Special Purpose Devices:
Zener Diode – Characteristics
Voltage Regulator
Principle of Operation - SCR
Tunnel diode
UJT
Varactor Diode

# INTRODUCTION TO JFET

FET has three terminals.

1.Drain (d) 2.source (s) 3.gate(g)

The gate is the control input.

There are 3 basic FET circuit configurations:

i)Common Source.

ii)Common Drain.

iii)Common Gate.

# COMMON SOURCE AMPLIFIER

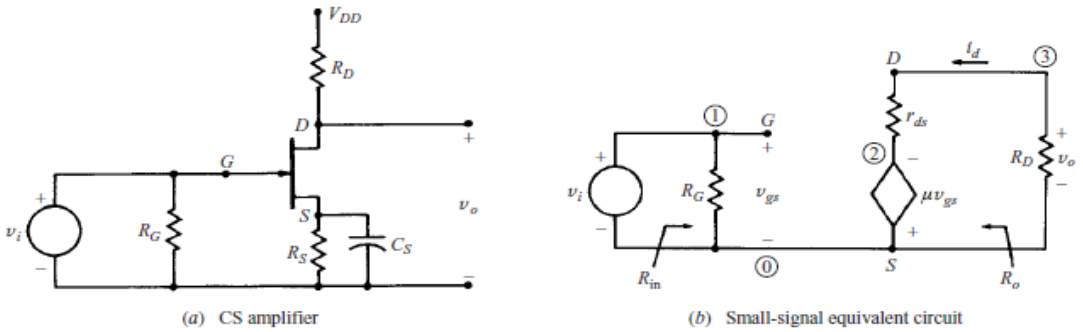



Fig:CS Amplifier (b) Small-signal equivalent circuit

**Voltage Gain:** Source resistance ($R_S$) is used to set the Q-Point but is bypassed by $C_S$ for mid-frequency operation.

From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs} (R_D + r_d)$$

Where $V_{gs} = V_i$ , the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

# COMMON SOURCE AMPLIFIER

**Input Impedance:**

From Fig. Input Impedance is

$$Z_{i} = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

**Output Impedance:**

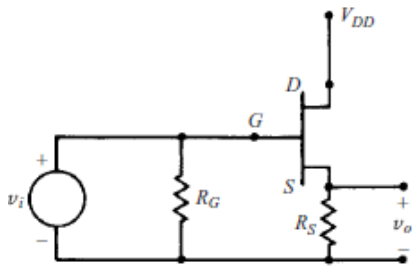
Output impedance is the impedance measured at the output terminals with the input voltage Vi = 0.

when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence $\mu V_{gs} = 0$

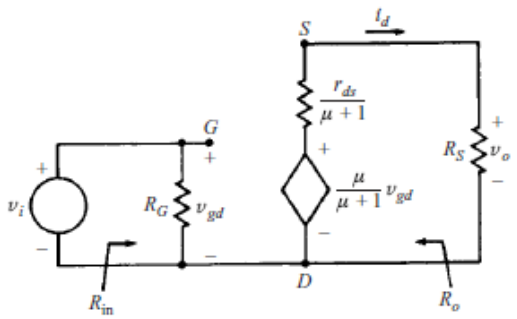
Output impedance $Z_o = r_d \parallel R_D$

Normally $r_d$ will be far greater than $R_D$ . Hence $Z_o \approx R_D$

# COMMON DRAIN AMPLIFIER




(a) CD or SF amplifier




(b) Small-signal equivalent circuit

In electronics, a **common-drain amplifier**, also known as a **source follower**, is one of three basic single-stage field effect transistor (FET) **amplifier** , typically used as a voltage buffer. ... That resistance reduction makes the combination a more ideal voltage source.

# COMMON DRAIN AMPLIFIER

**Voltage Gain:**

The output voltage,

$$V_O = R\text{-}_S \mu V_{gd} / (\mu + 1) R\text{-}_S + r_d$$

Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain, $\mathbf{A_v = V_O / V_i = R\text{-}_S \mu / (\mu + 1) R\text{-}_S + r_d}$

**Input Impedance:**

Input Impedance $Z_i = R_G$

**Output Impedance:**

Output impedance measured at the output terminals with input voltage $V_i = 0$ can be calculated from the equivalent circuit.

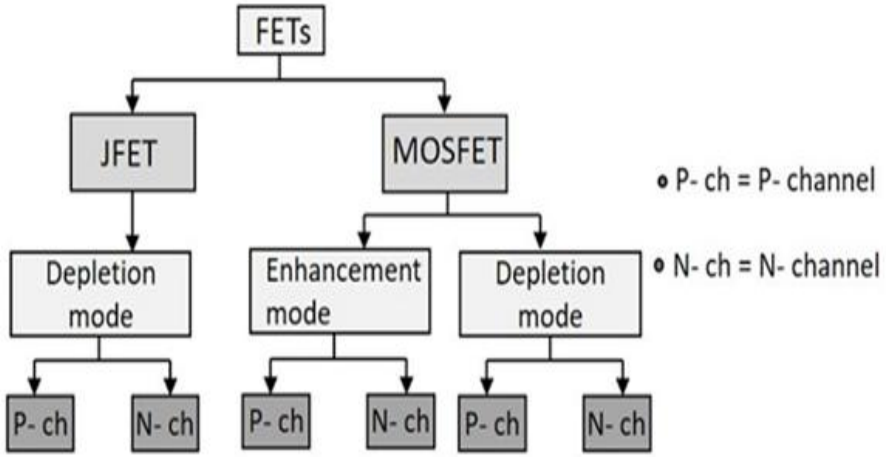
As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

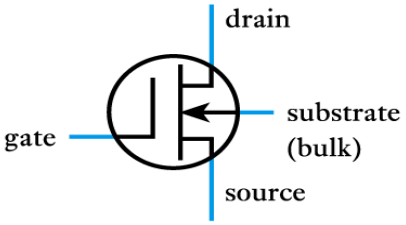
Output Impedance: $\mathbf{Z_O = r_d / (\mu + 1) \parallel R_S}$

When $\mu \gg 1$ $\mathbf{Z_O = (r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S}$

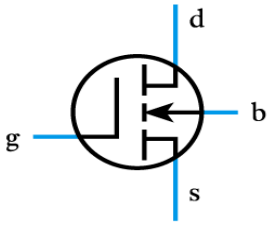
# Types of FETs

There are two main types of FETS. They are JFET and MOSFET.

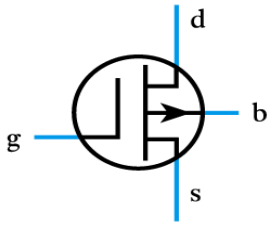


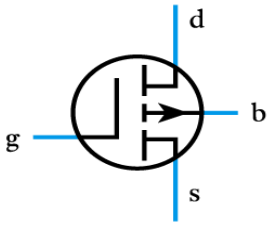

*n*–channel DE MOSFET




*n*–channel enhancement MOSFET



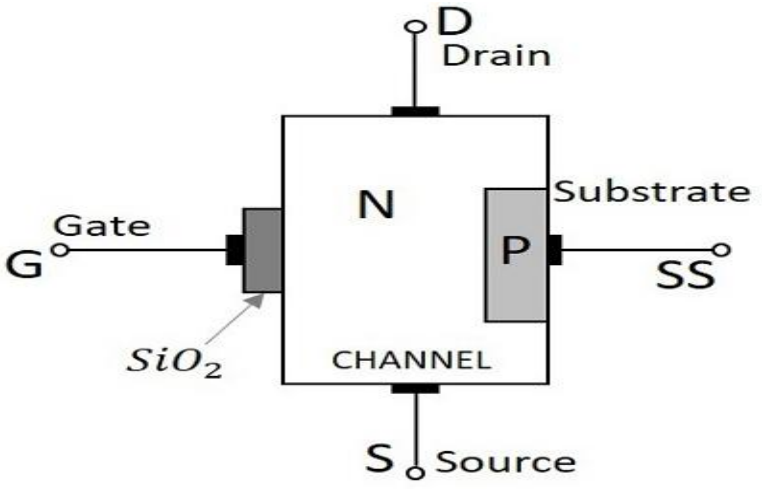

*p*–channel DE MOSFET



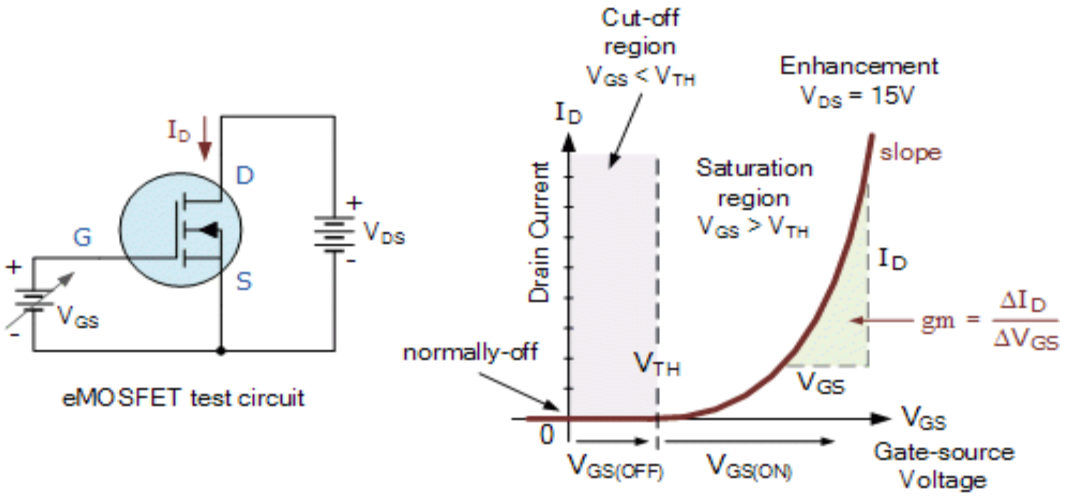

*p*–channel enhancement MOSFET

# Construction of MOSFET

The construction of a MOSFET is a bit similar to the FET. An oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as an insulator ($sio_2$ insulates from the substrate), and hence the MOSFET has another name as IGFET. In the construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region. Depending upon the substrate used, they are called as **P-type** and **N-type** MOSFETs.

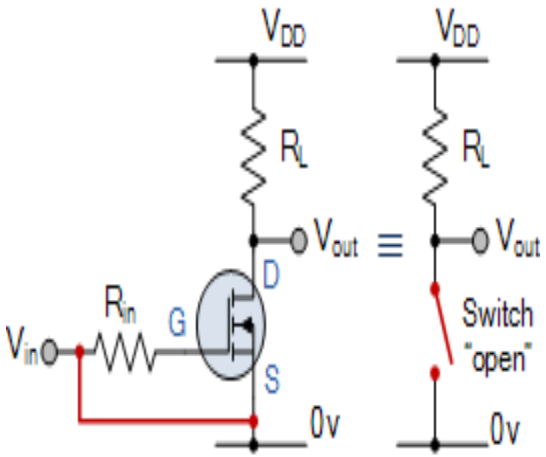


# V-I CHARACTERISTICS OF MOSFET




A **MOSFET** device has three different regions of operation. These regions are called the: Ohmic/Triode region, Saturation/Linear region and Pinch-off point. Therefore if we apply a small AC signal which is superimposed on to this DC bias at the gate input, then the **MOSFET** will act as a linear **amplifier.**

# MOSFET AS SWITCH

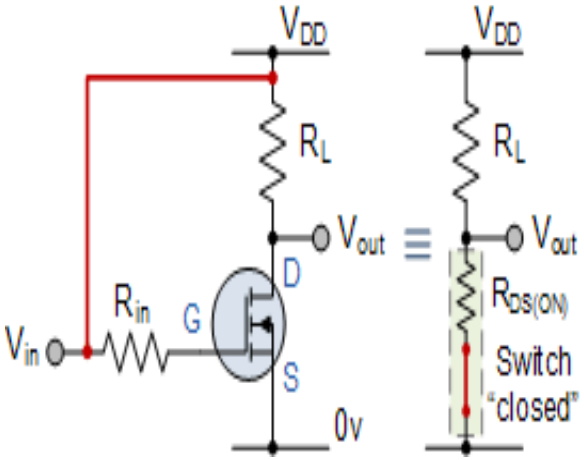



**CUT-OFF CHARACTERIOSTICS:**

The input and Gate are grounded ( 0V )

- Gate-source voltage less than threshold voltage $V_{GS} < V_{TH}$
- MOSFET is “OFF” ( Cut-off region )
- No Drain current flows ( $I_D$ = 0 Amps )
- $V_{OUT} = V_{DS} = V_{DD}$ = ”1”
- MOSFET operates as an “open switch”

# MOSFET AS SWITCH

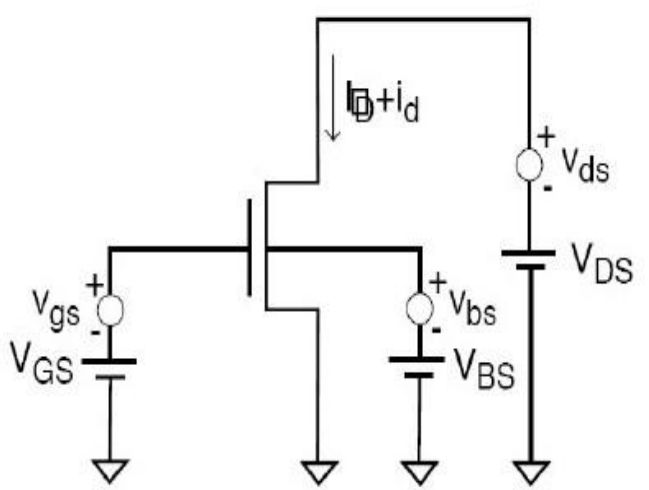


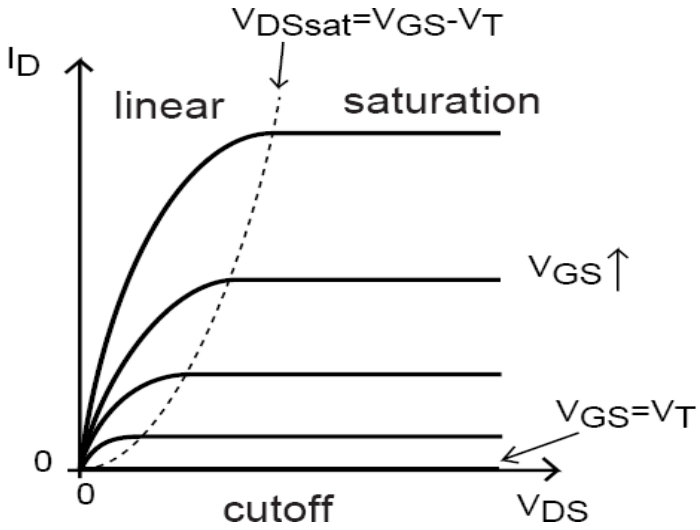

**SATURATION CHARACTERIOSTICS:**

The input and Gate are connected to $V_{DD}$.

- Gate-source voltage is much greater than threshold voltage $V_{GS} > V_{TH}$.
- MOSFET is "ON" ( saturation region )
- Max Drain current flows( $I_D = V_{DD} / R_L$ )
- $V_{DS}$ = 0V (ideal saturation)
- Min channel resistance $R_{DS(on)} < 0.1\Omega$
- $V_{OUT} = V_{DS} \cong 0.2V$ due to $R_{DS(on)}$
- MOSFET operates as a low resistance "closed switch".

# SMALL-SIGNAL OPERATION OF MOSFET



# SMALL-SIGNAL OPERATION OF MOSFET

With id linear on small-signal drives:

$$i_d = g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs}$$

Define: $g_m$ transconductance [S]

$g_o$ output or drain conductance [S]

$g_{mb}$ backgate transconductance [S]

Approach to computing $g_m$, $g_o$, and $g_{mb}$.

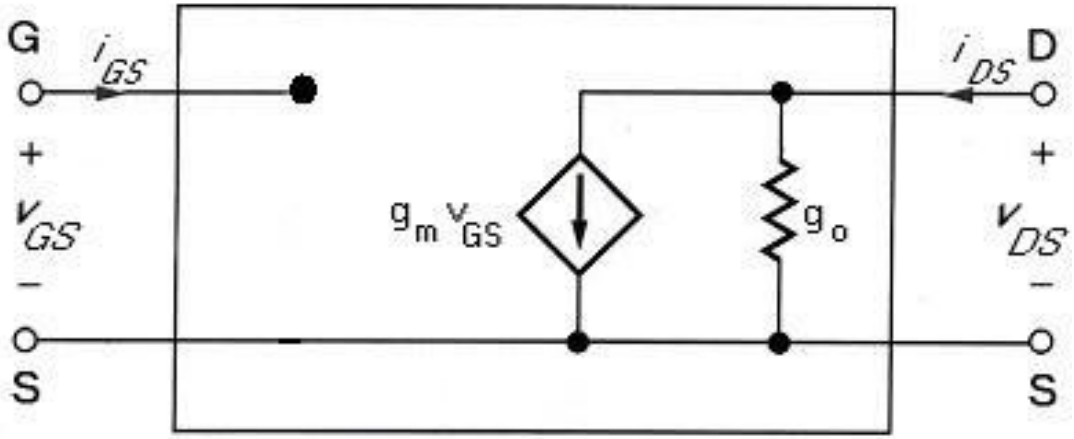
$$g_m \approx \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q$$

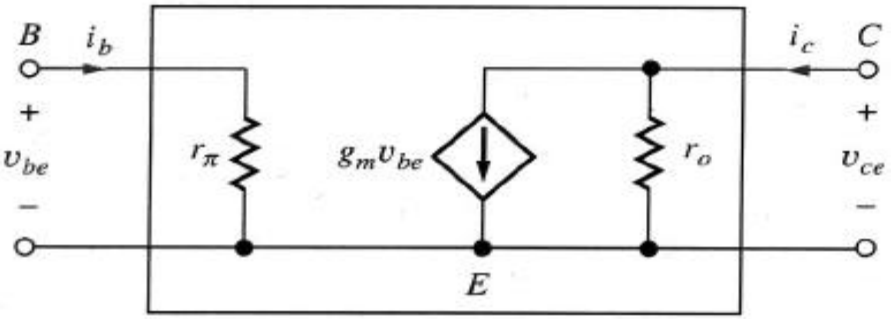
$$g_o \approx \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q$$

$$g_{mb} \approx \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q$$

$$Q \equiv [v_{GS} = V_{GS}, v_{DS} = V_{DS}, v_{BS} = V_{BS}]$$

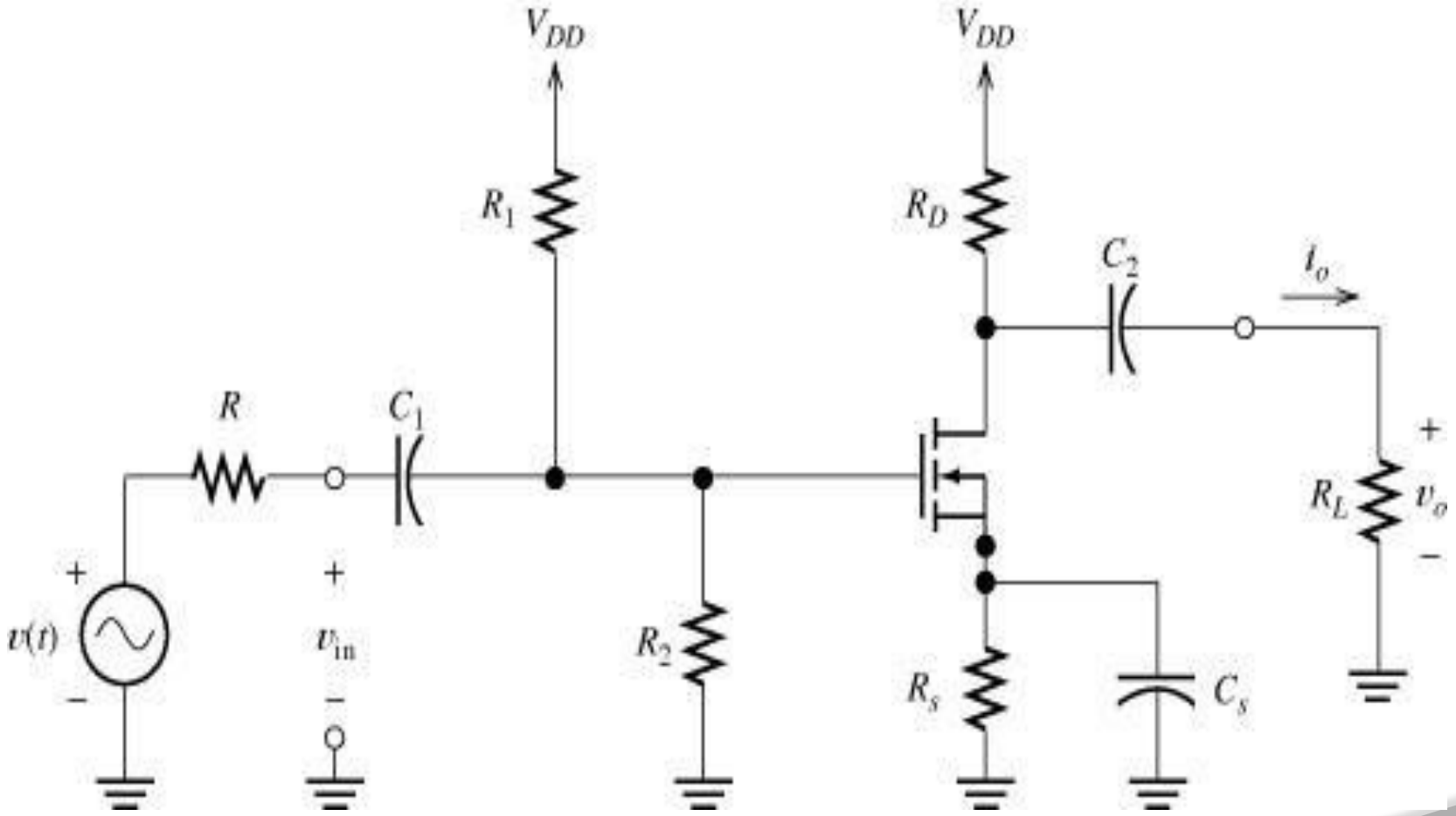
# SMALL-SIGNAL OPERATION OF MOSFET




the BJT small signal equivalent circuit

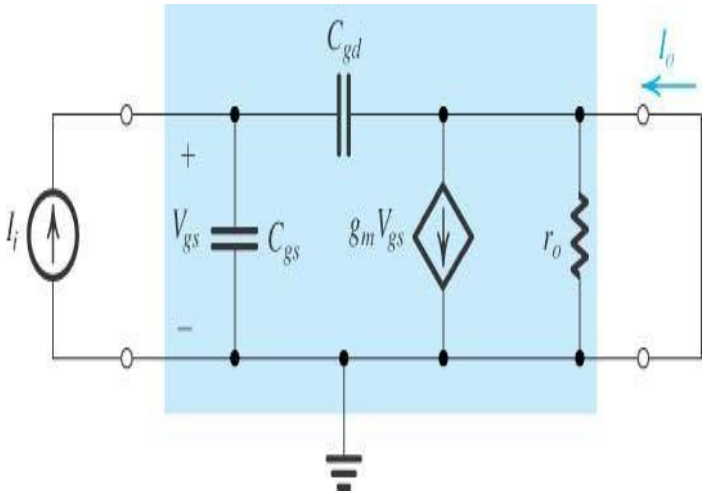
# FET as common source amplifier



# FET as common source amplifier

- In electronics, a **common-source amplifier** is one of three basic single-stage field-effect transistor. FET **amplifier** topologies, typically used as a voltage or transconductance **amplifier**.
- A **common-drain amplifier** is one in which the input signal is applied to the gate and the output is taken from the source, making the **drain common** to both. Because it is **common**, there is no need for a **drain** resistor. A **common-drain amplifier** is also called a source-follower.

# High frequency model of MOSFET

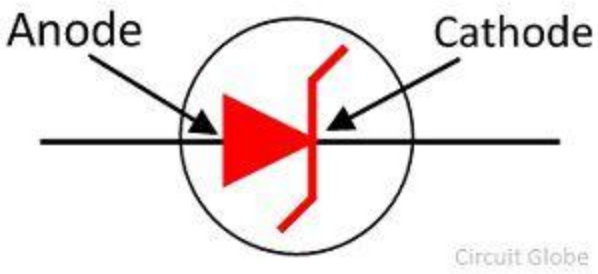


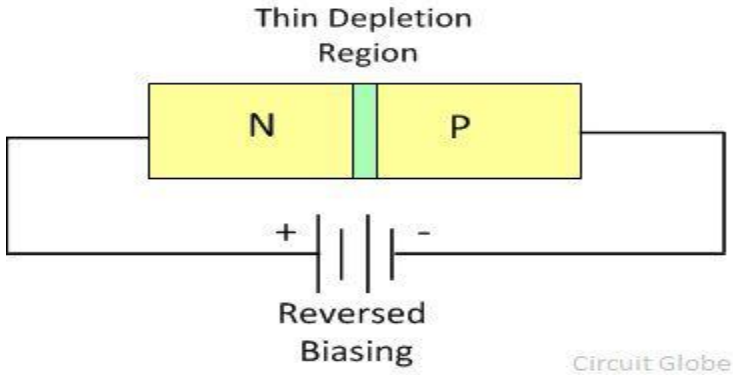

- The MOSFET's internal capacitances limit the high-frequency performance of the MOSFET that means:
- Limit the switching speed of the circuits in digital applications
- Limit the frequency at which useful amplification can be obtained in the amplifiers.

# ZENER DIODE

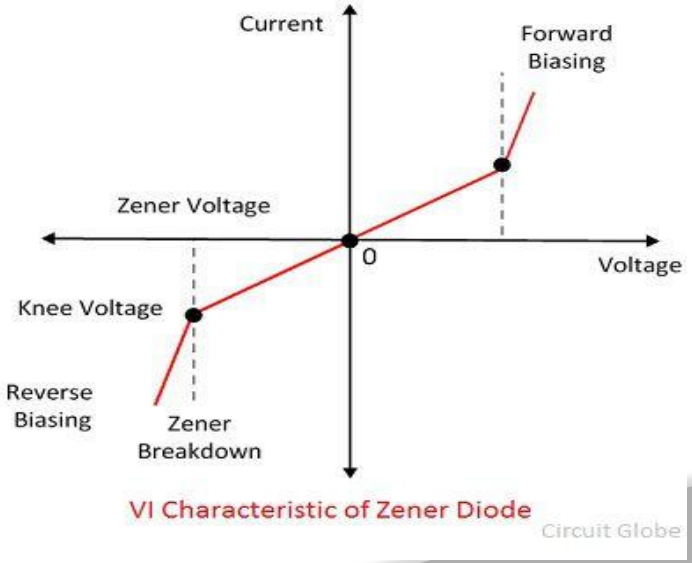
- A heavily doped semiconductor diode which is designed to operate in reverse direction is known as the Zener diode.
- A **Zener diode** is a type of **diode** that allows current to flow not only from its anode to its cathode, but also in the reverse direction, when the **Zener** voltage is reached.
- **Zener diodes** have a highly doped p–n junction.
- When the **diode** is connected in forward bias **diode** acts as a normal **diode**. When the reverse bias voltage is greater than a predetermined voltage then the **Zener** breakdown voltage occurs.

# ZENER DIODE



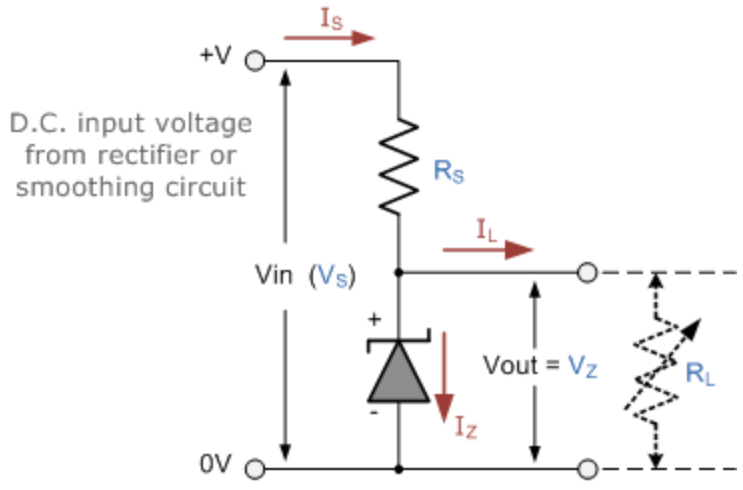




This curve shows that the Zener diode, when connected in forwarding bias, behaves like an ordinary diode. But when the reverse voltage applies across it and the reverse voltage rises beyond the predetermined rating, the Zener breakdown occurs in the diode.



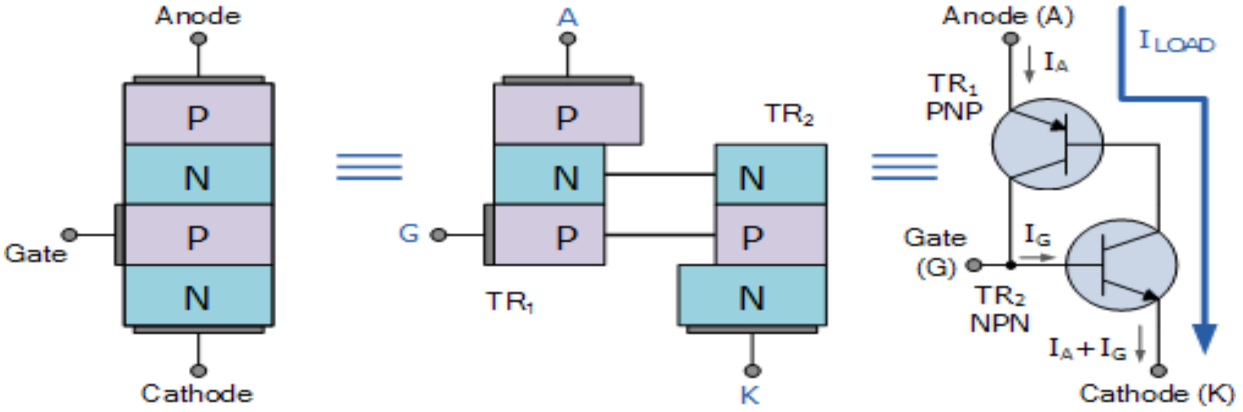
# ZENER DIODE AS VOLTAGE REGULATOR

- A **zener diode** is always operated in its reverse biased condition.
- A **voltage regulator** circuit can be designed using a **zener diode** to maintain a constant DC output voltage across the load in spite of variations in the input voltage or changes in the load current.

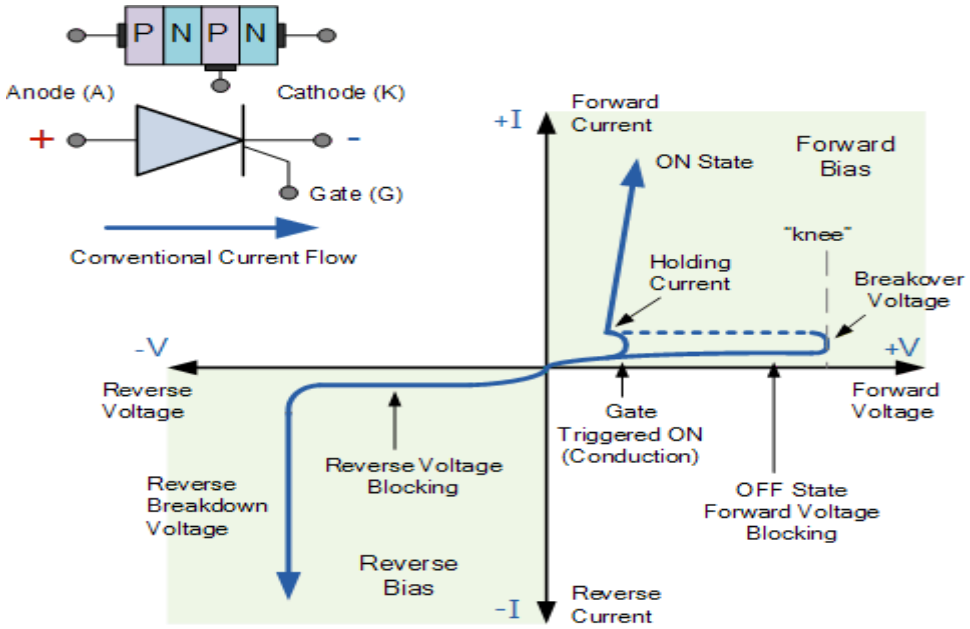


# Principle of operation of SCR

A **Silicon-Controlled Rectifier**, or **SCR**, is essentially a Shockley **diode** with an extra terminal added. This extra terminal is called the gate, and it is used to trigger the device into conduction (latch it) by the application of a small voltage.



# SCR



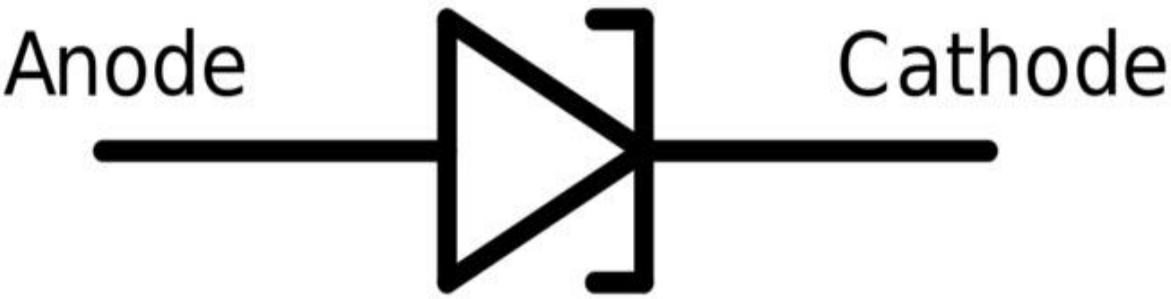

It is a multi-layer semiconductor device, hence the “silicon” part of its name. It requires a gate signal to turn it “ON”, the “controlled” part of the name and once “ON” it behaves like a rectifying diode, the “rectifier” part of the name

# APPLICATIONS OF SCR

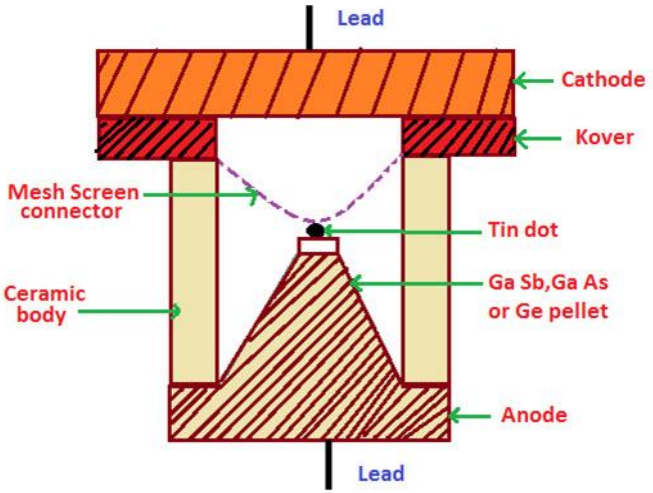
1. AC voltage stabilizers.
2. switch.
3. choppers.
4. inverters.
5. power control.
6. DC circuit breaker.

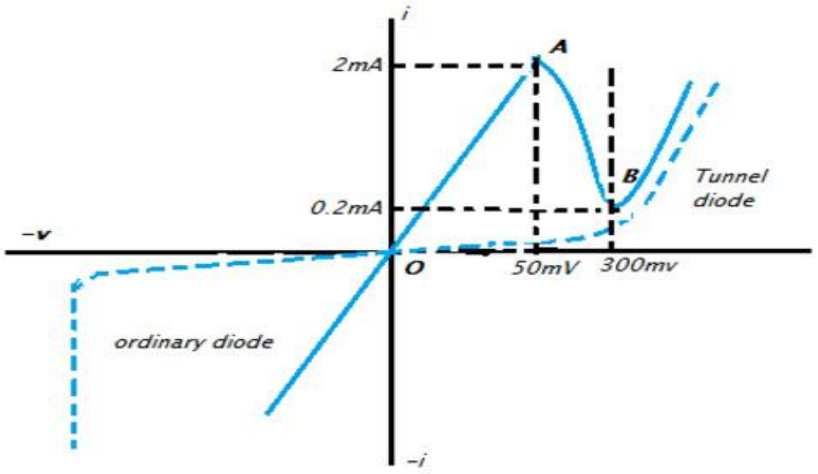
# TUNNEL DIODE

**Tunnel Diode** is the P-N junction device that exhibits negative resistance. When the voltage is increased then the current flowing through it decreases. It works on the principle of **Tunneling** effect.



# TUNNEL DIODE




**Under the forward bias condition**, as voltage increases, then current decreases and thus become increasingly misaligned, known as negative resistance.

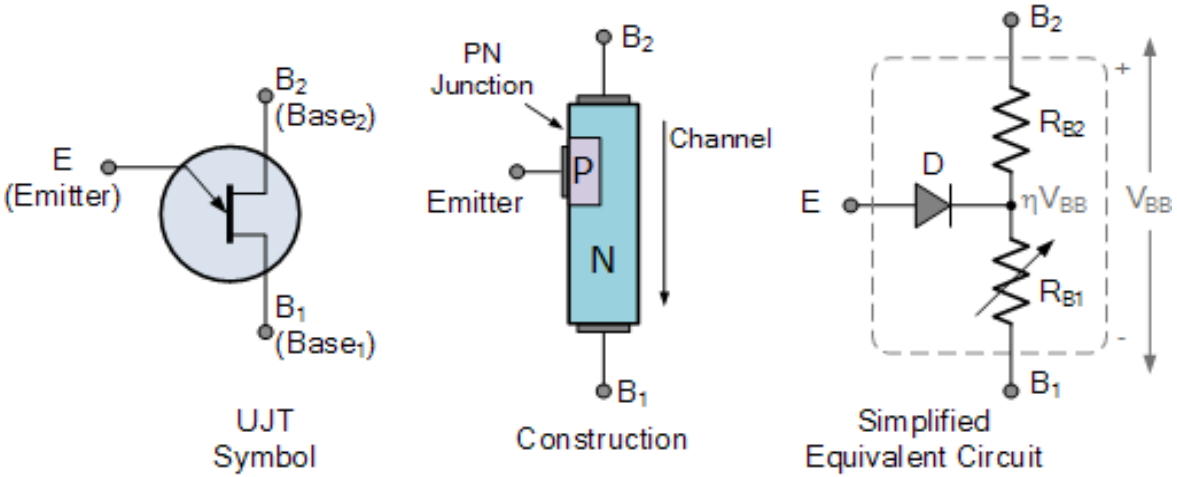
**Under the reverse condition**, the tunnel diode acts as a back diode or backward diode. With zero offset voltage it can act as a fast rectifier.

# APPLICATIONS OF TUNNEL DIODE

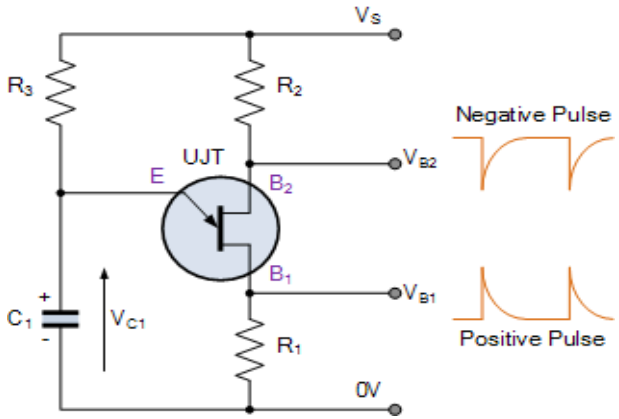
1. Ultra high speed switch.
2. Logic memory storage device.
3. Satellite communication equipment.
4. Relaxation oscillator circuits..
5. FM receivers.
6. Modern military equipment.

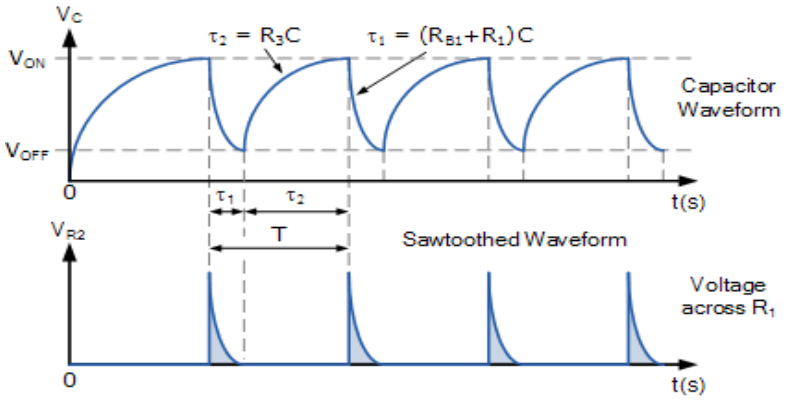
# UNIJUNCTION TRANSISTOR

The UJT is a three-terminal, semiconductor device which exhibits negative resistance and switching characteristics for use as a relaxation oscillator in phase control applications.



# UNI JUNCTION TRANSISTOR




- When a voltage (Vs) is firstly applied, the unijunction transistor is “OFF” and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3.
- As the Emitter of the UJT is connected to the capacitor, when the charging voltage Vc across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The unijunction transistor is “ON”.

# APPLICATIONS OF UJT

1. Relaxation oscillator.
2. Voltage detector.
3. Switching.
4. Silicon control rectifier (SCR) and TRIAC.
5. Phase control circuit.
6. Timing circuit.

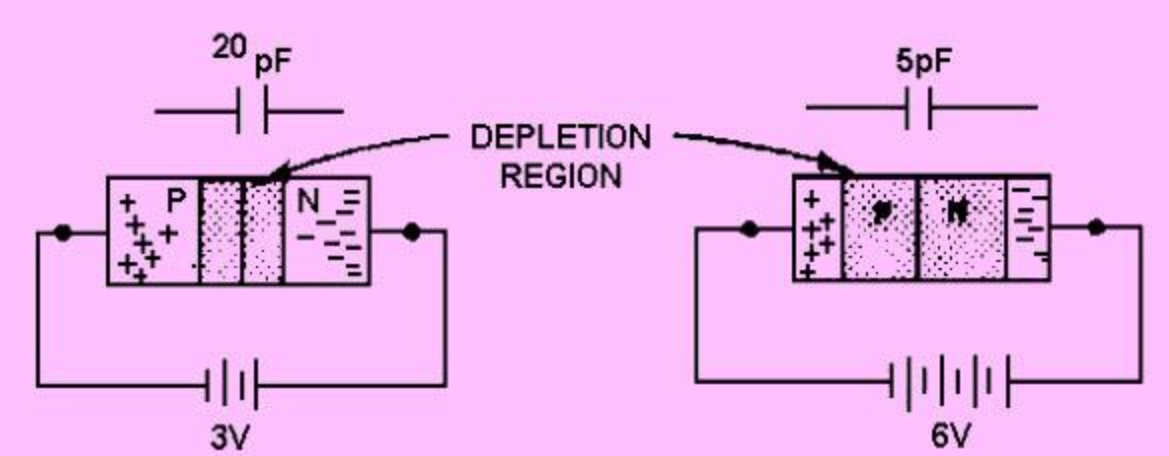
# VARACTOR DIODE

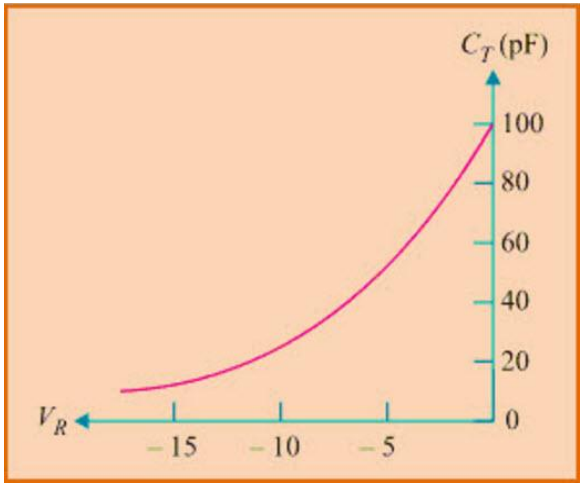
**Varactor diode** is a p-n junction **diode** whose capacitance is varied by varying the reverse voltage.


(a) Electrical Equivalent Circuit of Varactor Diode (b) Symbol of Varactor Diode

**Varactor Diode** is a reverse biased p-n junction diode, whose capacitance can be varied electrically. As a result these diodes are also referred to as varicaps, tuning diodes, voltage variable capacitor diodes, parametric diodes and variable capacitor diodes.

# VARACTOR DIODE




- These diodes significantly generate less noise compared to other diodes.
- The cost of these diodes is available at lower and more reliable also.
- These diodes are very small in size and very light weight.
- There is no useful when it is operated in forward bias.
- In reverse bias mode, Varactor diode enhances the capacitance.

# APPLICATIONS OF VARACTOR DIODE

- Microwave circuits.
- Tank circuits.
- Automatic frequency controller.
- Frequency modulator.
- RF phase shifter.