INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTEGRATED CIRCUITS APPLICATIONS**				
Course Code	AEC008				
Programme	B.Tech				
Semester	V	ECE | EEE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	3	2
Chief Coordinator	Ms. J Sravana, Assistant Professor				
Course Faculty	Ms. G Ajitha, Assistant Professor Ms. N Anusha, Assistant Professor Mr. S Lakshmanachari, Assistant professor Ms. P Saritha, Assistant Professor Ms. KS Indrani, Assistant Professor				

I. COURSE OVERVIEW:

Integrated Circuits design can be divided into the broad categories of digital and analog IC design. The physical world is inherently analog indicating that there is always need for analog circuitry. Today the growth of any industry is dependent upon electronics to a great extent. Integrated circuit is electronics and this course IC application acquaints the students with general analog principles and design methodologies using practical devices and applications. It focus on process of learning about signal condition, signal generation, instrumentation, timing and control using various IC circuitry. With modern digitization advantages we need to work with digital data and hence digital ICs play a crucial role in connecting physical world to the more sophisticated digital world. This course focuses on analysis, design and applications of modern digital integrated circuits.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC001	III	Electronic Devices and Circuits	4
UG	AEC006	IV	Pulse and Digital Circuits	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Integrated Circuits Applications	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE):

The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each unit. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz / Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Quiz / AAT	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars, assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Lectures and Assignments
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Assignments
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Lab related Exercises
PO 12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	2	Seminars

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications,	2	Lectures and Assignments

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
	Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.		
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	-	-
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Be acquainted to principles and characteristics of op-amp and apply the techniques for the design of comparators, instrumentation amplifier, integrator, differentiator, multivibrators, waveform generators, log and anti-log amplifiers.
II	Analyze and design filters, timer, analog to digital and digital to analog Converters.
III	Understand the functionality and characteristics of commercially available digital integrated circuits.

IX. COURSE OUTCOMES (COs):

COs	Course Outcomes	CLO's	Course Learning Outcome
CO1	Discuss the analysis of Op-Amp for different configurations and its properties.	CLO 1	Illustrate the block diagram, classifications, package types, temperature range, specifications and characteristics of Op-Amp.
		CLO 2	Discuss various types of configurations in differential amplifier with balanced and unbalanced outputs.
		CLO 3	Evaluate DC and AC analysis of dual input balanced output configuration and discuss the properties of differential amplifier and discuss the operation of cascaded differential amplifier.
CO2	Analyze and design the linear and non linear applications of Op-Amp	CLO 4	Analyze and design linear applications like inverting amplifier, non-inverting amplifier, instrumentation amplifier and etc. using Op-Amp.

COs	Course Outcomes	CLO's	Course Learning Outcome
		CLO 5	Analyze and design non linear applications like multiplier, comparator, log and anti log amplifiers, waveform generators and etc, using Op-Amp.
CO3	Design the various filters using Op-Amp and analysis of Multivibrators using 555 Timer	CLO 6	Discuss various active filter configurations based on frequency response and construct using 741 Op-Amp.
		CLO 7	Design bistable, monostable and astable multivibrators operation by using IC 555 timer and study their applications.
		CLO 8	Determine the lock range and capture range of PLL and use in various applications of communications.
CO4	Describe the various ADC and DAC techniques	CLO 9	Understand the classifications, characteristics and need of data converters such as ADC and DAC.
		CLO 10	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC.
		CLO 11	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters.
CO5	Explore the concepts of Combinational and sequential logic circuits using digital IC's	CLO 12	Design adders, multiplexers, demultiplexers, decoders, encoders by using TTL/CMOS integrated circuits and study the TTL and CMOS logic families.
		CLO 13	Design input/output interfacing with transistor – transistor logic or complementary metal oxide semiconductor integrated circuits.
		CLO 14	Understand the operation of SR, JK, T and D flip-flops with their truth tables and characteristic equations. Design TTL/CMOS sequential circuits.
		CLO 15	Design synchronous, asynchronous and decade counter circuits and also design registers like shift registers and universal shift registers.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
AEC008.01	CLO 1	Illustrate the block diagram, classifications, package types, temperature range, specifications and characteristics of Op-Amp.	PO 1 PO 2	2
AEC008.02	CLO 2	Discuss various types of configurations in differential amplifier with balanced and unbalanced outputs.	PO 1 PO 2	2
AEC008.03	CLO 3	Evaluate DC and AC analysis of dual input balanced output configuration and discuss the properties of differential amplifier and discuss the operation of cascaded differential amplifier.	PO 1	3
AEC008.04	CLO 4	Analyze and design linear applications like inverting amplifier, non-inverting amplifier, instrumentation amplifier and etc. using Op-Amp.	PO 5	2
AEC008.05	CLO 5	Analyze and design non linear applications like multiplier, comparator, log and anti log amplifiers, waveform generators and etc, using Op-Amp.	PO 2	2
AEC008.06	CLO 6	Discuss various active filter configurations based on frequency response and construct using 741 Op-Amp.	PO 5	3
AEC008.07	CLO 7	Design bistable, monostable and astable multivibrators operation by using IC 555 timer and study their applications.	PO 1	3
AEC008.08	CLO 8	Determine the lock range and capture range of PLL and use in various applications of communications.	PO 1	2
AEC008.09	CLO 9	Understand the classifications, characteristics and need of data converters such as ADC and DAC.	PO 1	2
AEC008.10	CLO 10	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC.	PO 1	3
AEC008.11	CLO 11	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters.	PO 1	1
AEC008.12	CLO 12	Design adders, multiplexers, demultiplexers, decoders, encoders by using TTL/CMOS integrated circuits and study the TTL and CMOS logic families.	PO 5	1

CLO Code	CLOs	At the end of the course, the student will have the ability to:	POs Mapped	Strength of Mapping
AEC008.13	CLO 13	Design input/output interfacing with transistor – transistor logic or complementary metal oxide semiconductor integrated circuits.	PO 1 PO 12	2
AEC008.14	CLO 14	Understand the operation of SR, JK, T and D flip-flops with their truth tables and characteristic equations. Design TTL/CMOS sequential circuits.	PO 1	3
AEC008.15	CLO 15	Design synchronous, asynchronous and decade counter circuits and also design registers like shift registers and universal shift registers.	PO 1	3

3 = High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)				Program Specific Outcomes(PSOs)		
	PO1	PO2	PO5	PO12	PSO1	PSO2	PSO3
CO 1	2			1	1		
CO 2	2	2	1	1	2		
CO 3	1	2		1			
CO 4		1	2	1	1		
CO 5		2		2	1		

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XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes	Program Outcomes (Pos)												Program Specific Outcomes(PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	2	2											1		
CLO 2	2	2											1		
CLO 3	3												1		
CLO 4					2										
CLO 5		2											3		

Course Learning Outcomes	Program Outcomes (Pos)												Program Specific Outcomes(PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 6					3										
CLO 7	3														
CLO 8	2														
CLO 9	2												1		
CLO 10	3												1		
CLO 11	1														
CLO 12					1										
CLO 13	2											2			
CLO 14	3												1		
CLO 15	3														

3 = High; 2 = Medium; 1 = Low

XIII. ASSESSMENT METHODOLOGIES – DIRECT:

CIE Exams	PO1, PO2 PO5,PO12, PSO 1	SEE Exams	PO1, PO2 PO5,PO12, PSO 1	Assignments	PO1, PO2	Seminars	PO 12
Laboratory Practices	PO 5	Student Viva	–	Mini Project	–	Certification	–
Term Paper	PO1, PO2 PO5,PO12, PSO 1						

XIV. ASSESSMENT METHODOLOGIES – INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects By Experts		

XV. SYLLABUS

Unit-I	INTEGRATED CIRCUITS:
Integrated Circuits: Classification of integrated circuits, Package types and temperature ranges; Differential Amplifier: DC and AC analysis of Dual input Balanced output Configuration; Properties of differential amplifier configuration: Dual Input Unbalanced Output, Single Ended Input, Balanced/ Unbalanced Output; DC Coupling and Cascade Differential Amplifier Stages, Level translator. Characteristics of OP-Amps: Op-amp Block Diagram, ideal and practical Op-amp specifications, DC	

and AC characteristics, 741 op-amp & its features; Op-Amp parameters & Measurement: Input & Out put Off set voltages & currents, slew rate, CMRR, PSRR, and Drift.	
Unit-II	**APPLICATIONS OF OP-AMPS:**
Linear applications of Op- Amps: Inverting and non-inverting amplifier, integrator, differentiator, instrumentation amplifier, AC amplifier; Non-linear applications of Op-Amps: Comparators, multivibrators, triangular and square wave generators, non- linear function generation, log and anti log amplifiers.	
Unit-III	**ACTIVE FILTERS AND TIMERS:**
Active Filters: Classification of filters, 1st order low pass and high pass filters, 2 nd order low pass, high pass, band pass, band reject and all pass filters. Timers: Introduction to 555 timer, functional diagram, monostable, astable operations and applications, Schmitt Trigger; PLL: Introduction, block schematic, principles and description of individual blocks, 565 PLL.	
Unit-IV	**DATA CONVERTERS:**
Data converters: Introduction, classification, need of data converters; DAC techniques: Weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, and IC 1408 DAC, DAC characteristics; ADC techniques: Integrating, successive approximation, flash converters, A/D characteristics.	
Unit-V	**DIGITAL IC APPLICATIONS:**
Combinational Design Using TTL/ CMOS ICs: Logic delays, TTL/CMOS interfacing, adders, multiplexer, demultiplexer, decoder, encoder; Sequential design using TTL/ CMOS ICs: SR, JK, T, and D flip-flops; Counters: Synchronous and asynchronous counters, decade counter; Registers: Shift registers, universal shift register, Ring counters and Johnson counters.	
Text Books:	
1. D. Roy Chowdhury ―Linear Integrated Circuits‖, New age international (p) Ltd, 2nd Edition, 2003. 2. Ramakanth A. Gayakwad ―Op-Amps & linear ICs‖, PHI, 3rd Edition, 2003. 3. John F. Wakerly ―Digital Design Principles and Practices‖, Prentice Hall, 3rd Edition, 2005.	
Reference Books:	
1. Salivahanan ―Linear Integrated Circuits and Applications‖, TMH, 1st Edition, 2008. 2. S P Bali ―Linear Integrated Circuits‖, TMH, 1st Edition, 2008.	

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes	Reference
1 - 3	Discuss the classification of integrated circuits, Package types, temperature ranges and Differential amplifier configurations.	CLO 1	T1:2.2 T2:1.2-1.7

Lecture No	Topics to be covered	Course Learning Outcomes	Reference
4 - 6	Analyze DC and AC analysis of various configuration of Differential amplifier.	CLO 3	T1:2.5 R1:3.4
7 - 8	Understand differential amplifier stages.	CLO 2	T1:2.4
9 - 10	Understand the DC characteristics of op-amp.	CLO 3	T2:1.12-1.13
11 - 12	Understand the AC characteristics of op-amp.	CLO 3	T1:3.2
13 - 15	Discuss op-amp parameters & measurements.	CLO 3	T1:3.3-3.4
16 - 18	Illustrate the linear applications of op-amp.	CLO 4	T1:2.3 R2:12.7
19 - 21	Illustrate the non linear applications of op-amp.	CLO 5	T1:11.1-11.5
22 - 26	Derive and analyze 1st order and 2nd order filters.	CLO 6	T1:4.8
27 - 28	Derive and analyze various types of filters.	CLO 6	T1:7.2
29 - 30	Understand the operation of 555 timer and discuss the operation.	CLO 7	T1:7.2
31- 34	Summarize the operation and applications of multivibrators using 555 timer.	CLO 7	T2:10.4 R2:7.2
35-39	Understand the operation of 565 PLL and discuss the operation.	CLO 8	T1:8.2-8.5
40	Discuss the classifications of data converters.	CLO 9	T1:9.2-9.7
41 - 42	Discuss and Analyze DAC techniques and characteristics.	CLO 10	T1:10.1
43 - 45	Discuss and Analyze ADC techniques and characteristics.	CLO 11	T1:10.2
46 - 47	Design and analyze the combinational circuits using TTL/CMOS logic.	CLO 12	T1:10.3 R2:5.4
48 - 50	Design and analyze the sequential circuits using TTL/CMOS logic.	CLO 14	T3:3.12 R2:12.7
51 - 54	Design and analyze different types of counters.	CLO 15	T3:7.2
55 - 60	Design and analyze different types of registers.	CLO 15	T3:8.4

XVII. GAPS IN THE SYLLABUS - TO MEET INDUSTRY/PROFESSION REQUIREMENTS:

S.No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Design a FET differential amplifier with swamping resistors for dual input balanced output differential amplifier with emitter resistance R_E.	Seminars	PO 1	PSO 1
2	Design and analyze the voltage series negative feedback amplifier and find the voltage gain, input and output resistances, and total output offset voltage with feedback.	Seminars / NPTEL	PO 2	PSO 1
3	Encourage students to solve real time applications and prepare towards competitive examinations.	NPTEL	PO 2	PSO 1

Prepared by:
Ms. J Sravana, Assistant Professor

HOD, ECE