

PPTs

INTEGRATED CIRCUIT APPLICATIONS

III B.Tech V semester
(Autonomous R16)
(2019-20)



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ELECTRICAL AND ELECTRONICS ENGINEERING



Unit-I

INTEGRATED CIRCUITS

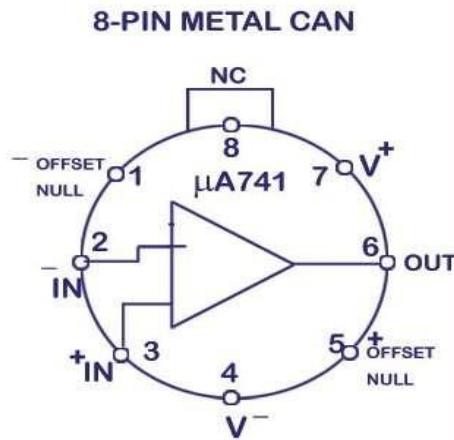


Package types and temperature ranges

The IC packages are classified as,

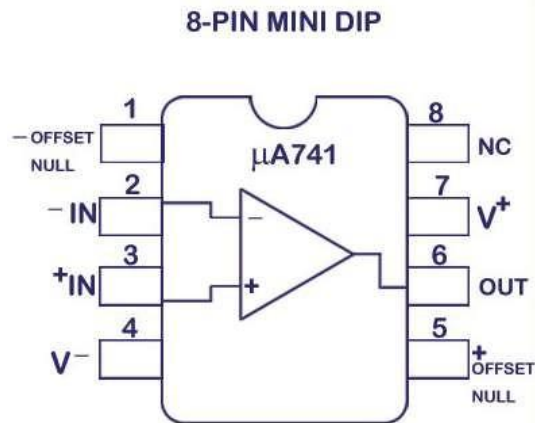
- Metal Can
- Dual In Line
- Flat Pack

❖ Metal Can



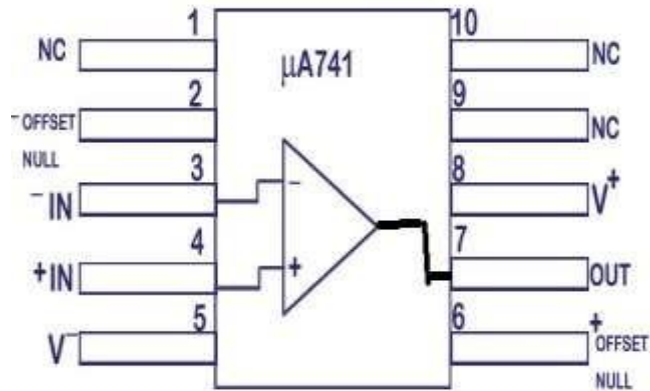
Package types and temperature ranges

❖ Dual- In-Line package



Package types and temperature ranges

10-PINFLATPAK

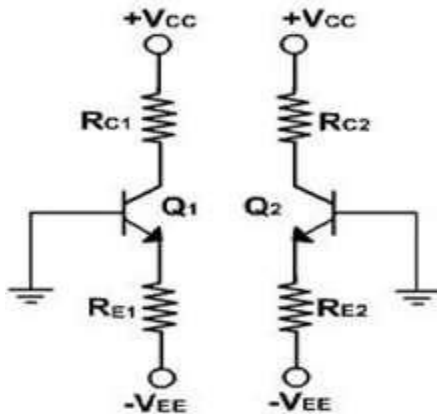


Package types and temperature ranges

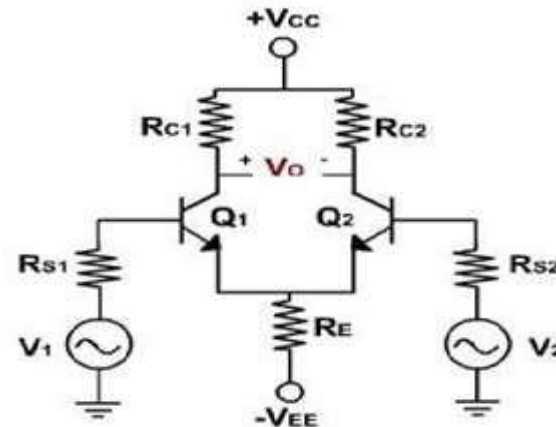
- Military temperature range : -55°C to +125°C (-55°C to +85°C)
- Industrial temperature range : -20°C to +85°C (-40°C to +85°C)
- Commercial temperature range: 0°C to +70°C (0°C to +75°C)

Differential amplifier

A **differential amplifier** is a type of electronic **amplifier** that amplifies the **difference** between two input voltages but suppresses any voltage common to the two inputs. It is an analog **circuit** with two inputs and one output in which the output is ideally proportional to the **difference** between the two voltages.



Two identical emitter biased circuits



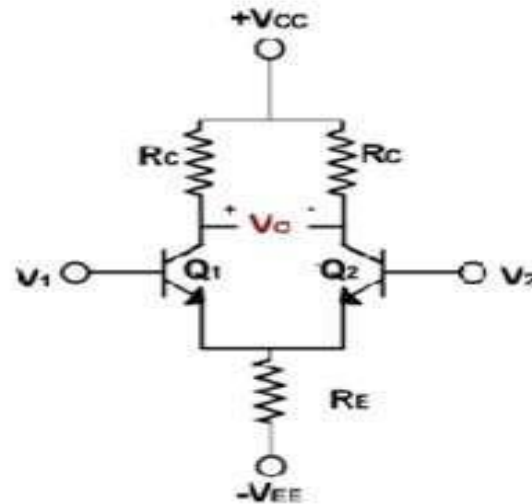
Dual i/p, balanced o/p differential amplifier

Differential amplifier configurations

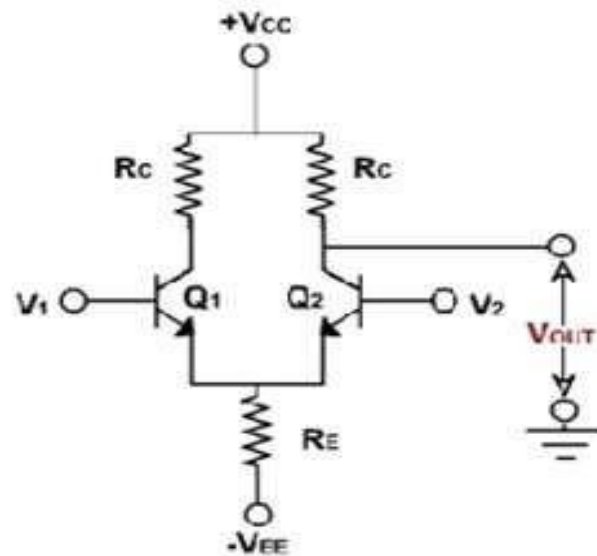
The four differential amplifier configurations are :

- Dual input, balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier.
- Single input balanced output differential amplifier.
- Single input unbalanced output differential amplifier.

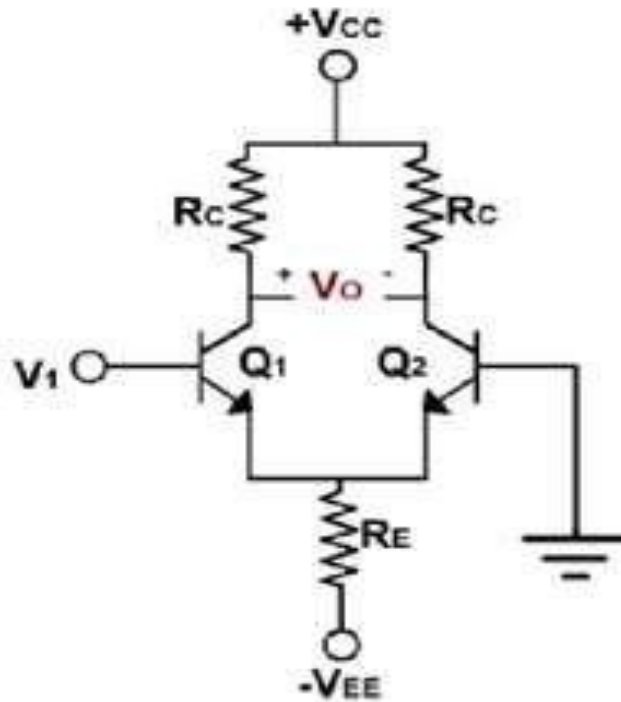
Dual i/p, balanced o/p differential amplifier



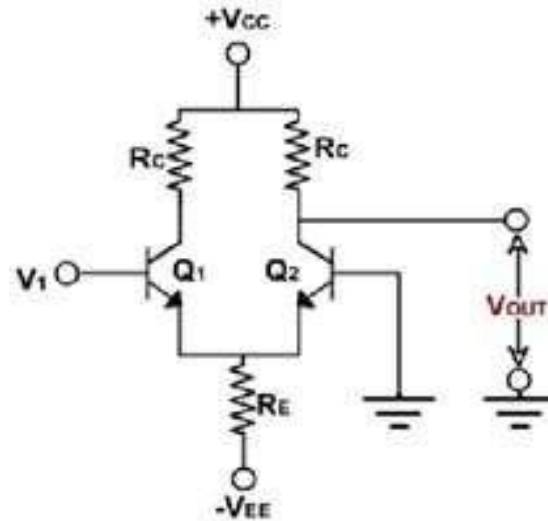
Dual i/p, unbalanced o/p differential amplifier



Single i/p, balanced o/p differential amplifier

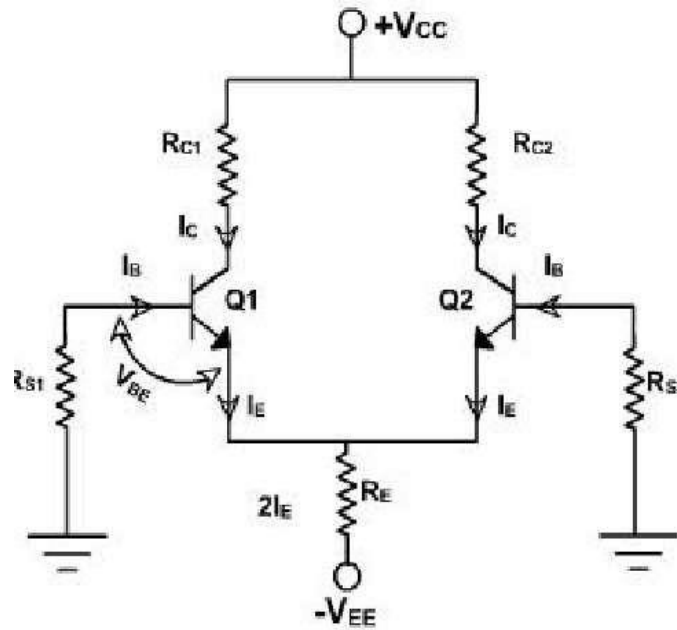


Single i/p, unbalanced o/p differential amplifier



Dual i/p, balanced o/p - DC analysis

Dual i/p, balanced o/p DC - analysis



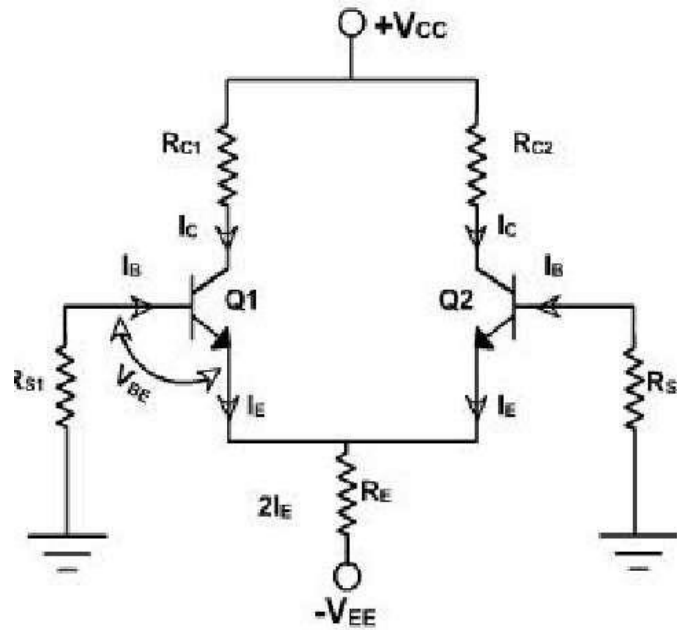
DC equivalent circuit

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CEQ} = V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

Dual i/p, balanced o/p - DC analysis

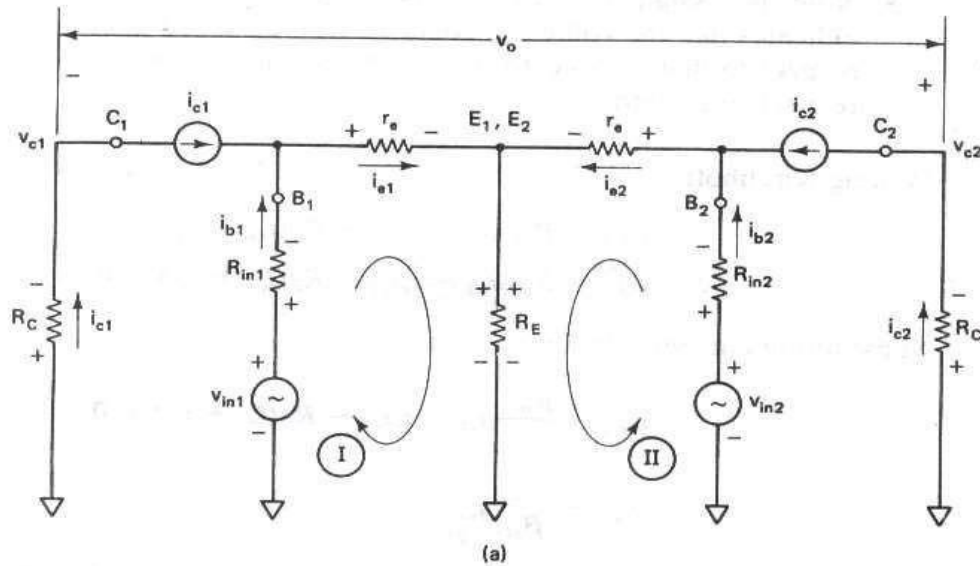
Dual i/p, balanced o/p - DC analysis



$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

Dual i/p, balanced o/p - AC analysis

Dual i/p, balanced o/p - AC analysis

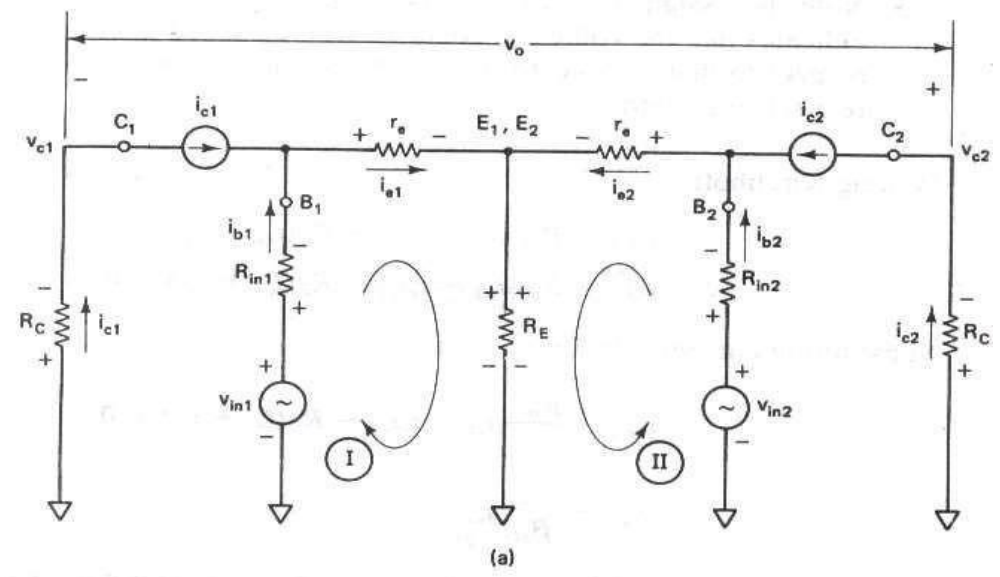


AC Equivalent circuit

Voltage gain, $A_d = R_C / r_e$

Dual i/p, balanced o/p - AC analysis

Dual i/p, balanced o/p - AC analysis

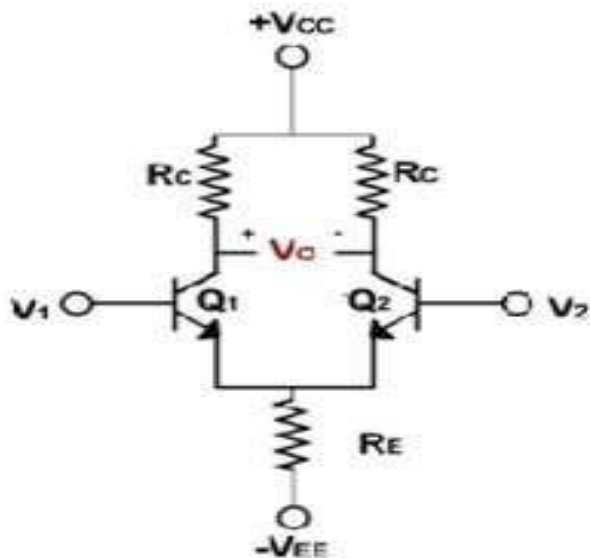


AC Equivalent circuit

Voltage gain,

$$A_d = R_C / r_e$$

❖ Dual i/p and balanced o/p configuration



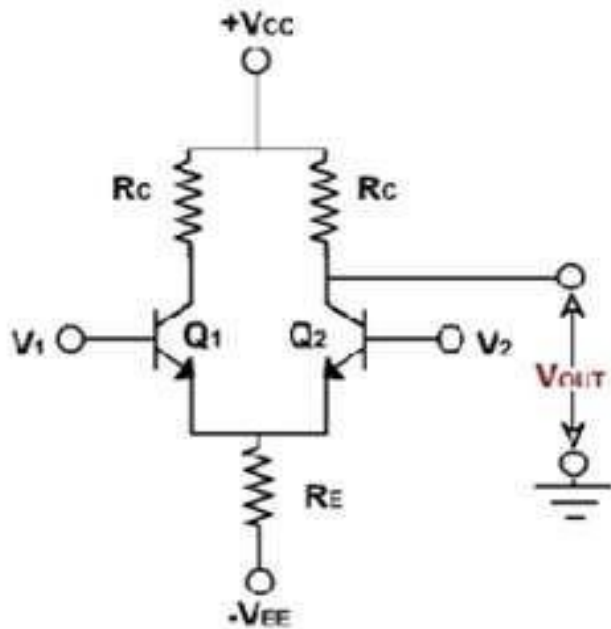
Voltage Gain, $A_d = R_C/r_e$

I/P Resistance, $R_{i1} = R_{i2} = 2\beta_{ac}r_e$

O/P Resistance, $R_{o1} = R_{o2} = R_C$

Properties of differential amplifier

❖ Dual i/p and unbalanced o/p differential amplifier



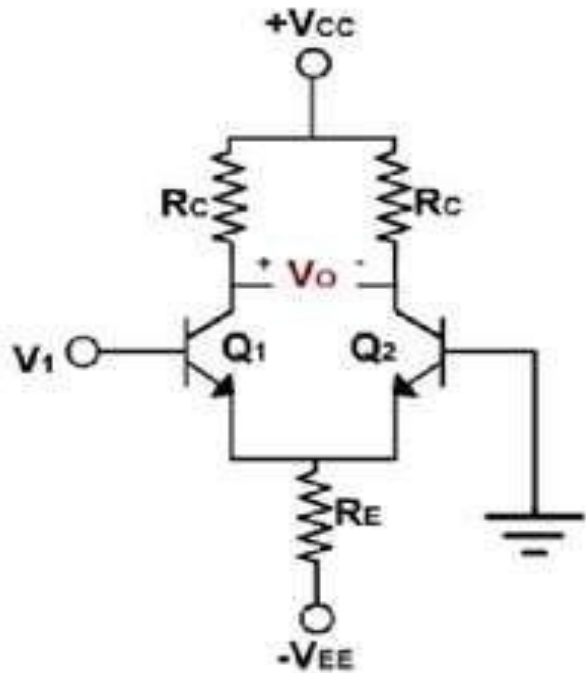
Voltage Gain, $A_d = R_C/2r_e$

I/P Resistance, $R_{i1} = R_{i2} = 2\beta_{ac}r_e$

O/P Resistance, $R_o = R_C$

Properties of differential amplifier

- ❖ Single i/p and balanced o/p configuration

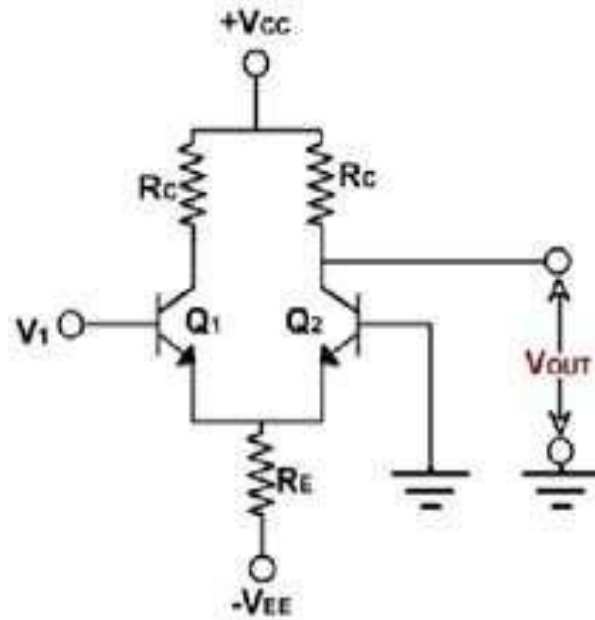


Voltage Gain, $A_d = R_C/r_e$

I/P Resistance, $R_i = 2\beta_{ac}r_e$

O/P Resistance, $R_{o1} = R_{o2} = R_C$

Properties of differential amplifier

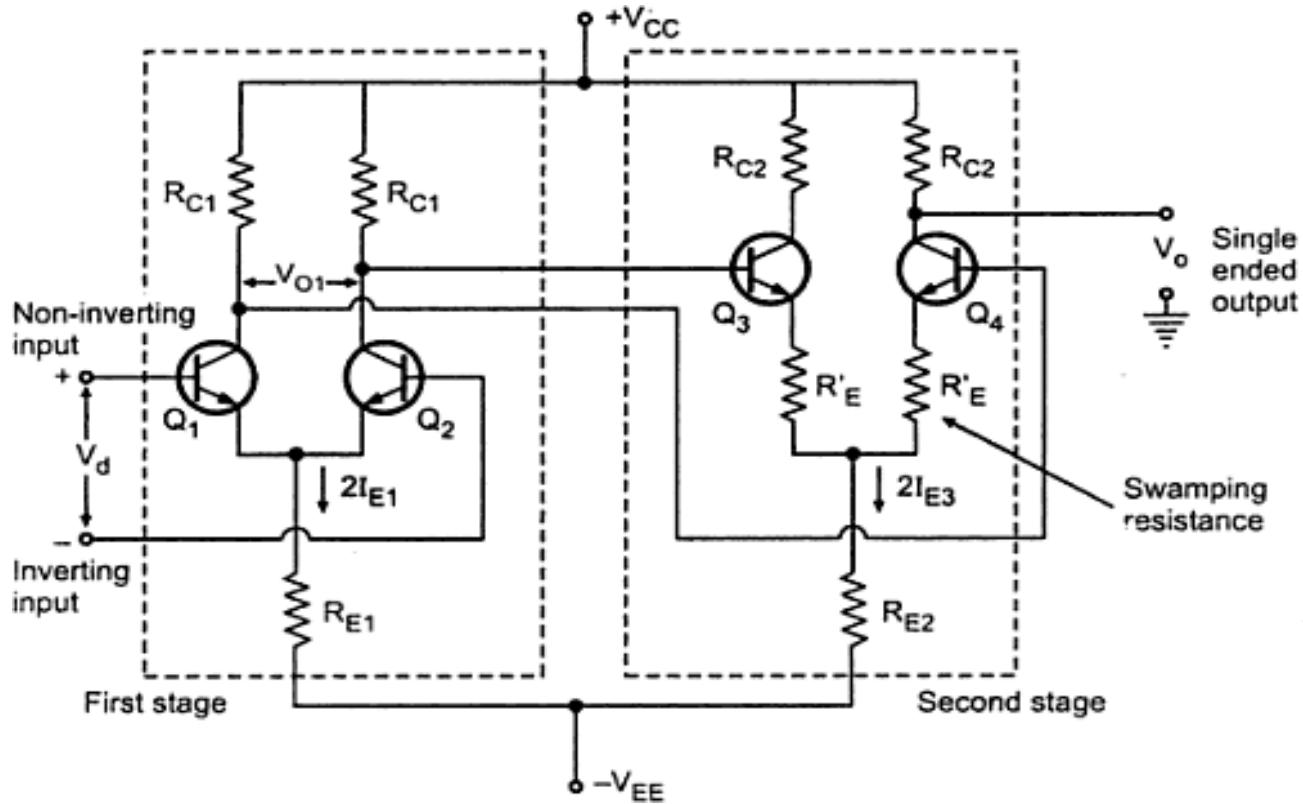


Voltage Gain, $A_d = R_C/2r_e$

I/P Resistance, $R_i = 2\beta_{ac}r_e$

O/P Resistance, $R_o = R_C$

Cascade Differential Amplifier



Level Translator

Level Translator

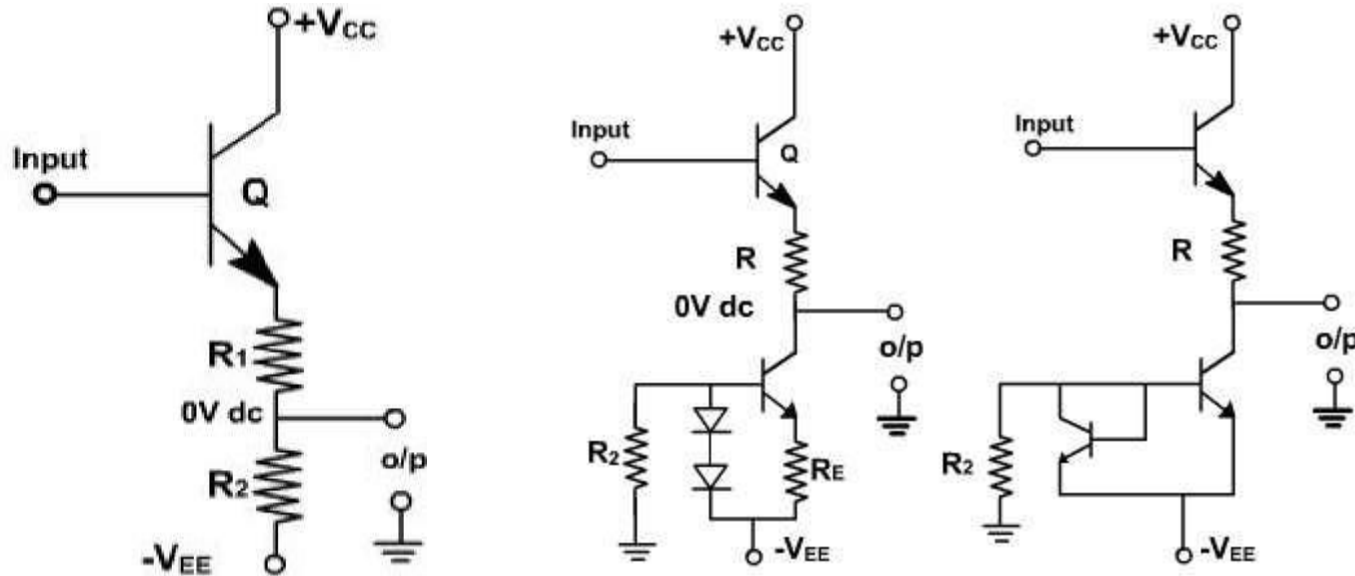
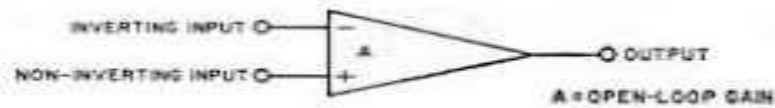
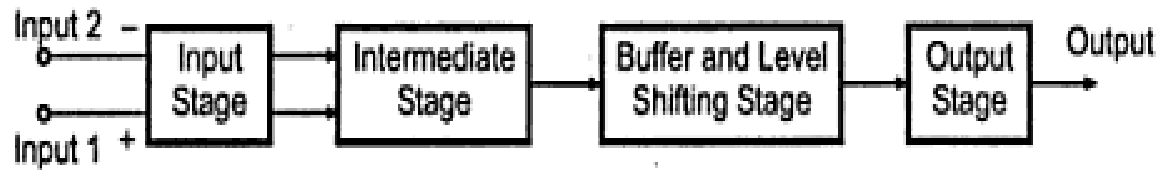


Fig: a) Common collector Amplifier with voltage divide b) Emitter follower with constant current bias c) Emitter follower with current mirror

Op-Amp block diagram & specifications

Op-Amp block diagram & specifications

❖ Op-amp Block Diagram



Ideal Op-Amp specifications:

- The input resistance R_{IN} would be infinite
- The output resistance R_{OUT} would be zero
- The voltage gain, V_G would be infinite
- The bandwidth (how quickly the output will follow the input) would be infinite
- If the voltages on the two inputs are equal than the output voltage is zero (If the output is not zero it is said to have an offset)

❖ Practical OP-AMP characteristics

- The open loop gain of practical Op – Amp is around 7000.
- Practical Op – Amp has non zero offset voltage. That is, the zero output is obtained for the non – zero differential input voltage only.
- The bandwidth of practical Op – Amp is very small value. This can be increased to desired value by applying an adequate negative feedback to the Op – Amp.

❖ Practical Op-Amp specifications

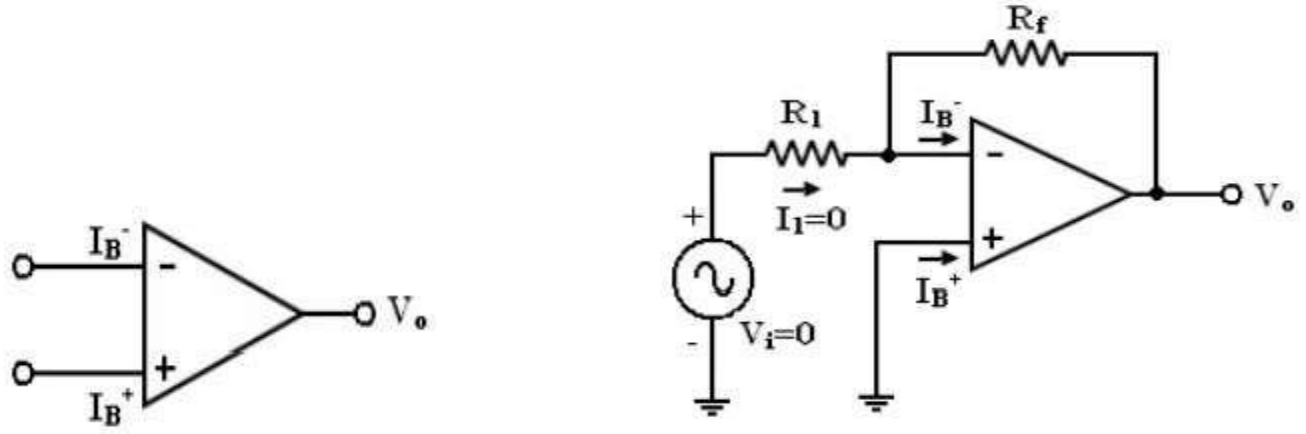
- The output impedance is in the order of hundreds. This can be minimized by applying an adequate negative feedback to the Op – Amp.
- The input impedance is in the order of Mega Ohms only. (Whereas the ideal Op – Amp has infinite input impedance).

DC Characteristics of Op-Amp

DC Characteristics of Op-Amp

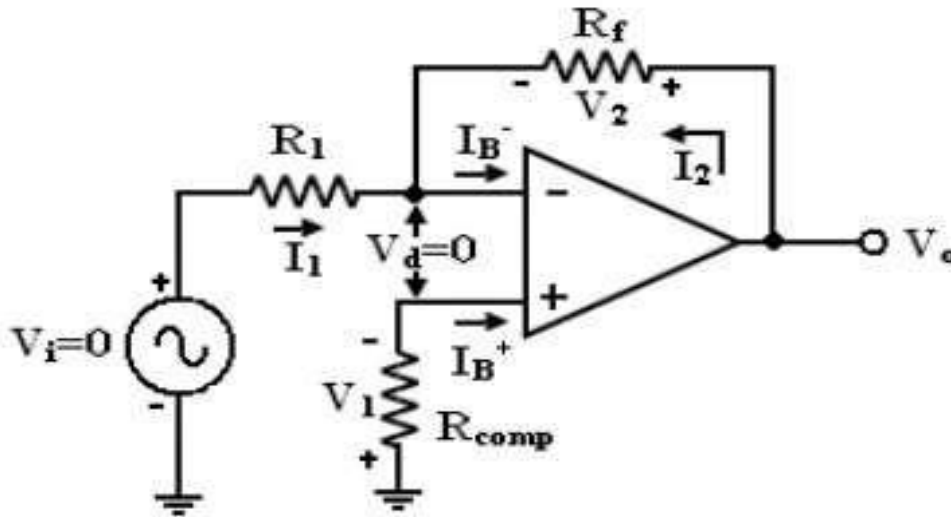
- ❖ Input bias current
- ❖ Input offset current
- ❖ Input offset voltage
- ❖ Thermal drift

DC Characteristics of Op-Amp



$$I_B = (I^+ + I^-) / 2 \quad \text{and}$$

DC Characteristics of Op-Amp

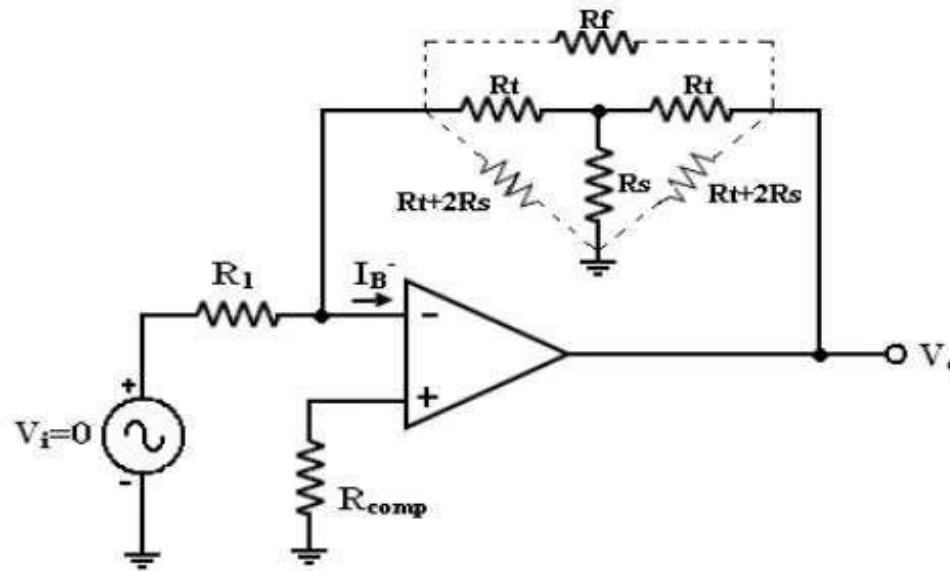


$$R_{\text{Comp}} = R_1 \parallel R_f$$

Bias current compensation in an inverting amplifier

DC Characteristics of Op-Amp

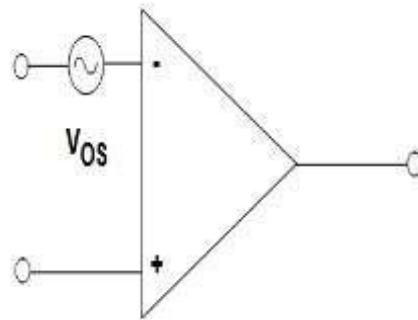
❖ In put offset current



Inverting amplifier with T-Feedback network

$$|I_{os}| = |I_B^+ - I_B^-|, \quad V_o = R_f I_{os} \quad \text{and} \quad R_s = R_f^2 / (R_f - 2R_t)$$

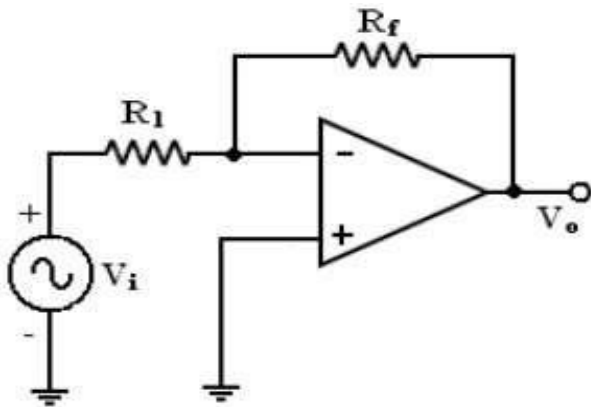
DC Characteristics of Op-Amp



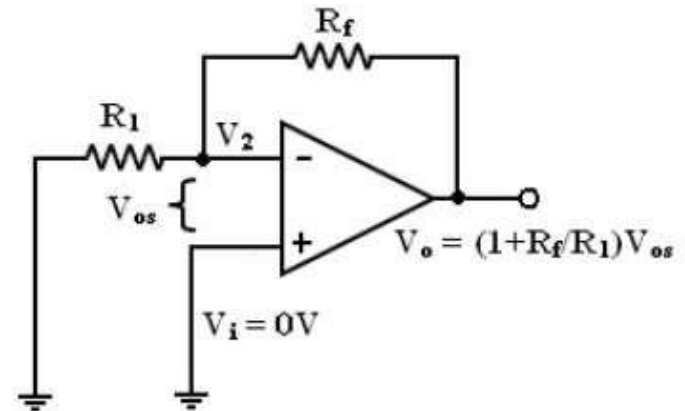
Op-Amp with input offset voltage

DC Characteristics of Op-Amp

❖ Input offset voltage



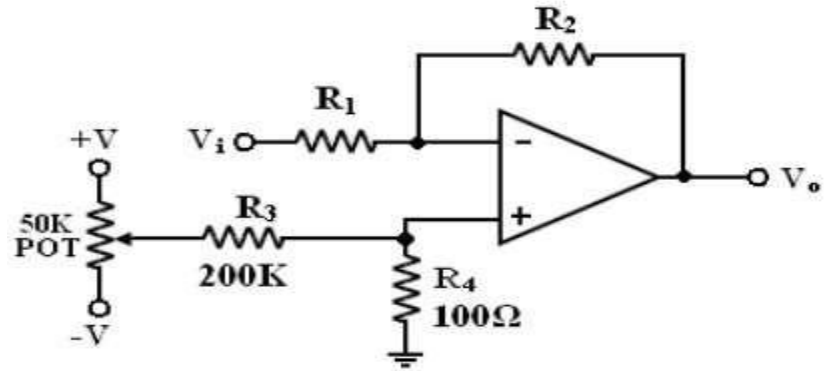
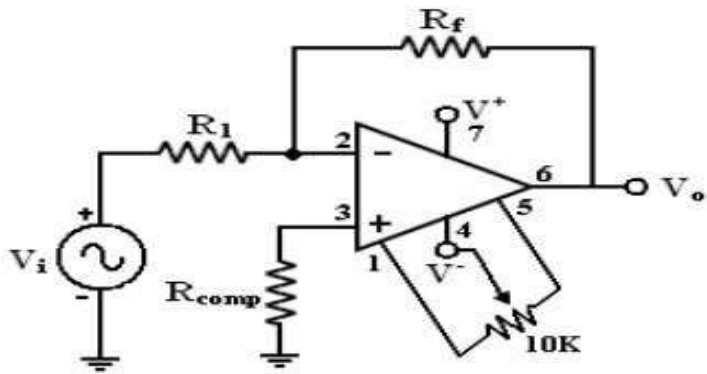
Inverting Amplifier



Equivalent circuit for $V_i = 0V$

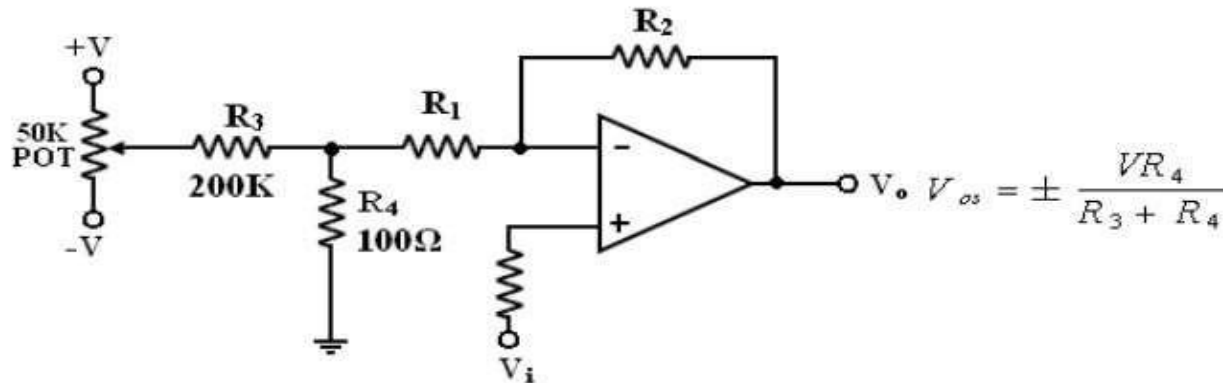
$$V_o = (1 + R_f/R_1)V_{ios}$$

DC Characteristics of Op-Amp



$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$

❖ Total O/P offset voltage



Balancing circuit for non-inverting amplifier

❖ Thermal Drift

- Bias current, offset current, and offset voltage change with temperature
- A circuit carefully nulled at 25°C may not remain. So when the temperature rises to 35°C . This is called drift.
- Offset current drift is expressed in $\text{nA}/^{\circ}\text{C}$.
- These indicate the change in offset for each degree Celsius change in temperature.

DC Characteristics of Op-Amp

DC Characteristics of Op-Amp

Design an inverting amplifier circuit using IC 741 Op-Amp to get a gain of -10 and an input impedance of $10\text{M}\Omega$. That is, calculate R_t , R_s and R_1 .

Sol : Set input impedance $R_i = 10\text{M}\Omega$, pick $R_1 = 10\text{M}\Omega$

$$\text{Since } A_{CL} = -(R_F / R_1)$$

$$\text{Therefore } R_F = A_{CL} R_1 = 100\text{M}\Omega$$

$$\text{Choose } R_t = 47\text{K}\Omega$$

$$R_s = R_t^2 / (R_f - 2R_t) = 22\Omega$$

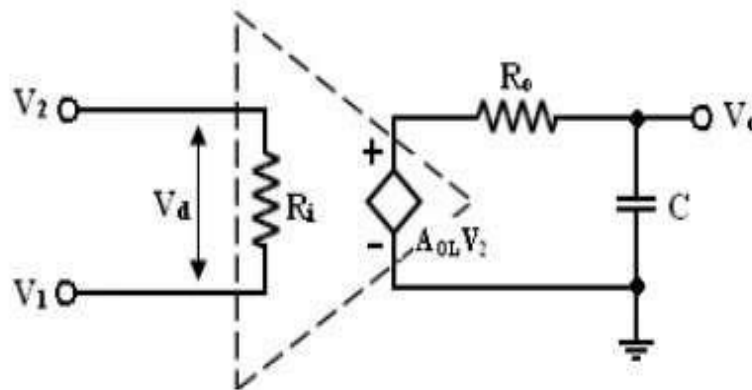
AC Characteristics of Op-Amp

AC Characteristics of Op-Amp



- ❖ Frequency response
- ❖ Stability of an Op-Amp
- ❖ Frequency compensation
- ❖ Slew rate

AC Characteristics of Op-Amp



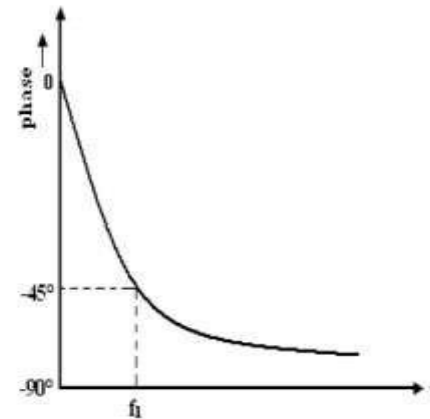
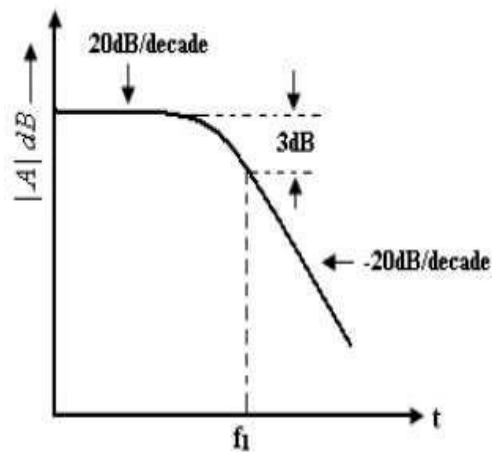
$$A = A_{OL} / (1 + j(f/f_1))$$

where $f_1 = 1/2\pi R_o C$

$$\Phi = -\tan^{-1} (f/f_1)$$

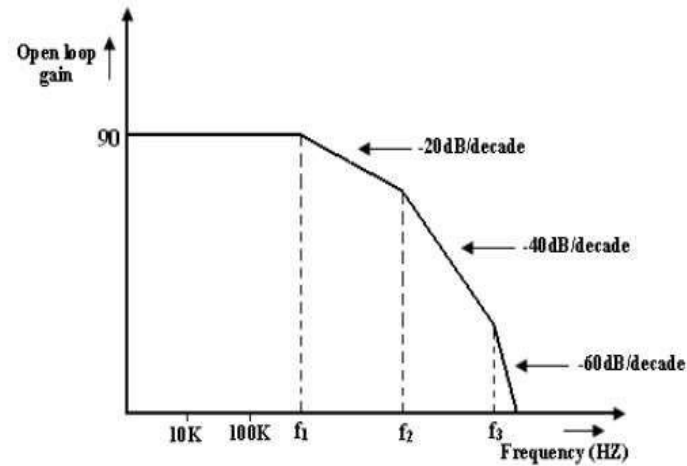
High frequency model of an Op-Amp with single corner frequency

AC Characteristics of Op-Amp



Open loop magnitude characteristics and phase characteristics for an op-amp with single break frequency

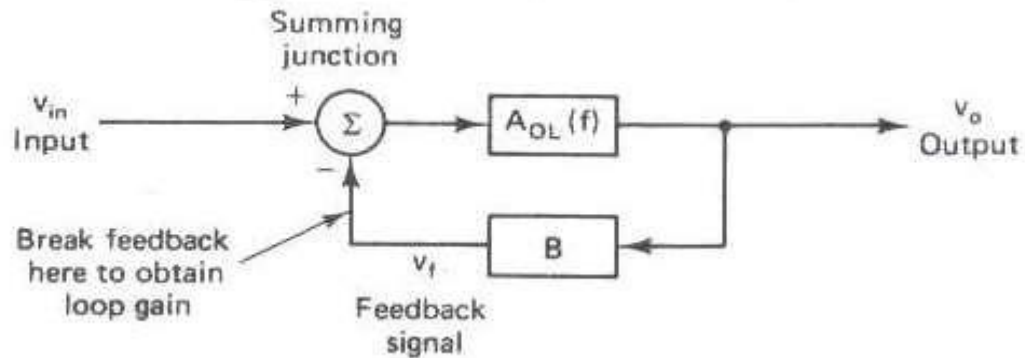
AC Characteristics of Op-Amp



Approximation of open loop gain vs frequency curve

$$A = A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3 / ((s + \omega_1) (s + \omega_2) (s + \omega_3))$$

AC Characteristics of Op-Amp



Condition for Magnitude $|A\beta| = 1$
Condition for Phase $\angle -A\beta = 0$ or

AC Characteristics of Op-Amp

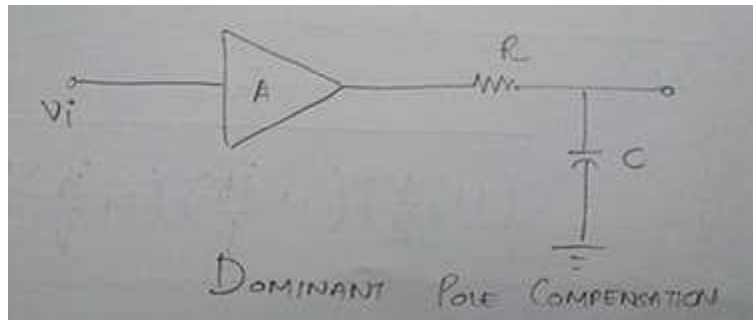
AC Characteristics of Op-Amp

- ❖ Frequency response
- ❖ Stability of an Op-Amp
- ❖ Frequency compensation
- ❖ Slew rate

AC Characteristics of Op-Amp

- External compensation
 - Internal Compensation
- Dominant – Pole compensation
 Pole – zero (Lag) compensation

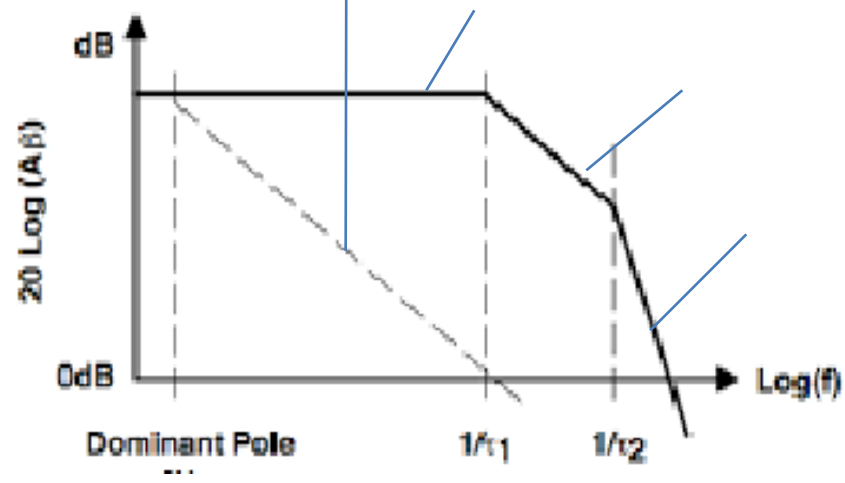
❖ Dominant – Pole Compensation



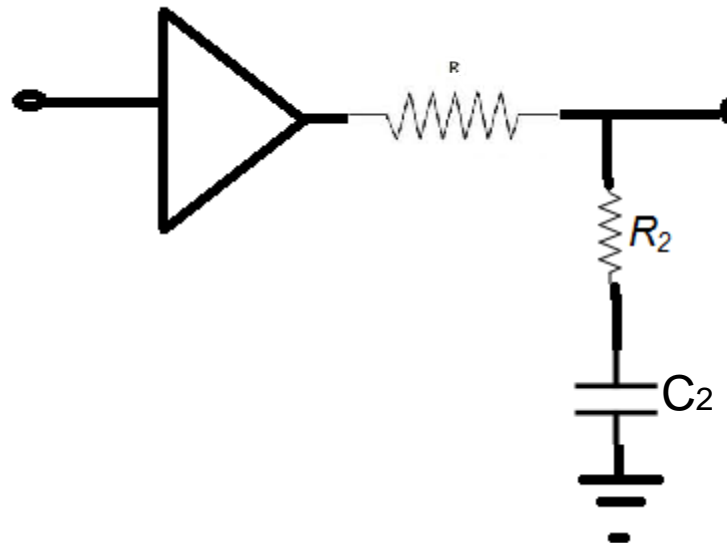
Transfer function $A' = A_{OL} / ((1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3))$
 Where $f_d < f_1 < f_2 < f_3$

AC Characteristics of Op-Amp

Dominant-pole compensation



AC Characteristics of Op-Amp

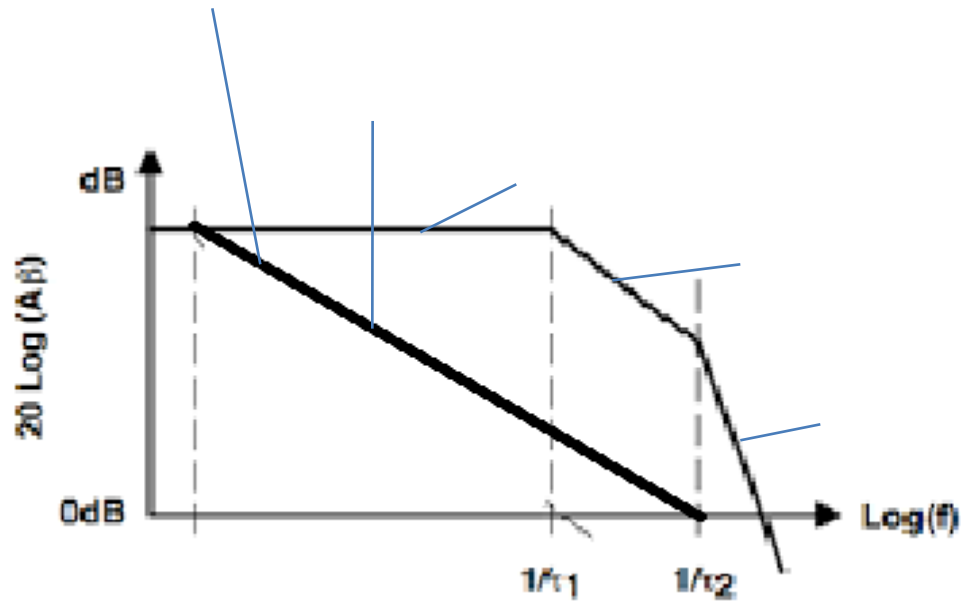


Pole-zero compensation

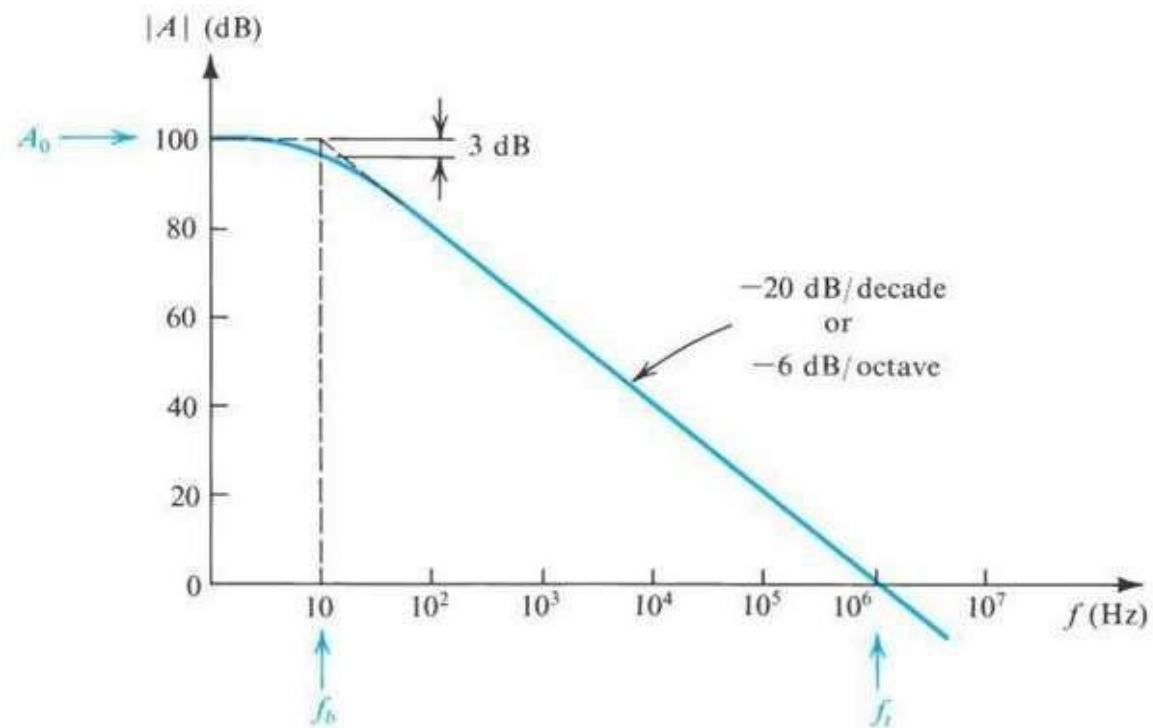
$$\text{Transfer function } A' = A_{OL} / ((1+jf/f_0)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3))$$

$$\text{Where } 0 < f_0 < f_1 < f_2 < f_3$$

AC Characteristics of Op-Amp



AC Characteristics of Op-Amp



Frequency response for internally compensated

AC Characteristics of Op-Amp

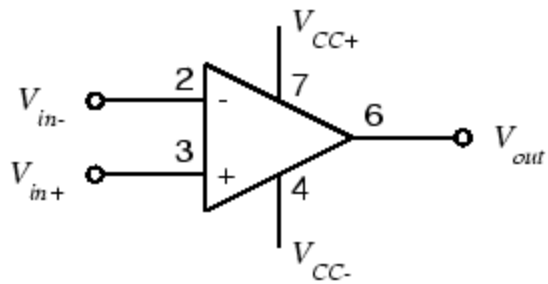
❖ Slew rate

The maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/ μ s.

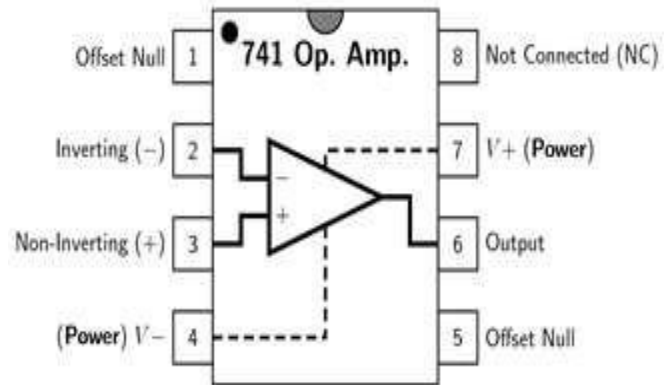
$$\left. \frac{dV_c}{dt} \right|_{max} = \frac{I}{C}$$

Features of IC741 Op-Amp

Features of IC741 Op-Amp



IC 741 Op-Amp Symbol



IC 741 Op-Amp Pin diagram

❖ Features of Op-Amp

- No frequency compensation required.
- Short circuit protection provided.
- Offset voltage null capability.
- Large common mode and Differential voltage range.
- No latch up.
- No External frequency compensation is required
- Short circuit Protection
- Low Power Dissipation

CMRR & PSRR

❖ CMRR

- Common mode rejection ratio is defined as the ratio of differential gain A_{DM} to the common mode gain A_{CM} .

CMRR is given by , $\rho = |A_{DM}|/|A_{CM}|$ in dB

❖ PSRR

- Power Supply Rejection Ratio. It is defined as the change in the input offset voltage due to the change in one of the two supply voltages when other voltage is maintained constant.



Unit-II

APPLICATIONS OF OP-AMPS



UNIT-II

APPLICATIONS OF OP-AMPS

Applications Of OP-Amps

A circuit is said to be linear, if there exists a linear relationship between its input and the output. Similarly, a circuit is said to be non-linear, if there exists a non-linear relationship between its input and output.

Op-amps can be used in both linear and non-linear applications.

The following are the basic applications of op-amp –

- 1) Inverting Amplifier
- 2) Non-inverting Amplifier
- 3) Voltage follower

Inverting amplifier:

- An inverting amplifier takes the input through its inverting terminal through a resistor R_1 , and produces its amplified version as the output. This amplifier not only amplifies the input but also inverts it (changes its sign).
- Note that for an op-amp, the voltage at the inverting input terminal is equal to the voltage at its non-inverting input terminal.

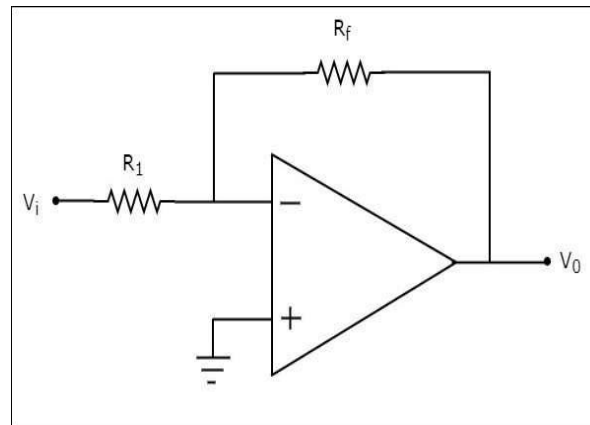


Fig: Circuit diagram of an inverting amplifier

Applications Of OP-Amps

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be zero volts.

The **nodal equation** at this terminal's node is as shown below.

$$\frac{0 - V_i}{R_1} + \frac{0 - V_0}{R_f} = 0$$

$$\Rightarrow \frac{-V_i}{R_1} = \frac{V_0}{R_f}$$

$$\Rightarrow V_0 = \left(\frac{-R_f}{R_1} \right) V_i$$

$$\Rightarrow \frac{V_0}{V_i} = \frac{-R_f}{R_1}$$

Applications Of OP-Amps

Non-inverting amplifier:

- A non-inverting amplifier takes the input through its non-inverting terminal, and produces its amplified version as the output. As the name suggests, this amplifier just amplifies the input, without inverting or changing the sign of the output.
- The circuit diagram of a non-inverting amplifier is shown in below figure.

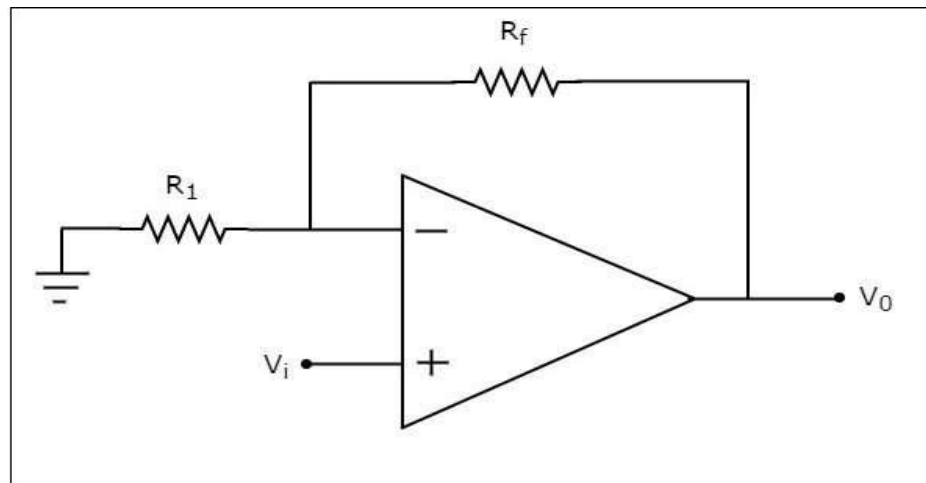


Fig: Circuit diagram of a Non-inverting amplifier

Applications Of OP-Amps

By using **voltage division principle**, we can calculate the voltage at the inverting input terminal of the op-amp as shown below –

$$\Rightarrow V_1 = V_0 \left(\frac{R_1}{R_1 + R_f} \right)$$

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal.

$$\Rightarrow V_1 = V_i$$

$$\Rightarrow V_0 \left(\frac{R_1}{R_1 + R_f} \right) = V_i$$

$$\Rightarrow \frac{V_0}{V_i} = \frac{R_1 + R_f}{R_1}$$

$$\Rightarrow \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Applications Of OP-Amps

Differentiator:

- A Differentiator is an electronic circuit that produces an output equal to the first derivative of its input. As the name suggests, the circuit performs the mathematical operation of differentiation.
- An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The circuit diagram of an op-amp based differentiator is shown in the following figure.

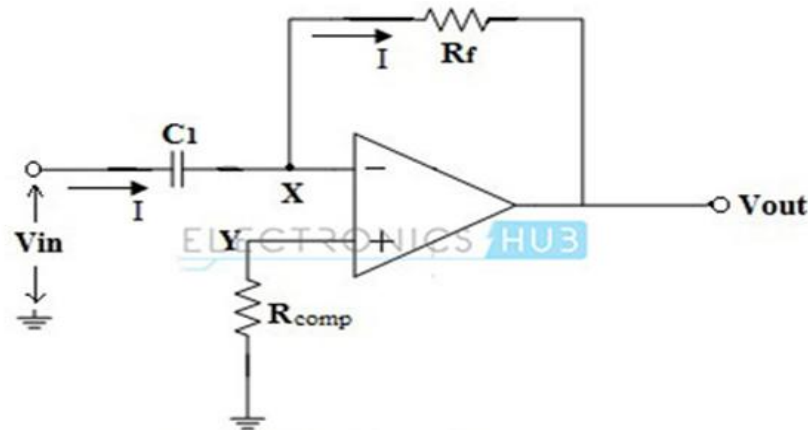


Fig: An Ideal Op-amp Differentiator

Applications Of OP-Amps

- According to the virtual short concept, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.
- The node equation at the inverting input terminals node is-

$$C \frac{d(0 - V_i)}{dt} + \frac{(0 - V_0)}{R} = 0$$

$$\Rightarrow -C \frac{dV_i}{dt} = \frac{V_0}{R}$$

$$\Rightarrow V_0 = -RC \frac{dV_i}{dt}$$

If $RC = 1$ sec, then the output voltage V_0 will be

$$V_0 = -\frac{dV_i}{dt}$$

Integrator:

- An Integrator is an electronic circuit that produces an output that is the integration of the applied input. This section discusses about the op-amp based integrator.
- An op-amp based integrator produces an output, which is an integral of the input voltage applied to its inverting terminal. The circuit diagram of an op-amp based integrator is shown in the below figure.

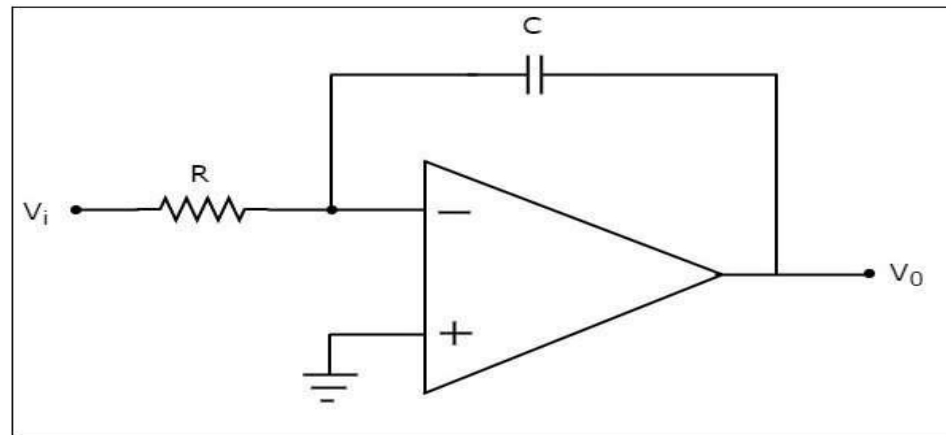


Fig: Integrator

Applications Of OP-Amps

- In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.
- According to virtual short concept, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

Applications Of OP-Amps

The **nodal equation** at the inverting input terminal is –

$$\begin{aligned} \frac{0 - V_i}{R} + C \frac{d(0 - V_0)}{dt} &= 0 \\ \Rightarrow \frac{-V_i}{R} &= C \frac{dV_0}{dt} \\ \Rightarrow \frac{dV_0}{dt} &= -\frac{V_i}{RC} \\ \Rightarrow dV_0 &= \left(-\frac{V_i}{RC}\right) dt \end{aligned}$$

Integrating both sides of the equation shown above, we get –

$$\begin{aligned} \int dV_0 &= \int \left(-\frac{V_i}{RC}\right) dt \\ \Rightarrow V_0 &= -\frac{1}{RC} \int V_i dt \end{aligned}$$

If $RC = 1$ sec, then the output voltage, V_0 will be –

$$V_0 = - \int V_i dt$$

Applications Of OP-Amps

Instrumentation amplifier:

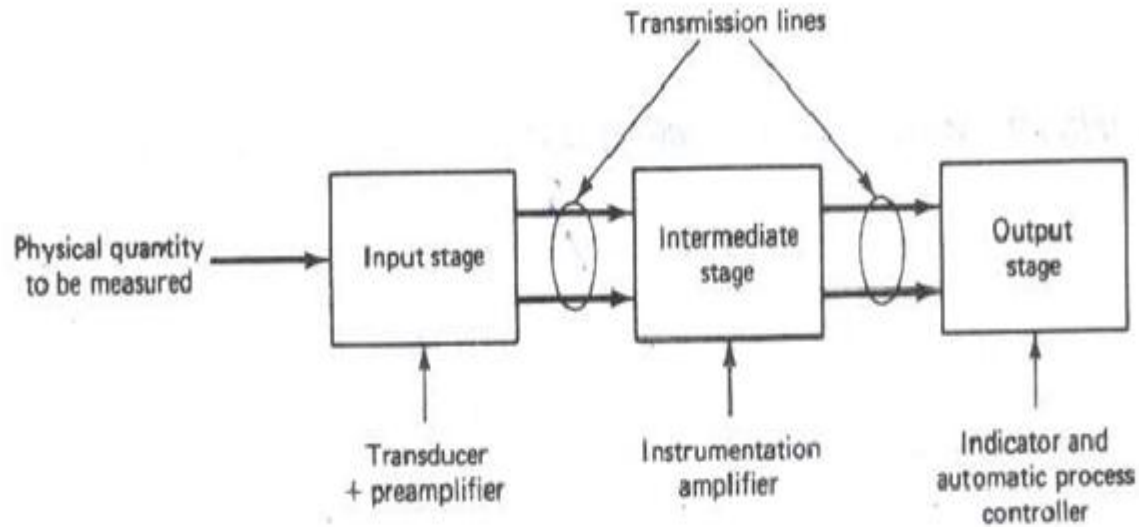


Fig: Block diagram of an Instrumentation system

Features of Instrumentation Amplifier:

- High gain Accuracy.
- High CMRR.
- High gain stability with low temperature coefficient.
- Low DC offset.
- Low output impedance.

Applications Of OP-Amps

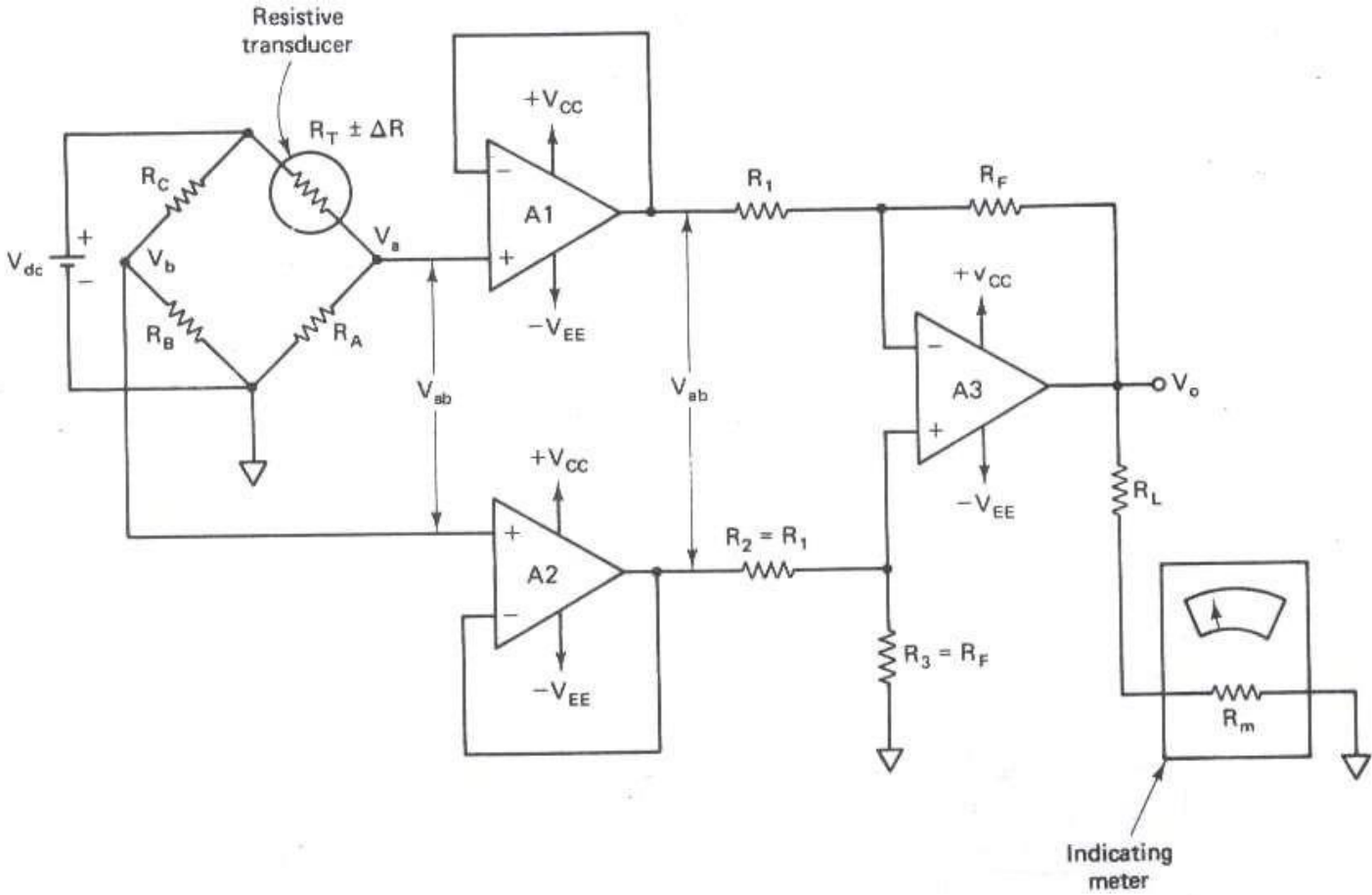


Fig: Instrumentation amplifier using transducer bridge

Applications Of OP-Amps

- A Resistive transducer whose resistance changes as a function of some physical energy is one arm of the bridge with a small circle around it and is denoted by $(R_T \pm \Delta R)$, where R_T is the resistance of the transducer and the change in resistance R_T .
- The bridge in the figure is dc excited but could be ac excited as well.
For the balanced bridge at some reference condition,

$$V_b = V_a$$

or

$$\frac{R_B (V_{dc})}{R_B + R_C} = \frac{R_A (V_{dc})}{R_A + R_T}$$

Applications Of OP-Amps

The bridge is balanced initially at a desired reference condition. However, as the physical quantity to be measured changes, the resistance of the transducer also changes, which causes the bridge to unbalance ($V_a \neq V_b$). The output voltage of the bridge can be expressed as a function of the change in resistance of the transducer, as described next.

Let the change in resistance of the transducer be ΔR . Since R_B and R_C are fixed resistors, the voltage V_b is constant. However, voltage V_a varies as a function of the change in transducer resistance. Therefore, according to the voltage-divider rule,

$$V_a = \frac{R_A(V_{dc})}{R_A + (R_T + \Delta R)}$$

$$V_b = \frac{R_B(V_{dc})}{R_B + R_C}$$

Consequently, the voltage V_{ab} across the output terminals of the bridge is

$$\begin{aligned} V_{ab} &= V_a - V_b \\ &= \frac{R_A V_{dc}}{R_A + R_T + \Delta R} - \frac{R_B V_{dc}}{R_B + R_C} \end{aligned}$$

However, if $R_A = R_B = R_C = R_T = R$, then

$$V_{ab} = - \frac{\Delta R(V_{dc})}{2(2R + \Delta R)}$$

Applications Of OP-Amps

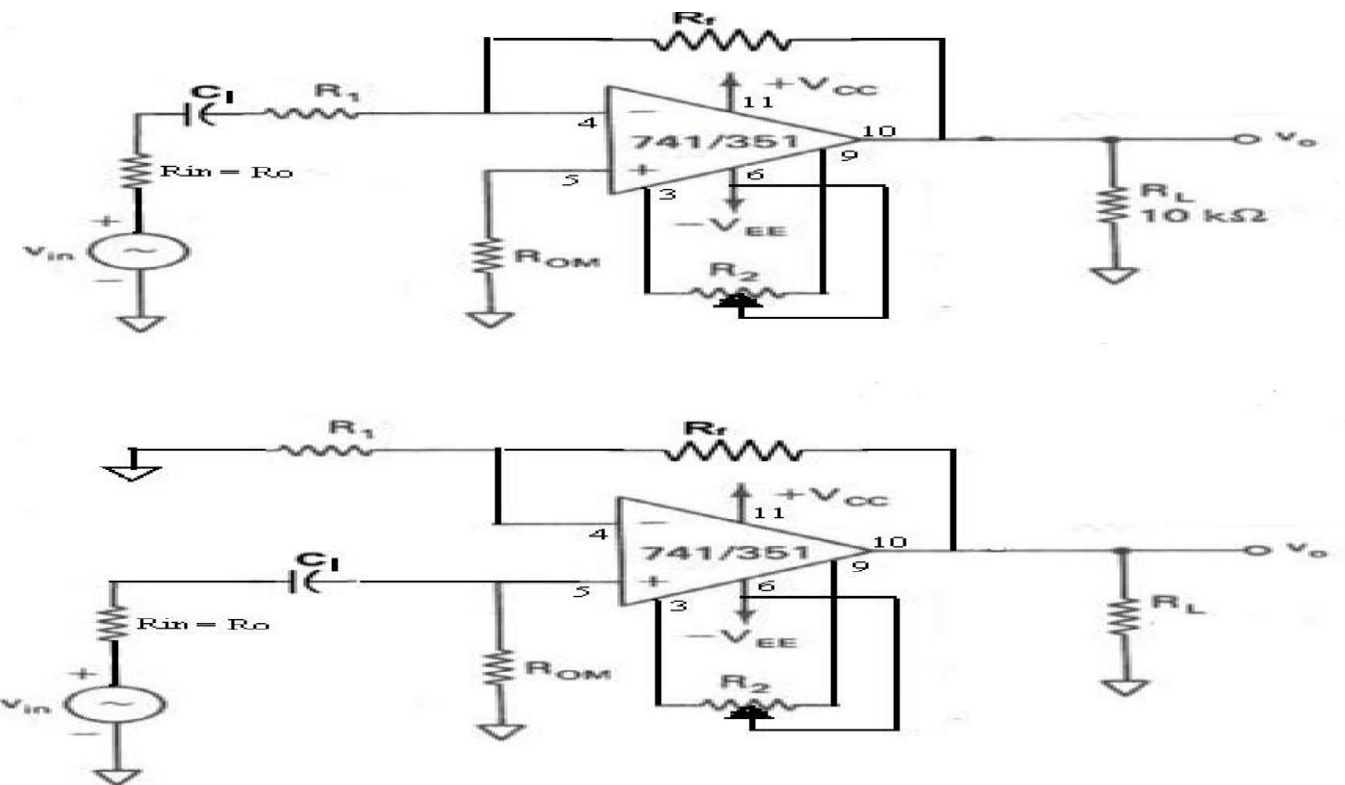
The negative (-) sign in this equation indicates that $V_a < V_b$ because of the increase in the value of R_T .

The output voltage V_{ab} of the bridge is then applied to the differential instrumentation amplifier composed of three op-amps (see Figure). The voltage followers preceding the basic differential amplifier help to eliminate loading of the bridge circuit. The gain of the basic differential amplifier is $(-R_F/R_1)$; therefore, the output V_o of the circuit is

$$V_o = V_{ab} \left(-\frac{R_F}{R_1} \right) = \frac{(\Delta R)V_{dc}}{2(2R + \Delta R)} \frac{R_F}{R_1}$$

Applications Of OP-Amps

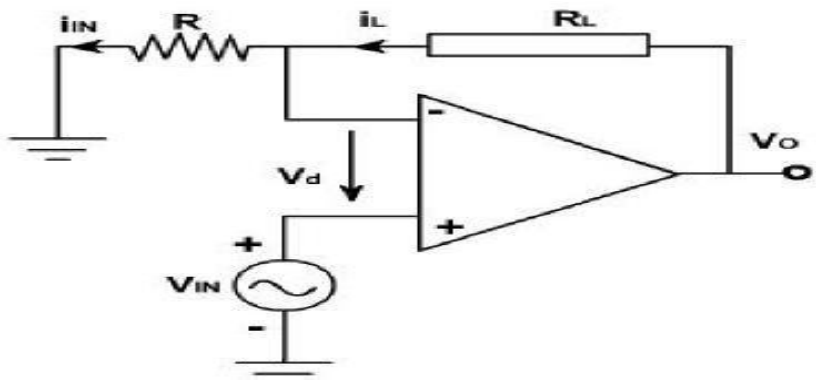
AC amplifier:



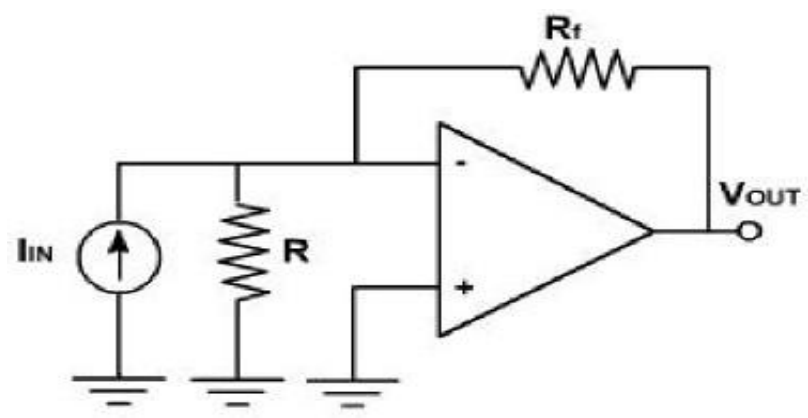
(a).AC Inverting Amplifier (b).AC Non-Inverting Amplifier

Applications Of OP-Amps

V to I Converter:



I to V Converter:



Applications Of OP-Amps

Comparators:

Voltage comparator circuit: Voltage comparator is a circuit which compares two voltages and switches the output to either high or low state depending upon which voltage is higher.

- A voltage comparator based on op-amp is shown below.
- Fig1 shows a voltage comparator in non inverting mode.
- Fig2 shows a voltage comparator in inverting mode and

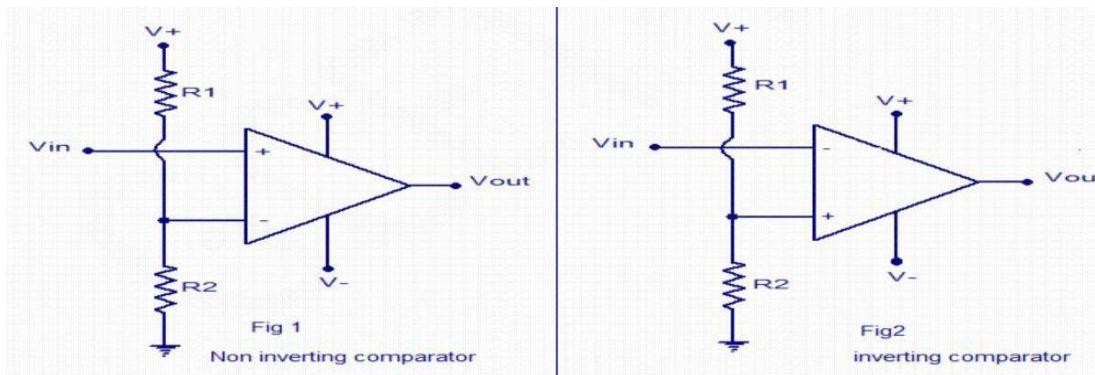
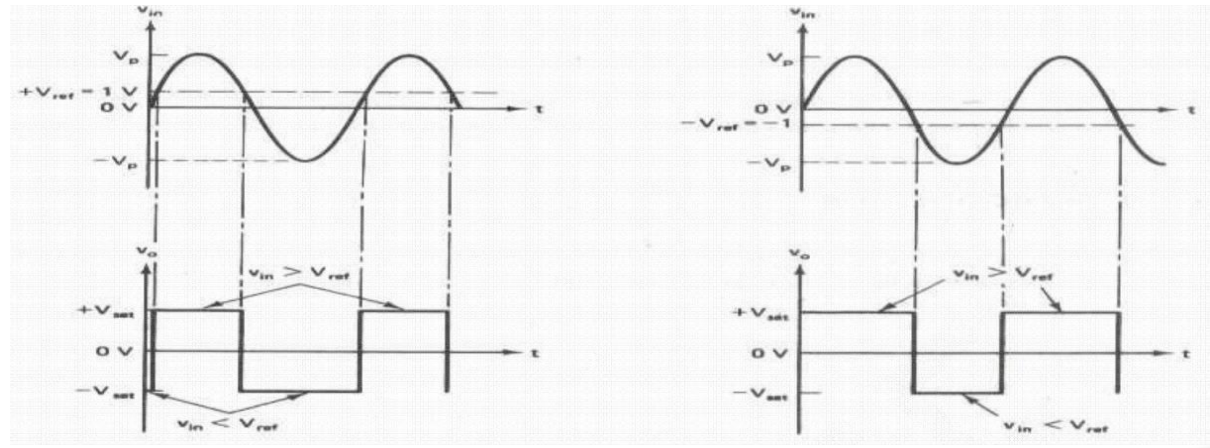
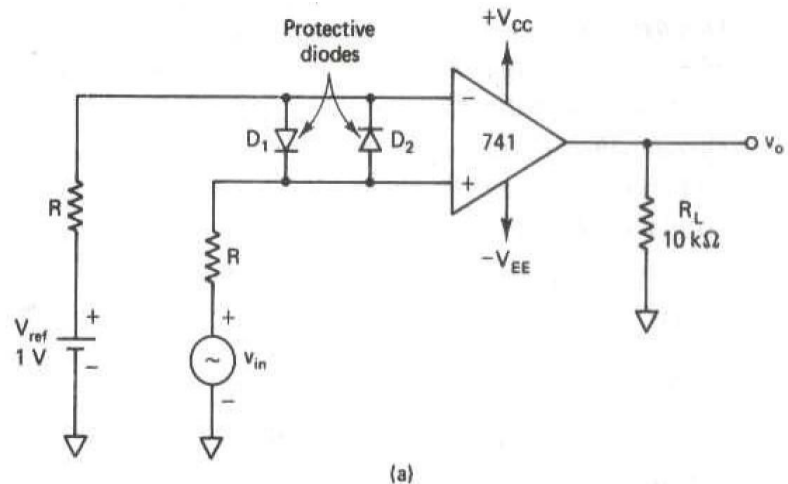


Fig: Circuit Diagram of Comparator

Applications Of OP-Amps

Op-amp voltage comparator:



Applications Of OP-Amps

Monostable multivibrator:

The monostable multivibrator circuit using op-amp is shown in below fig(a).

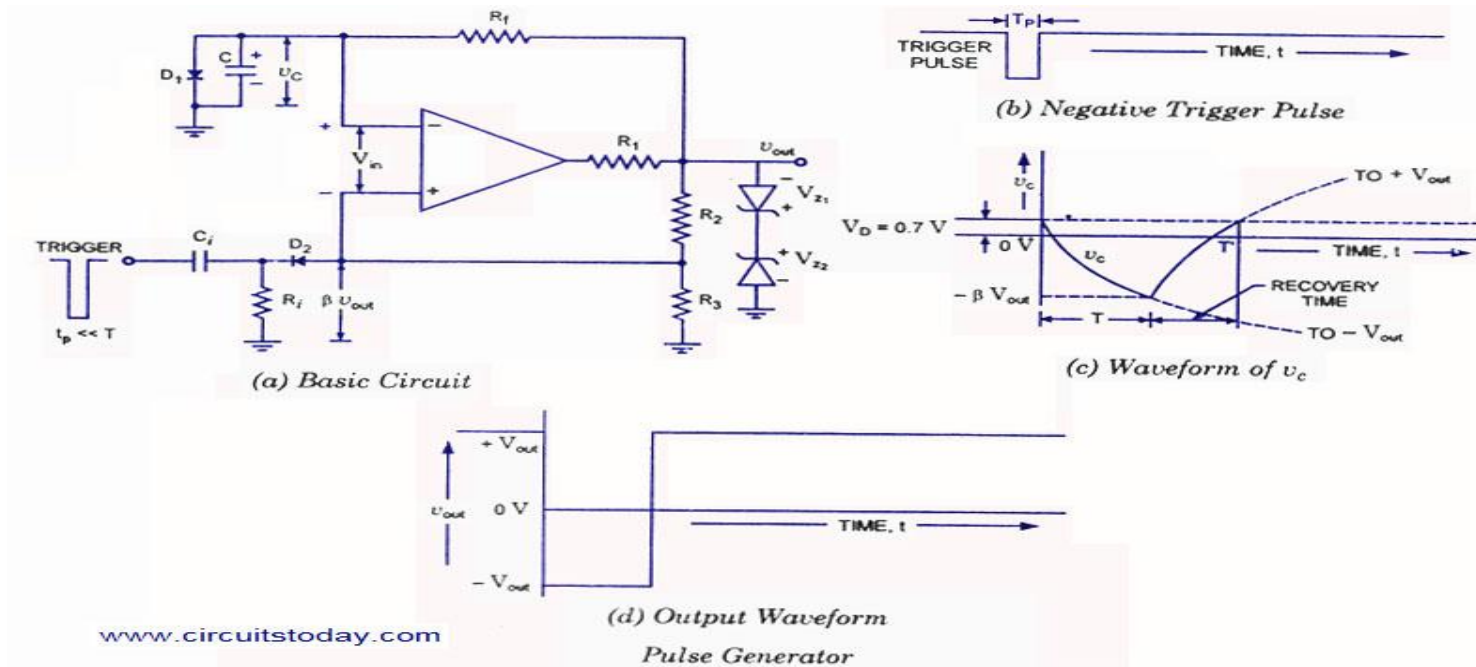


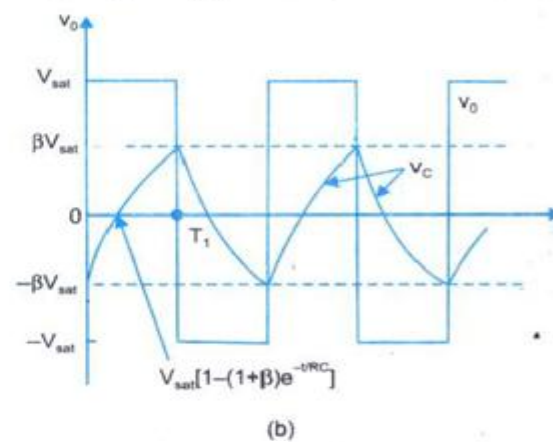
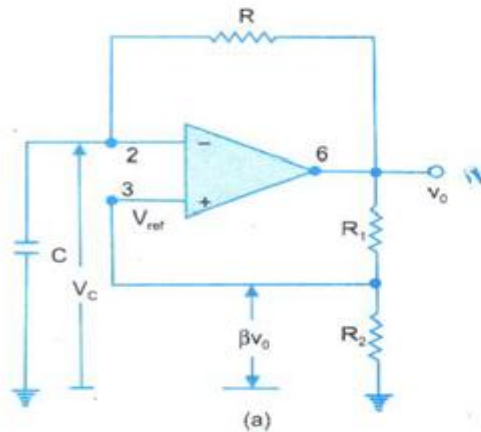
Fig: Monostable Multivibrator and input-output waveforms (a,b,c & d)

Applications Of OP-Amps

- The diode D1 is clamping diode connected across C the diode clamps the capacitor voltage to 0.7volts when the output is at $+V_{sat}$.
- A narrow $-ve$ triggering pulse V_t is applied to the non-inverting input terminal through diode D2.
- To understand the operation of the circuit, let us assume that the output V_o is at $+V_{sat}$ that is in its stable state. The diode D1 conducts and the voltage across the capacitor C that is V_c gets clamped to 0.7V.
- The voltage at the non-inverting input terminal is controlled by potentiometric divider of R1,R2 to βV_o that is $+\beta V_{sat}$ in the stable state.

Applications Of OP-Amps

Astable multivibrator:



(a) Simple op-amp square wave generator (b) waveforms

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat} (1 + \beta) e^{-t/RC}$$

Applications Of OP-Amps

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place, Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat} (1 + \beta) e^{-T_1/RC}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1 + \beta}{1 - \beta}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1 + \beta}{1 - \beta}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2 RC$

or

$$f_0 = \frac{1}{2RC}$$

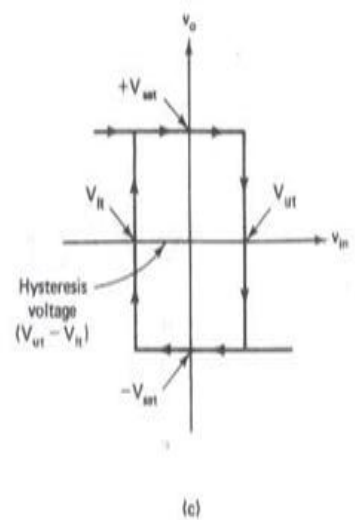
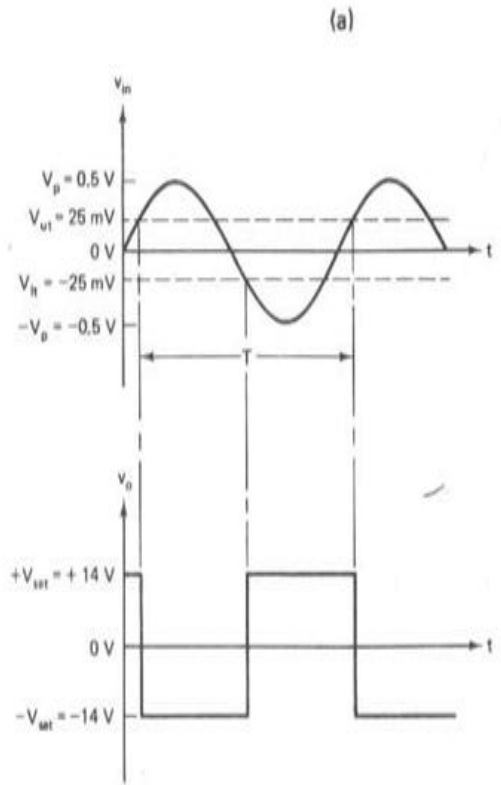
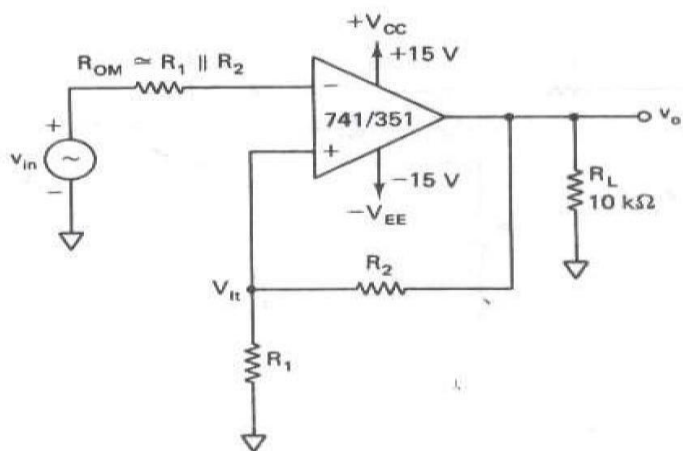
The output swings from $+ V_{sat}$ to $- V_{sat}$, so,

$$v_o \text{ peak-to-peak} = 2 V_{sat}$$

Triangular and Square wave generators:

- An inverting comparator with +ve feed back. This circuit converts an irregular shaped wave forms to a square wave form or pulse. The circuit is known as schmitt trigger or squaring circuit.
- The input voltage being triggers the output V_o every time it exceeds certain voltage levels called the upper threshold voltage V_{UT} and lower threshold voltage V_{LT} .
- These threshold voltages are obtained by using the voltage divider R_1 , R_2 , where the voltage across R_1 is feedback to +ve input. The voltage across R_1 is a variable reference, threshold voltage that depends on the value and polarity of the output voltage V_o . when $V_o = +V_{sat}$, the voltage across R_1 is called the upper threshold voltage V_{UT} .

Applications Of OP-Amps



Applications Of OP-Amps

Log Amplifier:

- An operational amplifier can be configured to function as a Logarithmic amplifier, or simply Log amplifier.
- Log amplifier is a non-linear circuit configuration, where the output is K times the logarithmic value of the input voltage applied.
- Log amplifiers find the applications in computations such as multiplication and division of signals, computation of powers and roots, signal compression and decompression, as well as in process control in industrial applications.
- A log amplifier can be constructed using a bipolar junction transistor in the feedback to the op-amp, since the collector current of a BJT is logarithmically related to its base-emitter voltage.

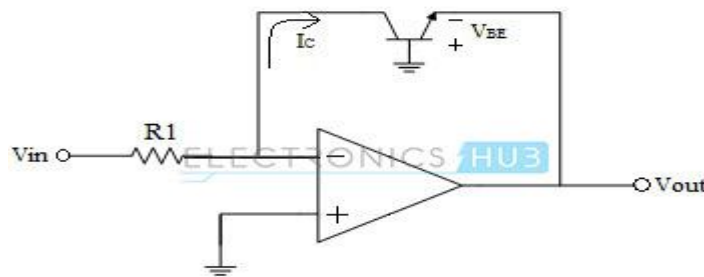


Fig: Op-amp Logarithmic Amplifier

Applications Of OP-Amps

- The necessary condition of the log amplifier to work is that the input voltage always must be positive. It can be seen that $V_{OUT} = -V_{BE}$.
- Since the collector terminal of the transistor is held at virtual ground and the base terminal is also grounded, the voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_S \cdot [e^{q(V_{be})/kT} - 1]$$

Where,

I_S = the saturation current,

k = Boltzmann's constant,

T = absolute temperature (in K).

Applications Of OP-Amps

Since $I_E = I_C$ for grounded base transistor,

$$I_C = I_S \cdot [e^{q(V_{be})/kT} - 1]$$

$$(I_C/I_S) = [e^{q(V_{be})/kT} - 1]$$

$$(I_C/I_S) + 1 = [e^{q(V_{be})/kT}]$$

$$(I_C + I_S)/I_S = e^{q(V_{be})/kT}$$

$$e^{q(V_{BE})/kT} = (I_C/I_S) \text{ since } I_C \gg I_S$$

Taking natural log on both sides of the above equation, we get

$$V_{be} = (kT/q) \ln[I_C/I_S]$$

The collector current $I_C = V_{in}/R_1$ and $V_{out} = -V_{be}$

Therefore,

$$V_{out} = -(kT/q) \ln[V_{in}/R_1 \cdot I_S]$$



Unit-III

ACTIVE FILTERS AND TIMERS



ACTIVE FILTERS

An electric filter is often a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filters may be classified in a number of ways:

Analog or digital

Passive or active

Audio (AF) or radio frequency (RF)

Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques. Depending on the type of elements used in their construction, filters may be classified as passive or active.

Elements used in passive filters are resistors, capacitors, and inductors. Active filters, on the other hand, employ transistors or op-amps in addition to the resistors and capacitors. The type of element used dictates the operating frequency range of the filter.

An active filter offers the following advantages over a passive filter:

Gain and frequency adjustment flexibility. Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.

No loading problem. Because of the high input resistance and low output resistance of the op- amp, the active filter does not cause loading of the source or load.

Cost. Typically, active filters are more economical than passive filters. This is because of the variety of cheaper op-amps and the absence of inductors.

The most commonly used filters are these:

- Low-pass filter

- High-pass filter

- Band-pass filter

- Band-reject filter

- All-pass filter

ACTIVE FILTERS

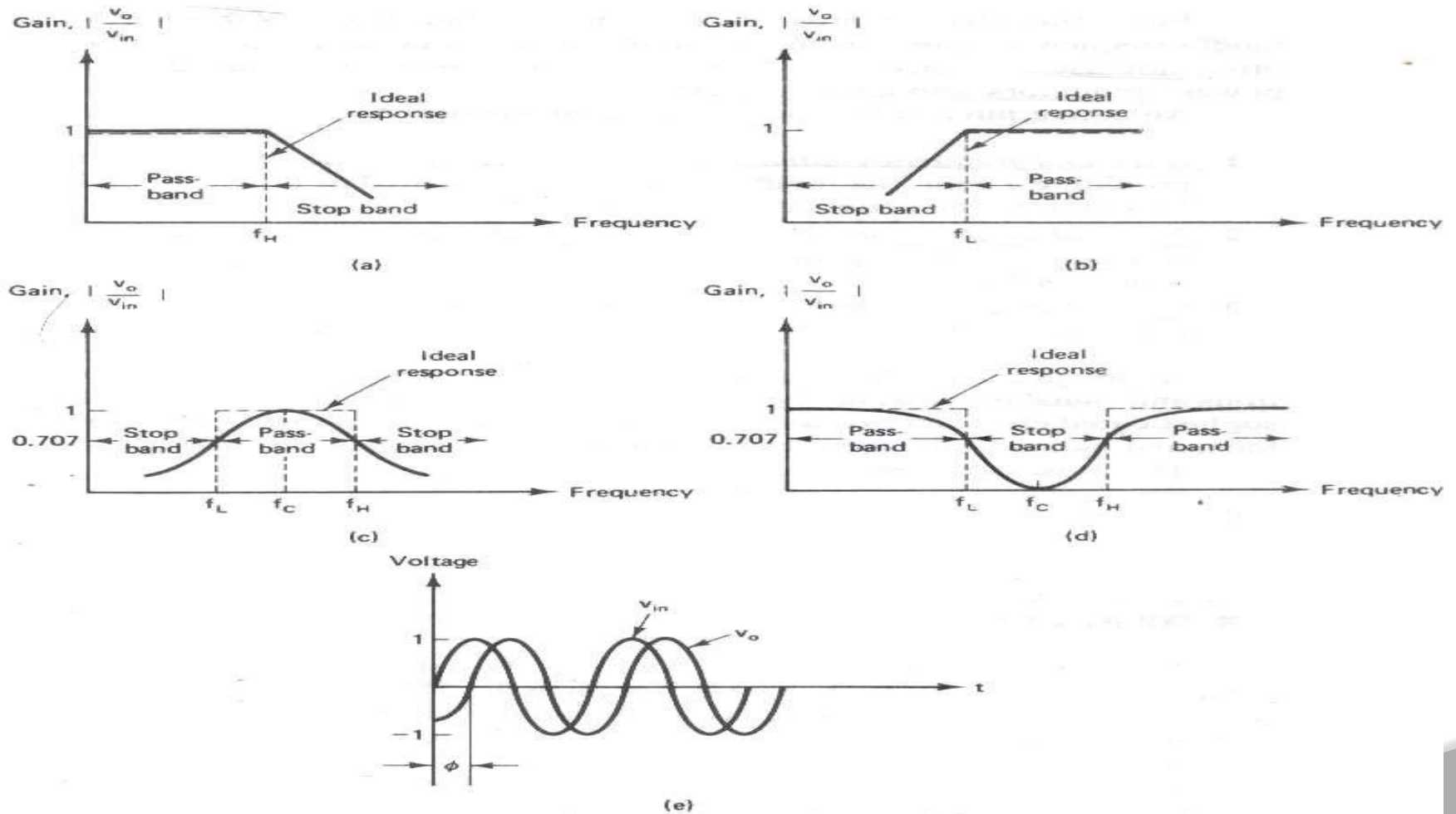


Figure 8-1 Frequency response of the major active filters. (a) Low pass. (b) High pass. (c) Band pass. (d) Band reject. (e) Phase shift between input and output voltages of an all-pass filter.

ACTIVE FILTERS

FIRST-ORDER LOW-PASS BUTTER WORTH FILTER

Fig. shows a first-order low-pass Butterworth filter that uses an RC network for filtering. Note that the op-amp is used in the non-inverting configuration; hence it does not load down the RC network. Resistors R_1 and R_F determine the gain of the filter.

According to the voltage-divider rule, the voltage at the non-inverting terminal (across capacitor

$$v_1 = \frac{-jX_C}{R - jX_C} v_{in} \quad \text{Is}$$

$$j = \sqrt{-1} \quad \text{and} \quad -jX_C = \frac{1}{j2\pi fC}$$

$$v_1 = \frac{v_{in}}{1 + j2\pi fRC}$$

$$v_o = \left(1 + \frac{R_F}{R_1}\right) v_1$$

ACTIVE FILTERS

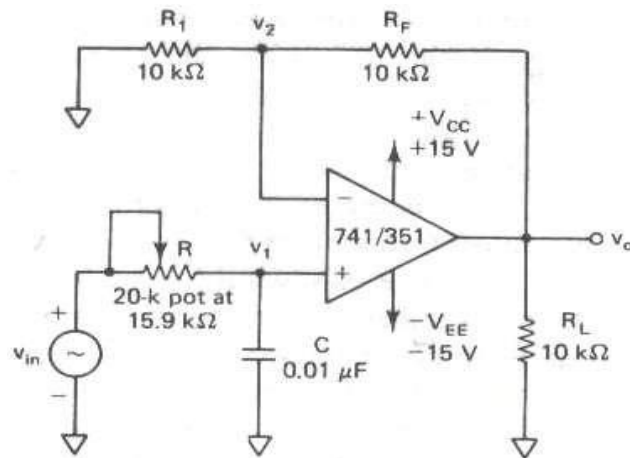
$$v_o = \left(1 + \frac{R_F}{R_1}\right) \frac{v_{in}}{1 + j2\pi fRC}$$

where $\frac{v_o}{v_{in}}$ = gain of the filter as a function of frequency

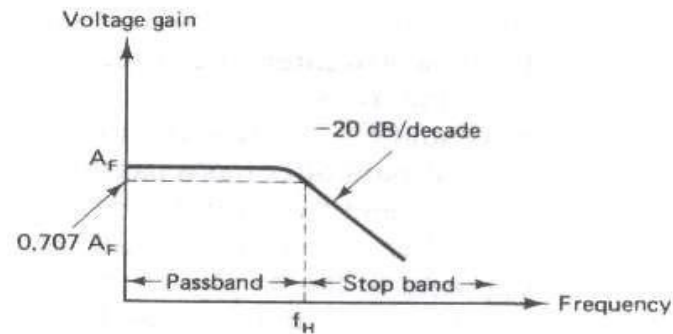
$$A_F = 1 + \frac{R_F}{R_1} = \text{passband gain of the filter}$$

f = frequency of the input signal

$$f_H = \frac{1}{2\pi RC} = \text{high cutoff frequency of the filter}$$



(a)



(b)

Figure 8-2 First-order low-pass Butterworth filter. (a) Circuit. (b) Frequency response.

ACTIVE FILTERS

The gain magnitude and phase angle equations of the low-pass filter can be obtained by converting Equation (1) into its equivalent polar form, as follows:

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

$$\phi = -\tan^{-1} \left(\frac{f}{f_H} \right)$$

Where ϕ is the phase angle in degrees.

The operation of the low-pass filter can be verified from the gain magnitude equation, (2):

1. At very low frequencies, that is, $f < f_H$, $\left| \frac{v_o}{v_{in}} \right| \cong A_F$
2. At $f = f_H$, $\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{2}} = 0.707A_F$
3. At $f > f_H$, $\left| \frac{v_o}{v_{in}} \right| < A_F$

ACTIVE FILTERS

SECOND-ORDER LOW-PASS BUTTER WORTH FILTER

A stop-band response having a 40-dB/decade roll-off is obtained with the second order low-pass filter. A first-order low-pass filter can be converted into a second order type simply by using an additional RC network, as shown in Fig.

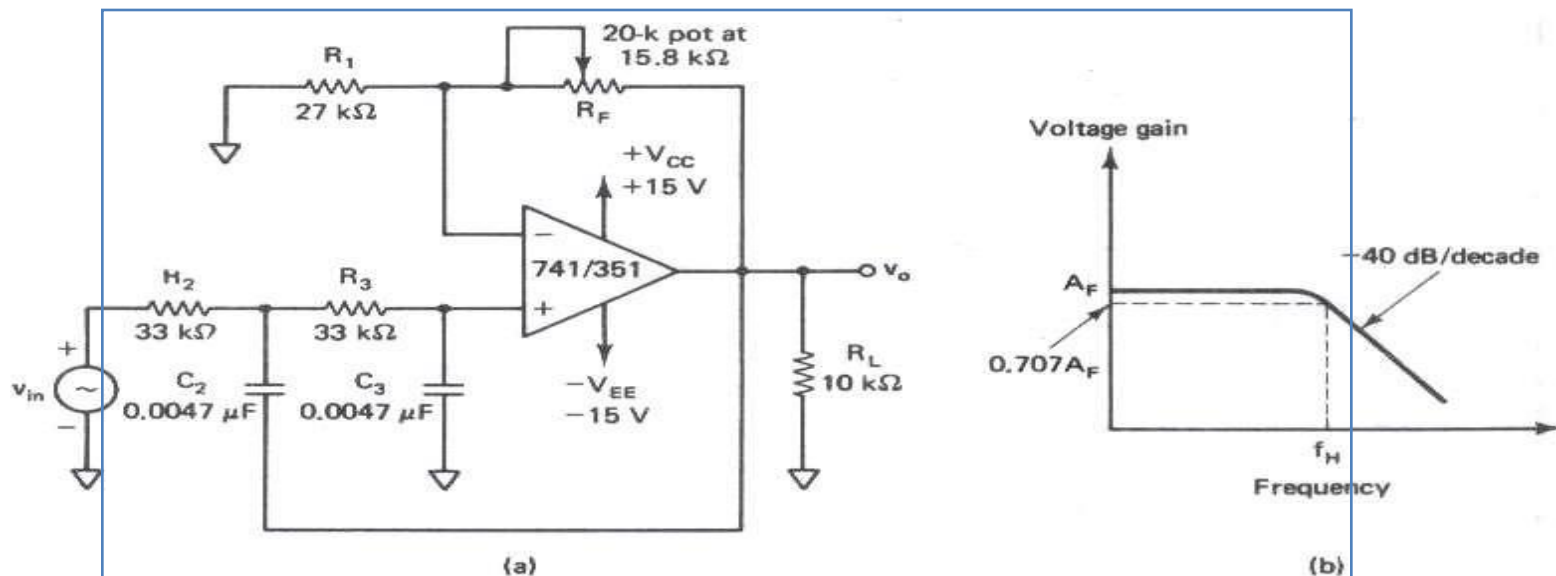


Figure 8-4 Second-order low-pass Butterworth filter. (a) Circuit. (b) Frequency response.

ACTIVE FILTERS

high cutoff frequency f_H is determined by R_2 , C_2 , R_3 , and C_3 , as follows:

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

Furthermore, for a second-order low-pass Butterworth response, the voltage gain magnitude equation is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^4}}$$

where $A_F = 1 + \frac{R_F}{R_1}$ = passband gain of the filter

f = frequency of the input signal (Hz)

$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$ = high cutoff frequency (Hz)

ACTIVE FILTERS

FIRST-ORDER HIGH-PASS BUTTERWORTH FILTER

High-pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters. That is, a first-order high-pass filter is formed from a first-order low-pass type by interchanging components R and C.

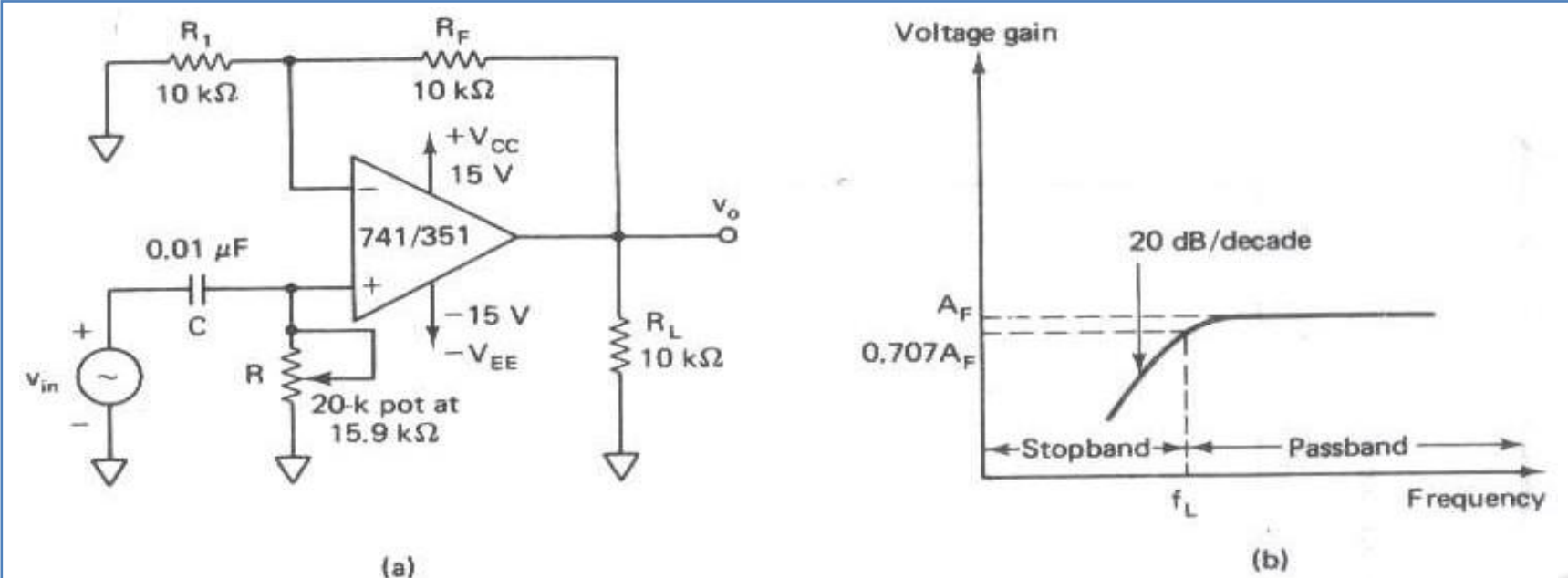


Figure 8–6 (a) First-order high-pass Butterworth filter. (b) Its frequency response.

ACTIVE FILTERS

For the first-order high-pass filter of Figure (a), the output voltage is

$$v_o = \left(1 + \frac{R_F}{R_1}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} v_{in}$$

$$\frac{v_o}{v_{in}} = A_F \left[\frac{j(f/f_L)}{1 + j(f/f_L)} \right]$$

where $A_F = 1 + \frac{R_F}{R_1}$ = passband gain of the filter
 f = frequency of the input signal (Hz)
 $f_L = \frac{1}{2\pi RC}$ = low cutoff frequency (Hz)

Hence the magnitude of the voltage gain is

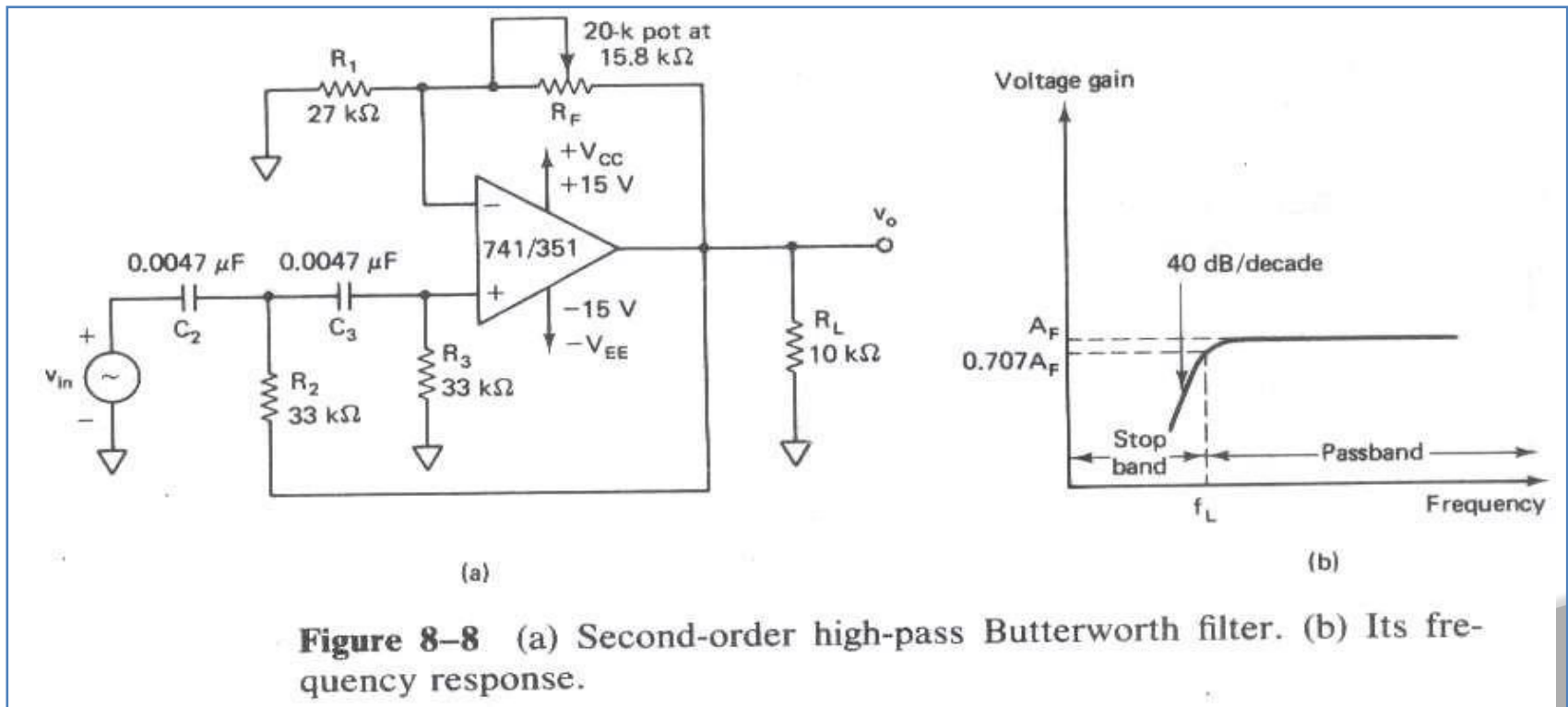
$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

Since high-pass filters are formed from low-pass filters simply by interchanging R's and C's, the design and frequency scaling procedures of the low-pass filters are also applicable to the high-pass filters.

ACTIVE FILTERS

SECOND-ORDER HIGH-PASS BUTTERWORTH FILTER

As in the case of the first-order filter, a second-order high-pass filter can be formed from a second-order low-pass filter simply by interchanging the frequency-determining resistors and capacitors. Figure(a) shows the second-order high-pass filter.



ACTIVE FILTERS

The voltage gain magnitude equation of the second-order high-pass filter is as follows:

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + (f_L/f)^4}}$$

Where $A_F = 1.586$ = passband gain for the second-order Butterworth response

f = frequency of the input signal (Hz)

f_L = low cutoff frequency (Hz)

Since second-order low-pass and high-pass filters are the same circuits except that the positions of resistors and capacitors are interchanged, the design and frequency scaling procedures for the high-pass filter are the same as those for the low-pass filter.

BAND-PASS FILTERS

A band-pass filter has a passband between two cutoff frequencies f_H and f_L such that $f_H > f_L$. Any input frequency outside this passband is attenuated.

Basically, there are two types of band-pass filters:

- Wide band pass, and
- Narrow band pass.

$$Q = \frac{f_c}{\text{BW}} = \frac{f_c}{f_H - f_L}$$

wide band-pass filter the center frequency f_c can be defined as

$$f_c = \sqrt{f_H f_L}$$

where f_H = high cutoff frequency (Hz)

f_L = low cutoff frequency of the wide band-pass filter (Hz)

In a narrow band-pass filter, the output voltage peaks at the center frequency.

ACTIVE FILTERS

Wide band-pass filter

A wide band-pass filter can be formed by simply cascading high-pass and low-pass sections and is generally the choice for simplicity of design and performance.

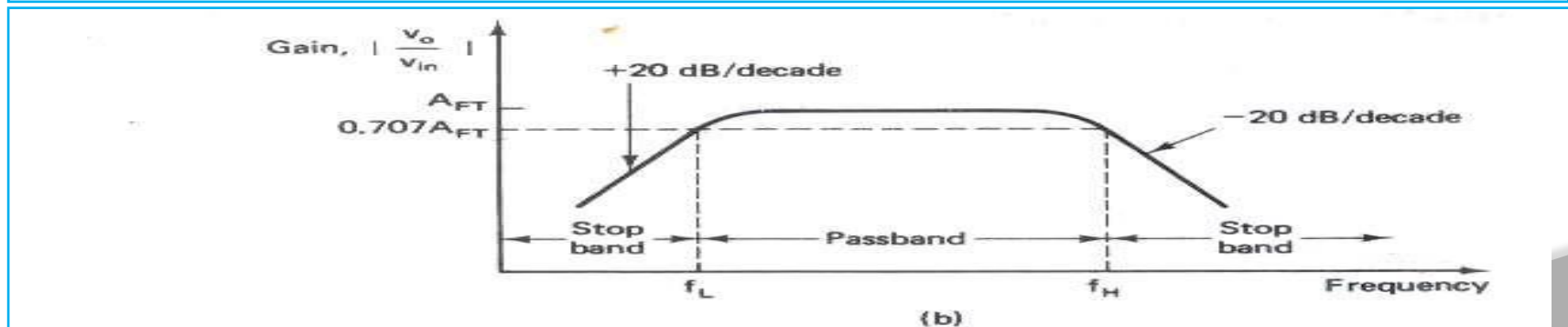
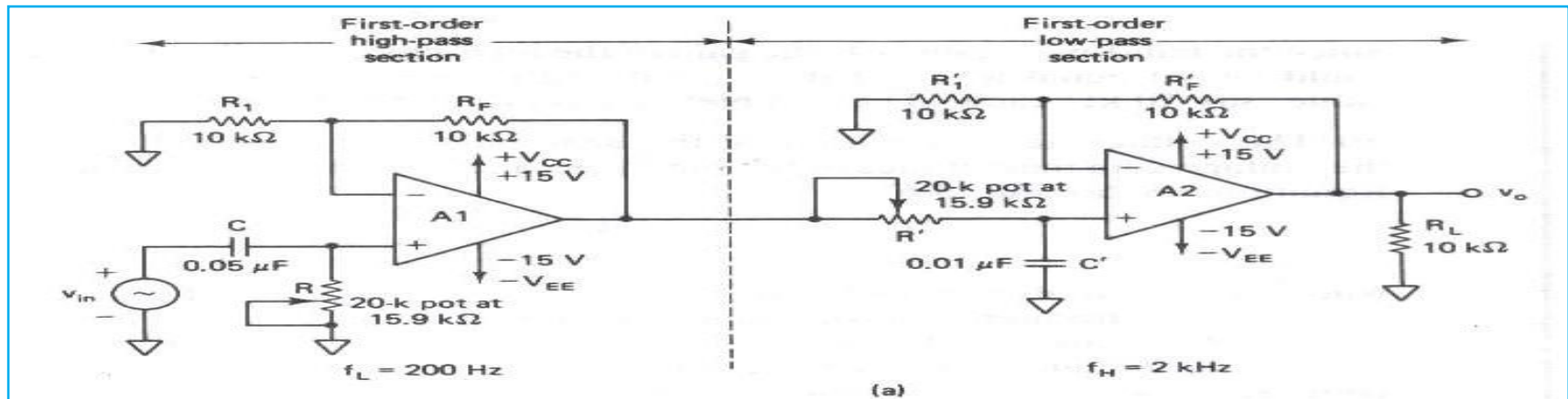


Figure 8-11 (a) $\pm 20 \text{ dB/decade}$ -wide band-pass filter. (b) Its frequency response. A_1 and A_2 dual op-amp: 1458/353.

ACTIVE FILTERS

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}} \quad \left| \frac{v_o}{v_{in}} \right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

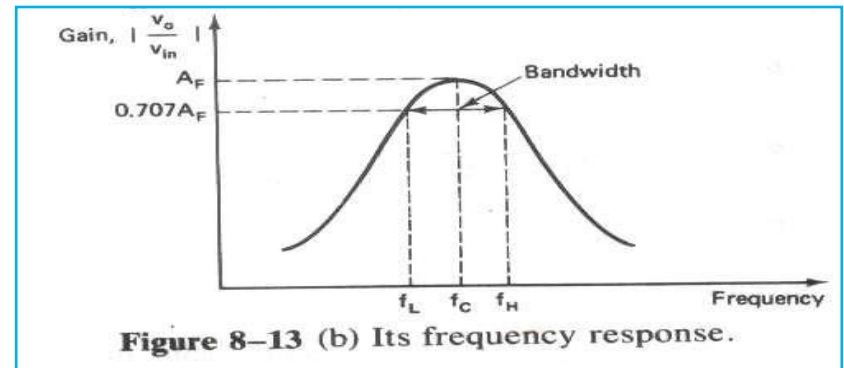
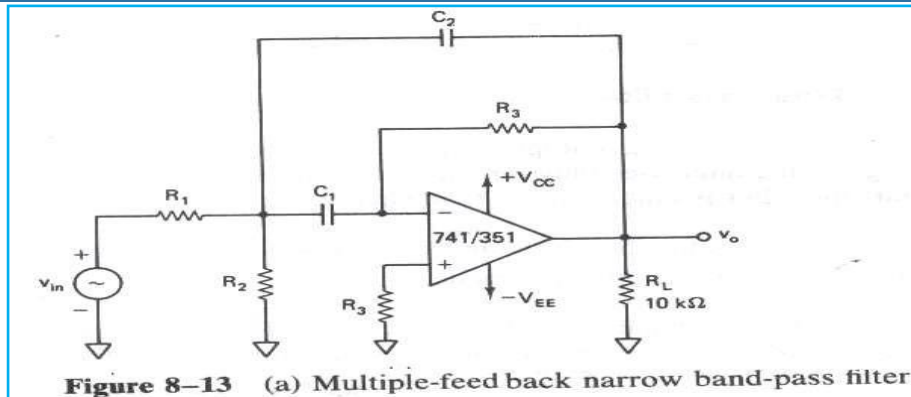
$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_{FT}(f/f_L)}{\sqrt{[1 + (f/f_L)^2][1 + (f/f_H)^2]}}$$

where A_{FT} = total passband gain
 f = frequency of the input signal (Hz)
 f_L = low cutoff frequency (Hz)
 f_H = high cutoff frequency (Hz)

Narrow Band-Pass Filter

The narrow band-pass filter using multiple feedback is shown in Figure 8-13. As shown in this figure, the filter uses only one op-amp. Compared to all the filters discussed so far, this filter is unique in the following respects: It has two feedback paths, hence the name multiple-feedback filter. The op-amp is used in the inverting mode.

ACTIVE FILTERS



The circuit components are determined from the following relationships. To simplify the design calculations, choose $C_1 = C_2 = C$.

$$R_1 = \frac{Q}{2\pi f_c C A_F} \qquad R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} \qquad R_3 = \frac{Q}{\pi f_c C}$$

Where A_F is the gain at f_c , given by

$$A_F = \frac{R_3}{2R_1}$$

ACTIVE FILTERS

The gain A_F , however, must satisfy the condition $A_F < 2Q^2$

Another advantage of the multiple feedback filter of Figure 8-13 is that its center frequency f_c can be changed to a new frequency f'_c without changing the gain or bandwidth. This is accomplished simply by changing R_2 to R'_2 so that

$$R'_2 = R_2 \left(\frac{f_c}{f'_c} \right)^2$$

BAND-REJECT FILTERS

The band-reject filter is also called a band-stop or band-elimination filter. In this filter, frequencies are attenuated in the stopband while they are passed outside this band
the band-reject filters can also be classified as (1) wide band-reject or (2) narrow band-reject.

ACTIVE FILTERS

Wide Band-Reject Filter

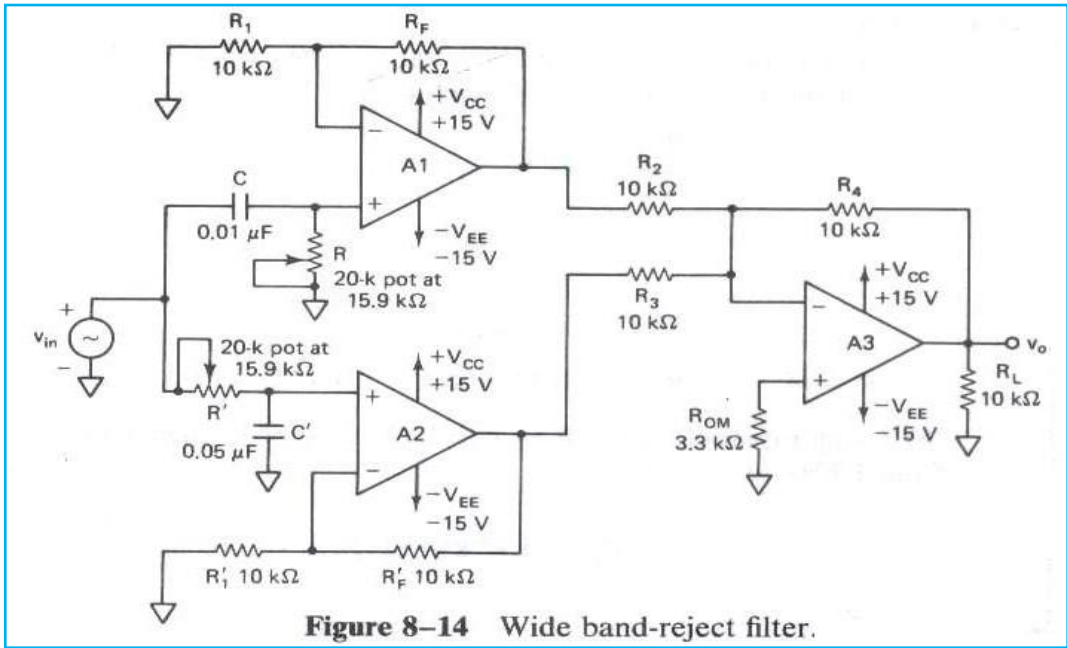


Figure 8-14 Wide band-reject filter.

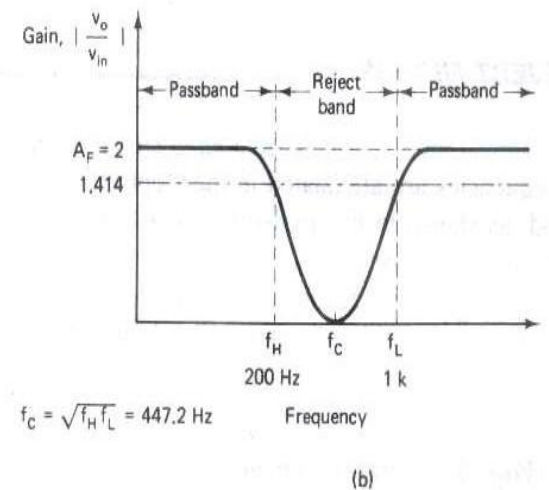


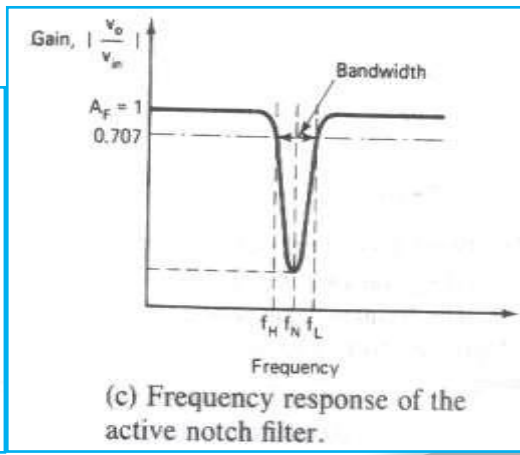
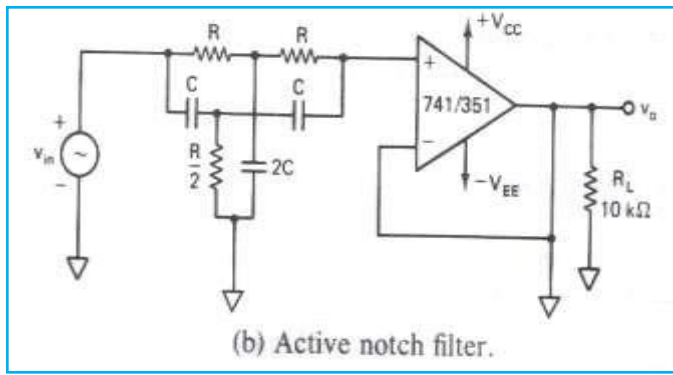
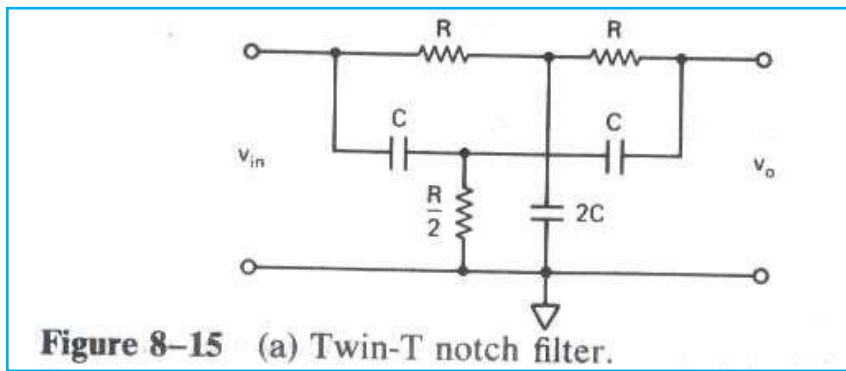
Figure 8-14 Wide band-reject filter. (a) Circuit. (b) Frequency response. For A_1 , A_2 , and A_3 use quad op-amp $\mu\text{AF774}/\text{MC34004}$.

Narrow Band-Reject Filter

The narrow band-reject filter, often called the notch filter, is commonly used for the rejection of a single frequency such as the 60-Hz power line frequency hum. This is a passive filter composed of two T-shaped networks. The notch-out frequency is the frequency at which maximum attenuation occurs; it is given by

ACTIVE FILTERS

$$f_N = \frac{1}{2\pi RC}$$



ACTIVE FILTERS

ALL-PASS FILTER

As the name suggests, an all-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different frequencies of the input signal. When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. To compensate for these phase changes, all-pass filters are required. The all-pass filters are also called delay equalizers or phase correctors. Figure 8-16(a) shows an all-pass filter wherein $R_F = R_1$. The output voltage V_o of the filter can be obtained by using the superposition theorem:

$$v_o = -v_{in} + \frac{-jX_C}{R - jX_C} v_{in}(2)$$

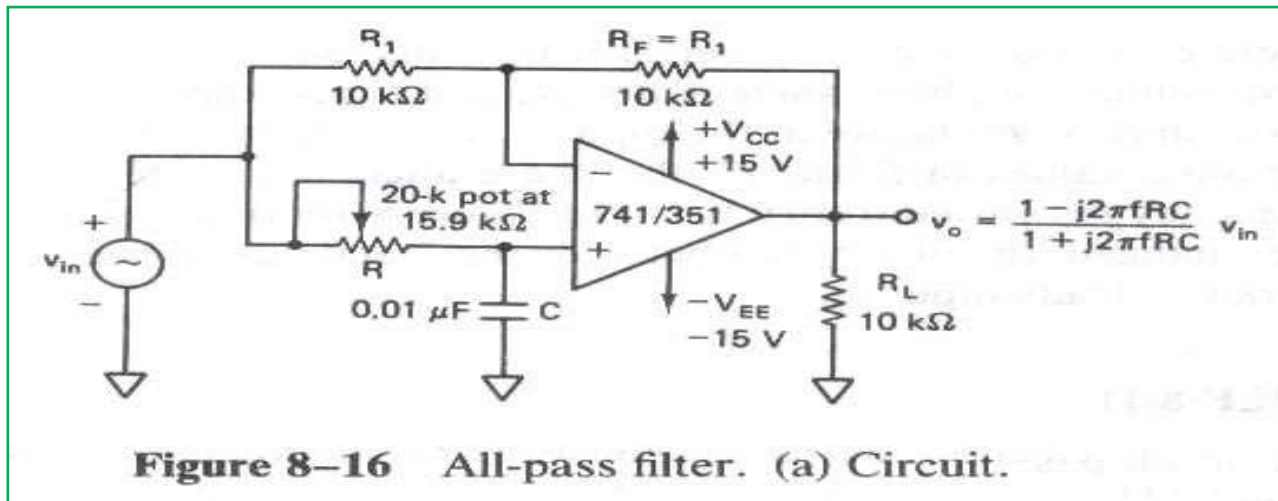


Figure 8-16 All-pass filter. (a) Circuit.

ACTIVE FILTERS

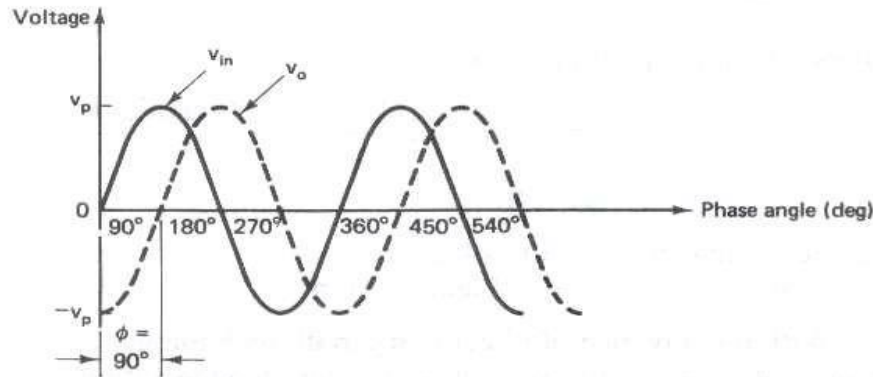


Figure 8-16 (b) Phase shift between input and output voltages.

But $-j = 1/j$ and $X_C = 1/2\pi fC$. Therefore, substituting for X_C and simplifying, we get

$$v_o = v_{in} \left(-1 + \frac{2}{j2\pi fRC + 1} \right)$$

$$\frac{v_o}{v_{in}} = \frac{1 - j2\pi fRC}{1 + j2\pi fRC}$$

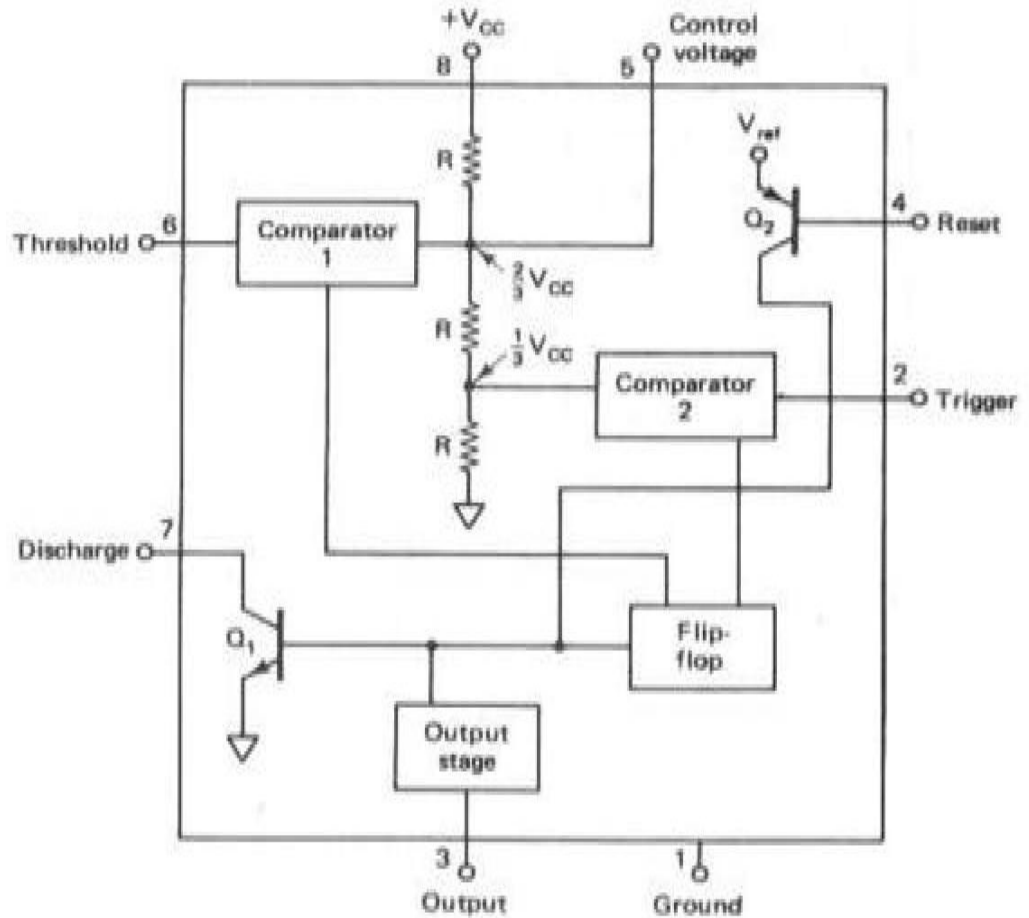
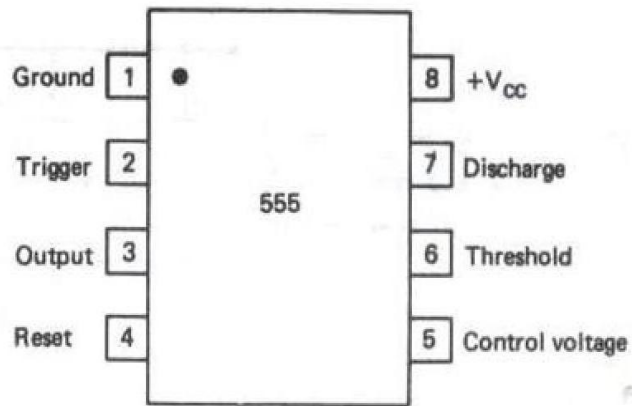
Where f is the frequency of the input signal in hertz.

Equation indicates that the amplitude of V_o/V_{in} is unity; that is, $|V_o|=|V_{in}|$ throughout the useful frequency range, and the phase shift between V_o and V_{in} is a function of input frequency f . The phase angle ϕ is given by

$$\phi = -2 \tan^{-1} \left(\frac{2\pi fRC}{1} \right)$$

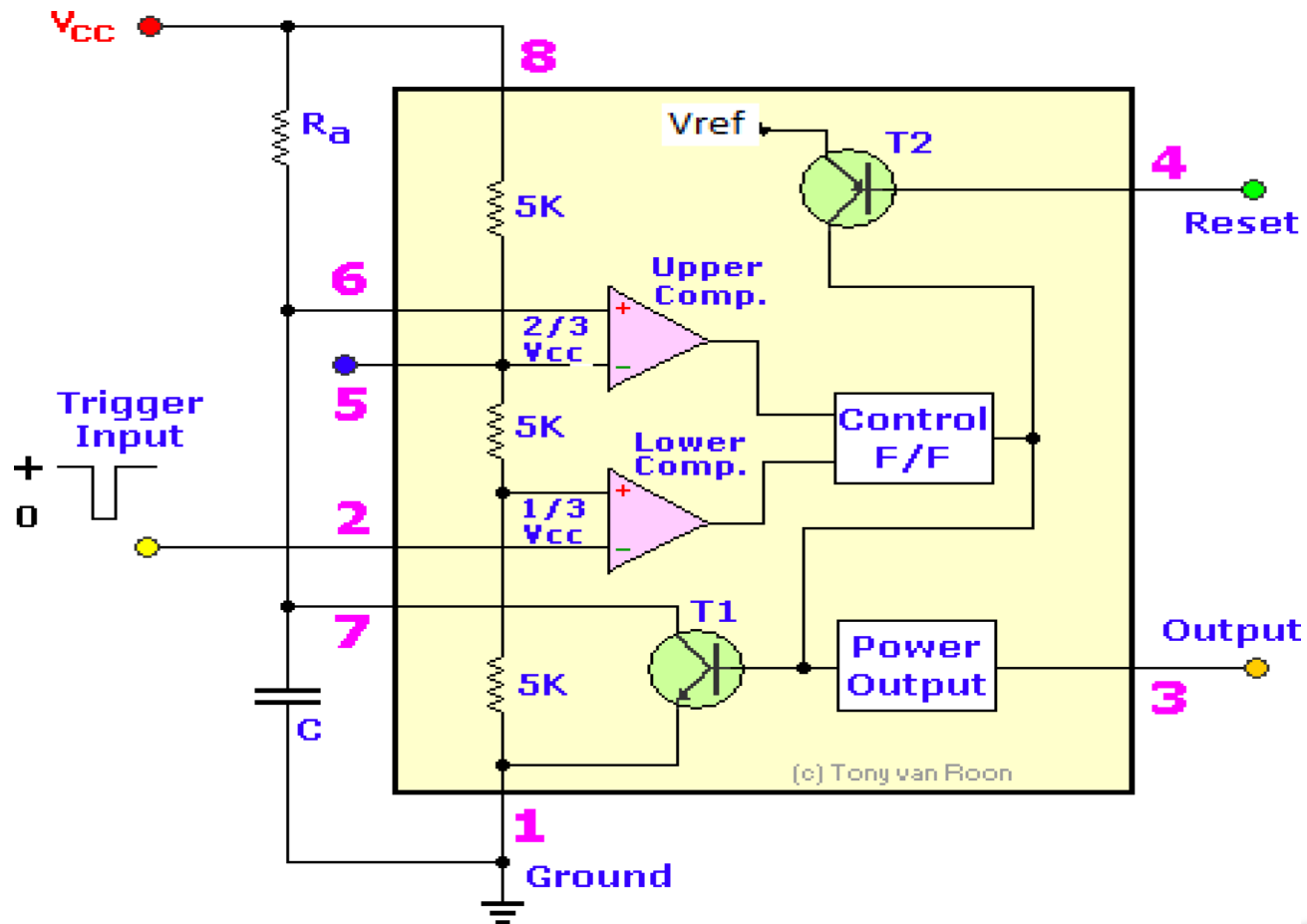
TIMER

INTRODUCTION TO 555 TIMER:



TIMER

FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER:



TIMER

THE 555 AS A MONOSTABLE MULTIVIBRATOR

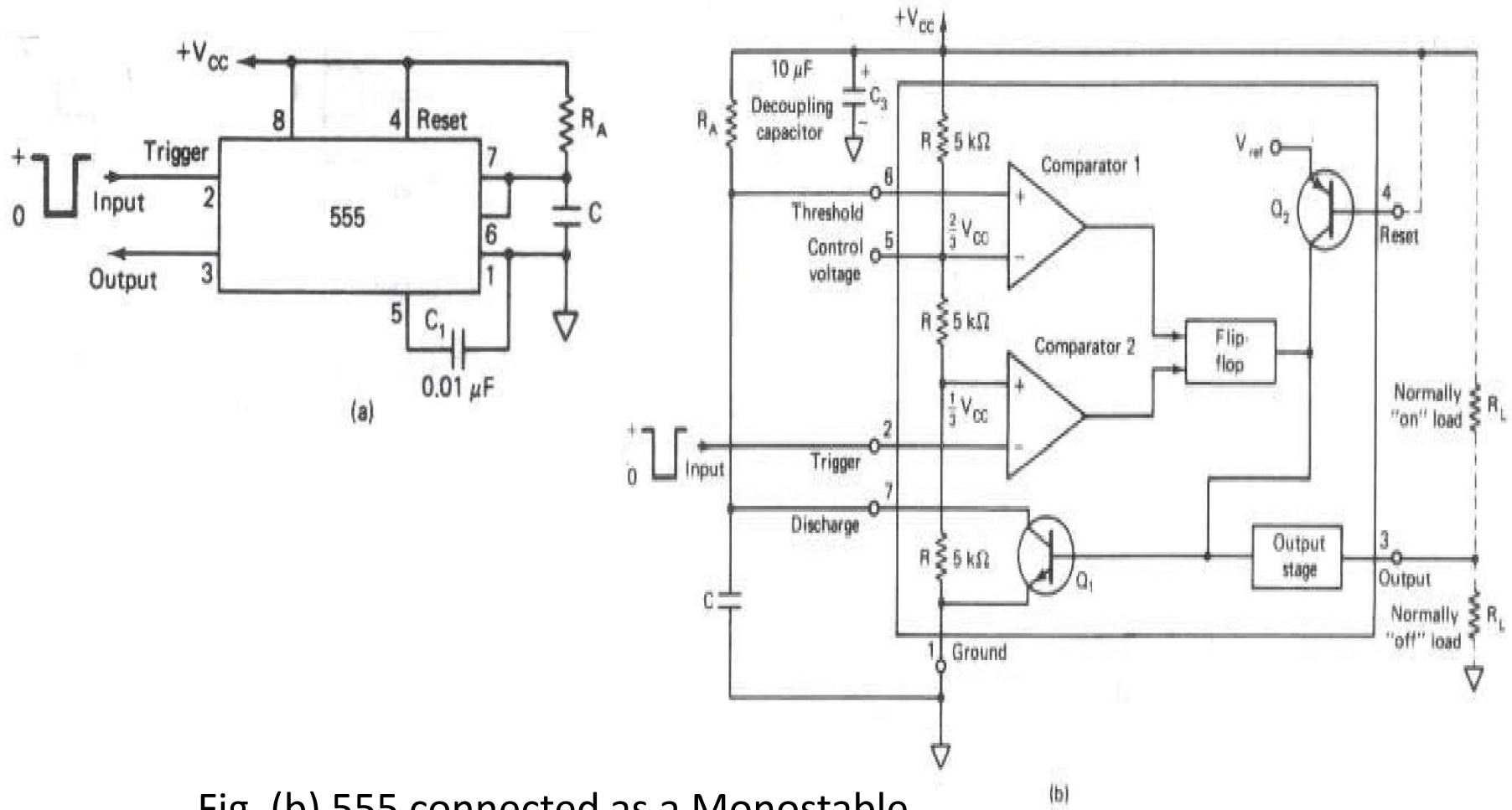
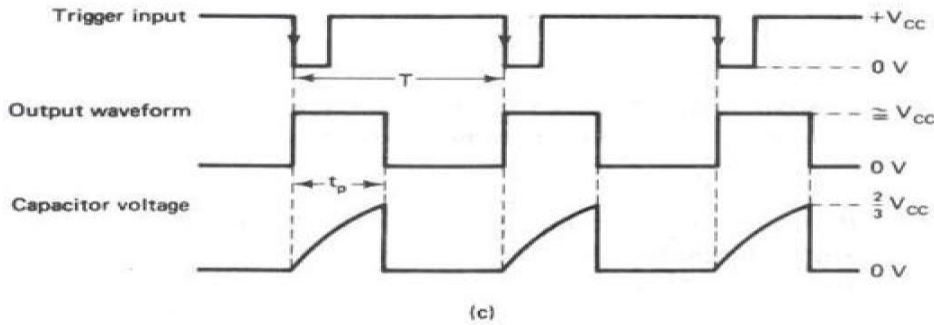
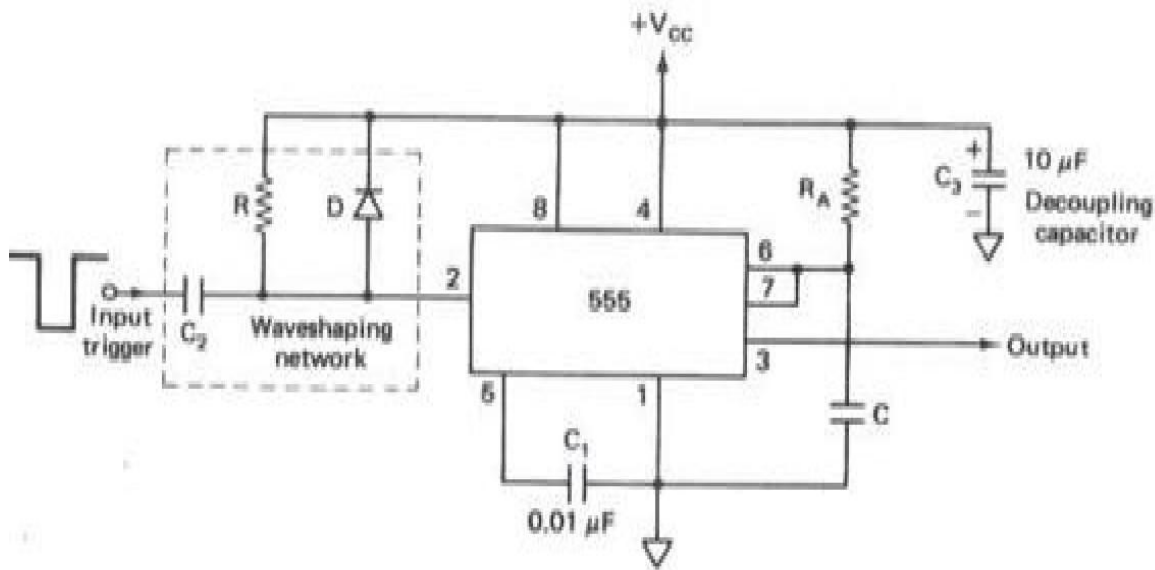


Fig. (b) 555 connected as a Monostable

TIMER



input and output waveforms

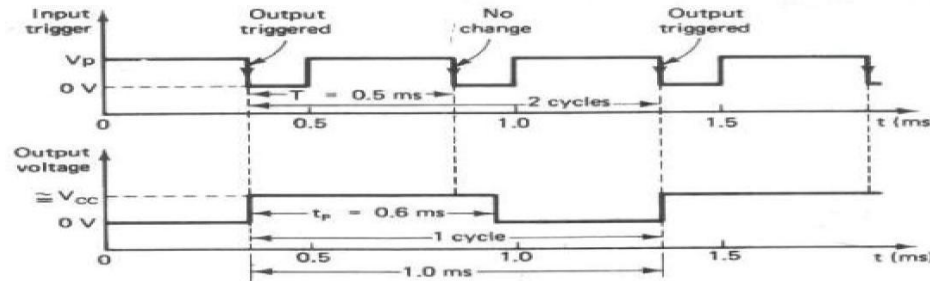


Monostable
Multivibrator with
wave shaping network
to prevent +ve pulse
edge triggering

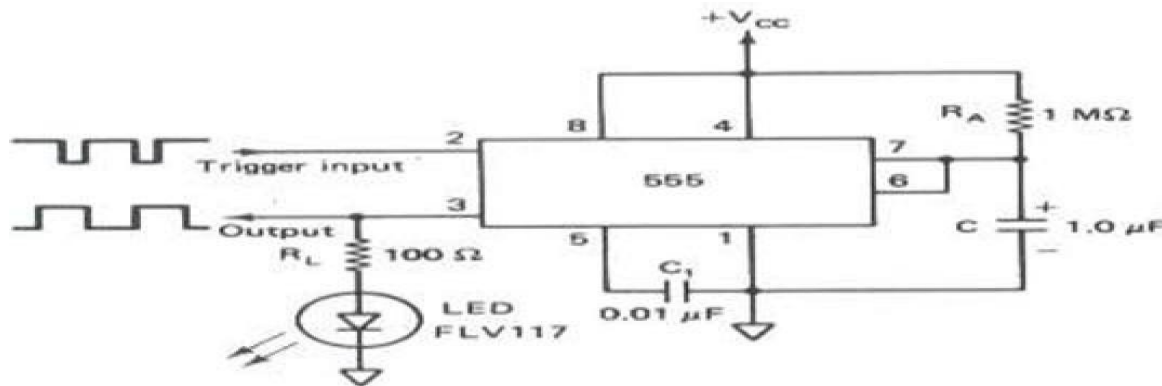
TIMER

Monostable Multivibrator Applications

Frequency divider

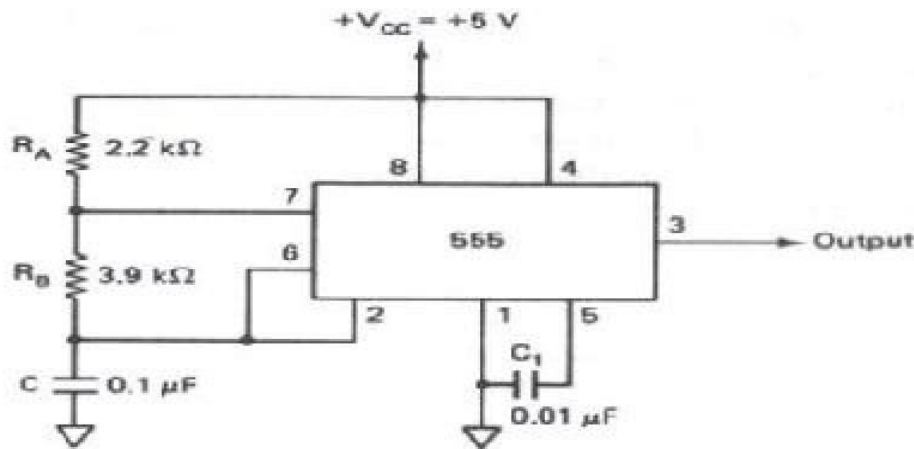


Pulse stretcher:

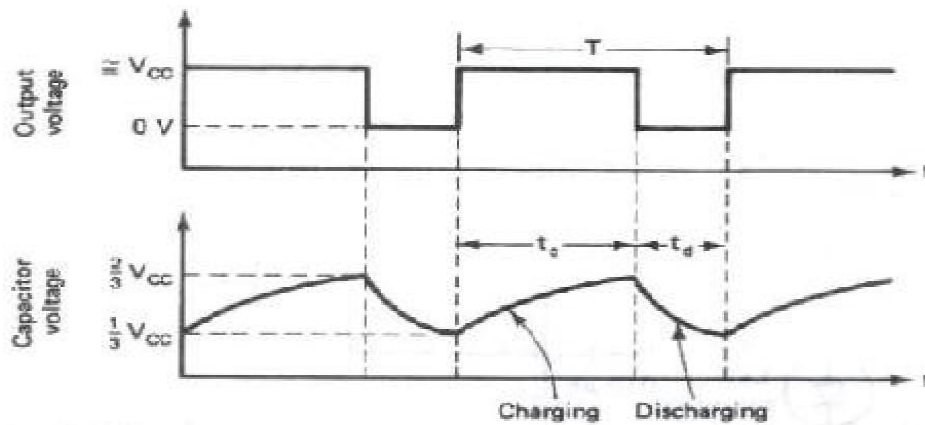


TIMER

THE 555 AS AN ASTABLE MULTIVIBRATOR:



(a)



(b)

$$t_c = 0.69(R_A + R_B)C$$

$$t_d = 0.69(R_B)C$$

$$T = t_c + t_d = 0.69(R_A + 2R_B)C$$

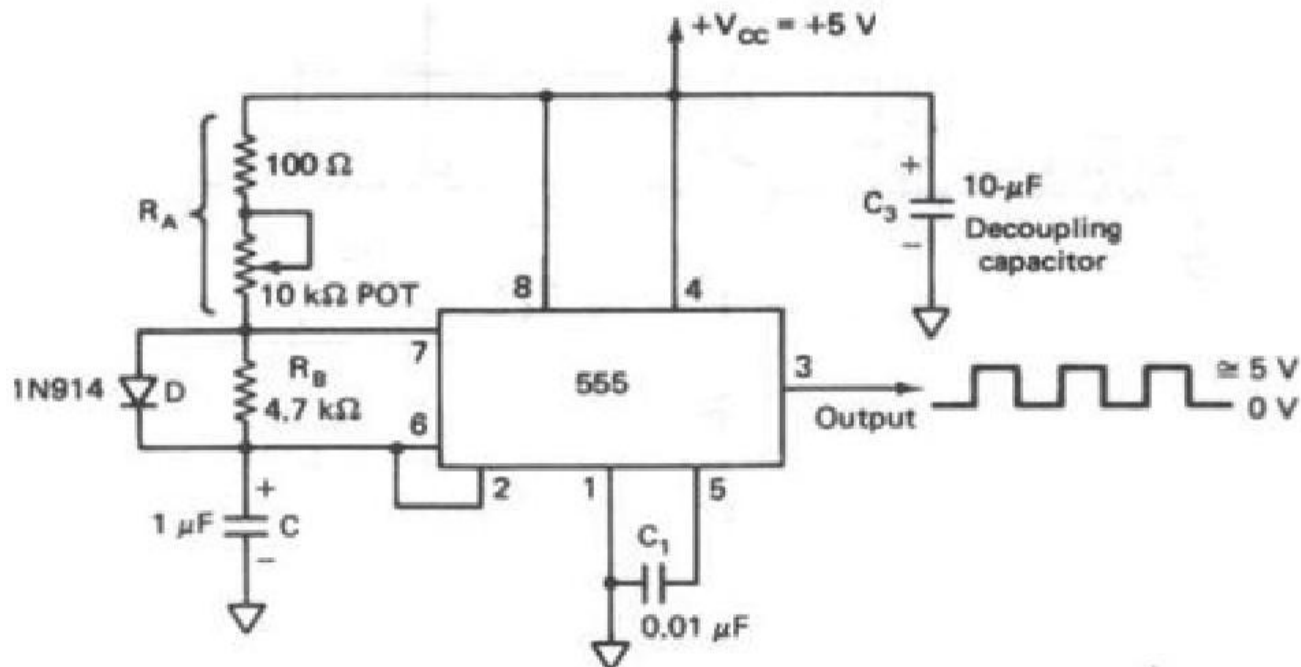
$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

$$\% \text{ duty cycle} = \frac{t_c}{T} \times 100$$

TIMER

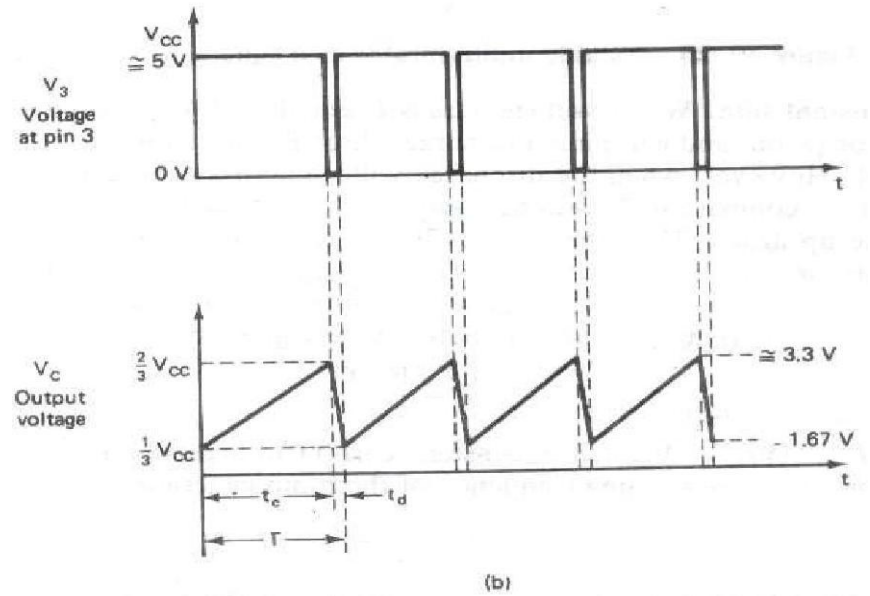
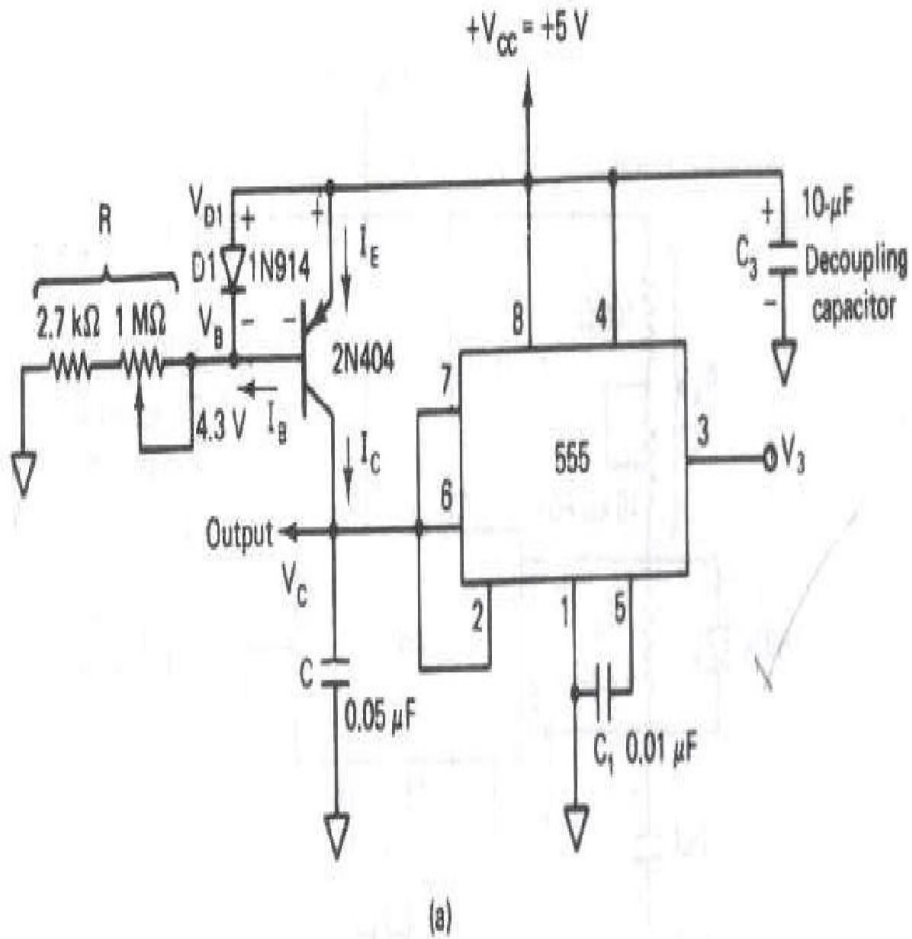
Astable Multivibrator Applications:

- Square-wave oscillator



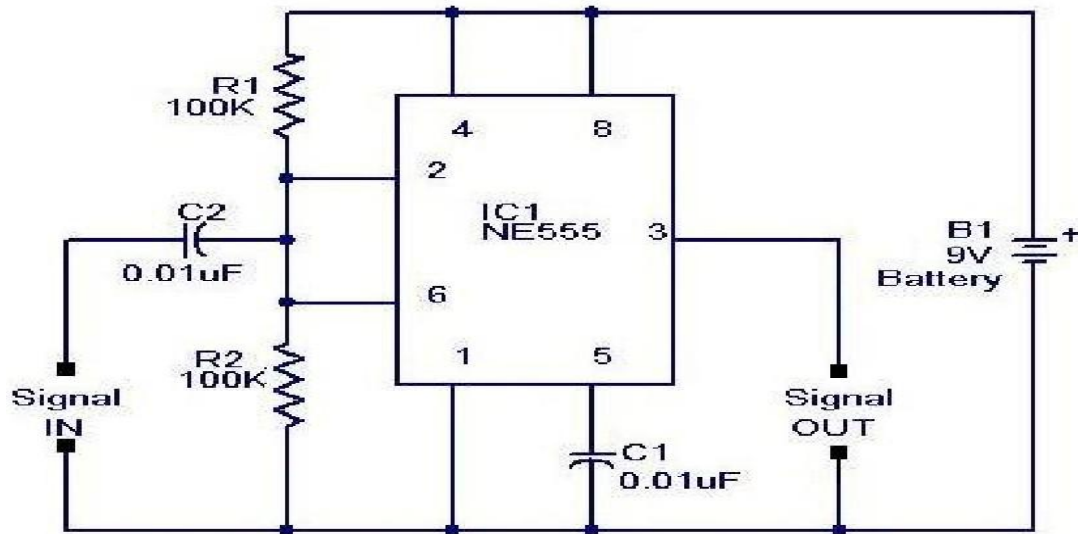
TIMER

Free-running ramp generator:



TIMER

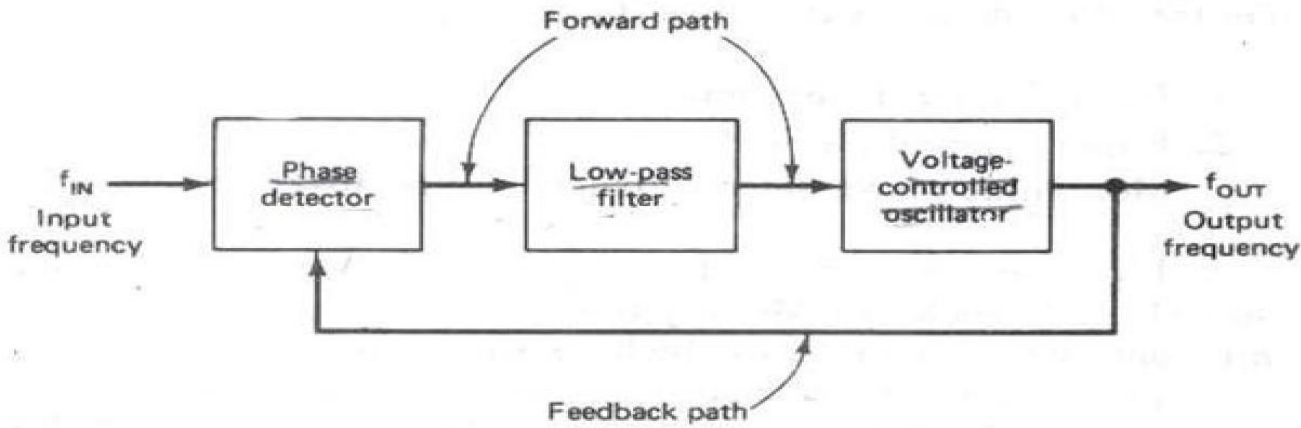
SCHMITT TRIGGER:



PHASE-LOCKED LOOPS

Block Schematic and Operating Principle

TIMER



Phase detector:

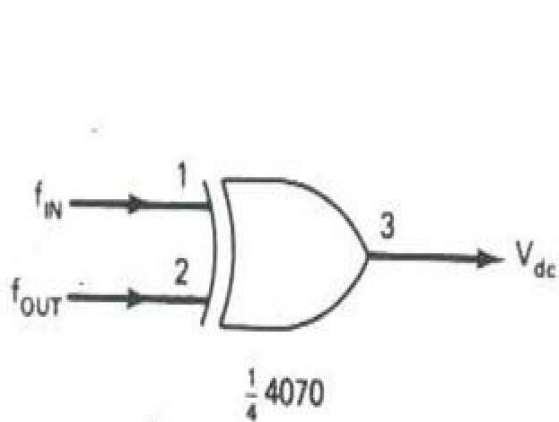
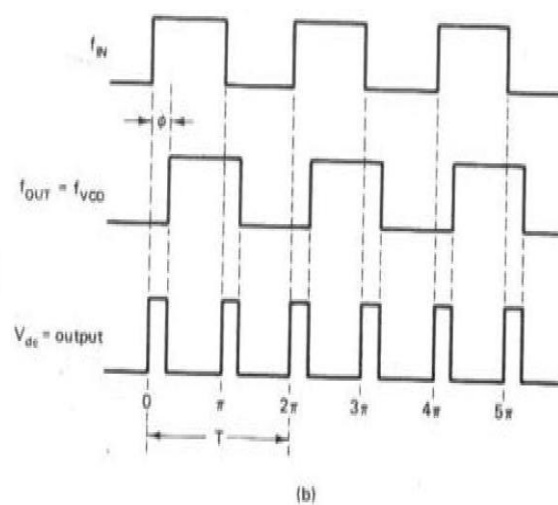


Fig (a)



(b)

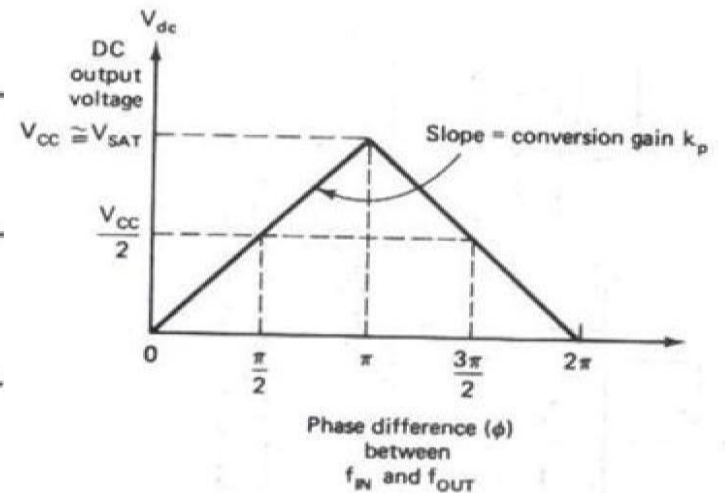


Fig (c)

TIMER

Low-pass filter.

The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

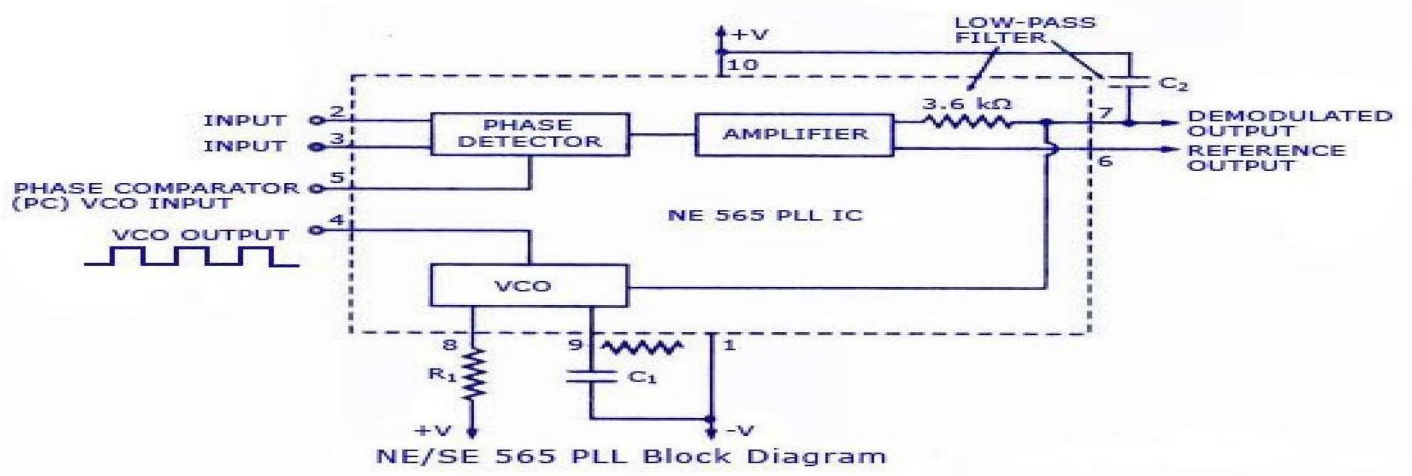
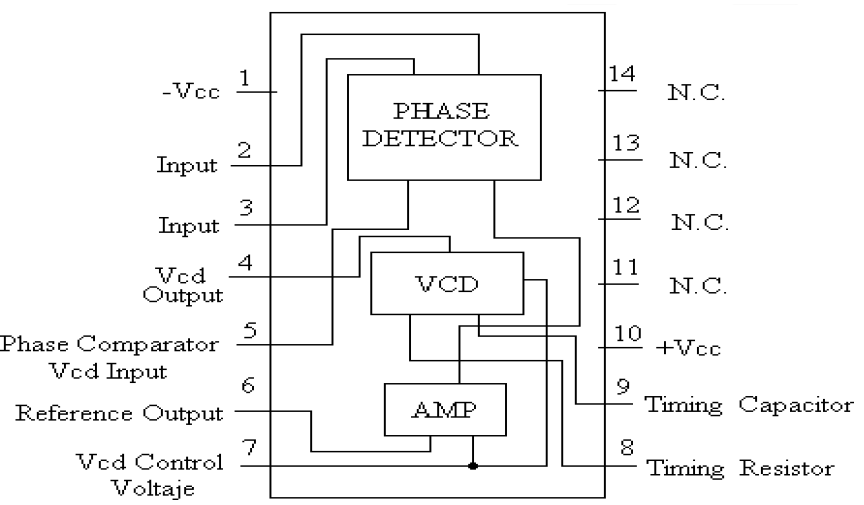
More important, the low-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency f_{IN} . An equivalent term for lock range is tracking range. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

Voltage-controlled oscillator:



TIMER

MONOLITHIC PHASE LOCK LOOPS IC 565





Unit-IV

DATA CONVERTERS



DATA CONVERTERS

Introduction:

- In electronics a digital to analog converter is a system that converts a digital signal into analog signal.
- An analog to digital converter is a system that converts a analog signal into digital signal.

DATA CONVERTERS

- **Classification of ADCs**
 - Direct type ADC.
 - Integrating type ADC
- **Direct type ADCs**
 - Flash (comparator) type converter
 - Counter type converter
 - Tracking or servo converter.
 - Successive approximation type converter

Integrating type converters:

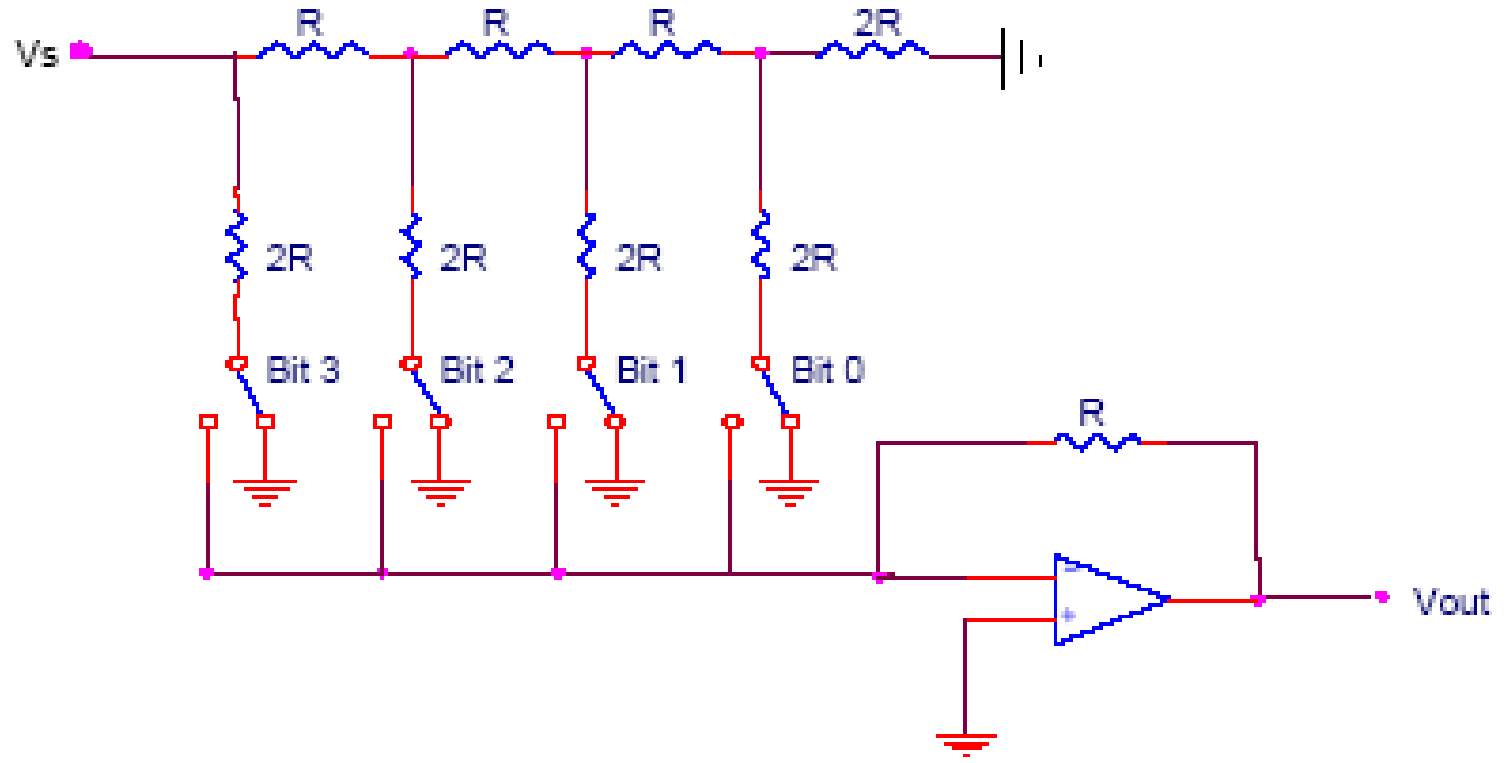
An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter.

DAC Techniques-Weighted resistor DAC, R-2R ladder DAC

DAC Techniques

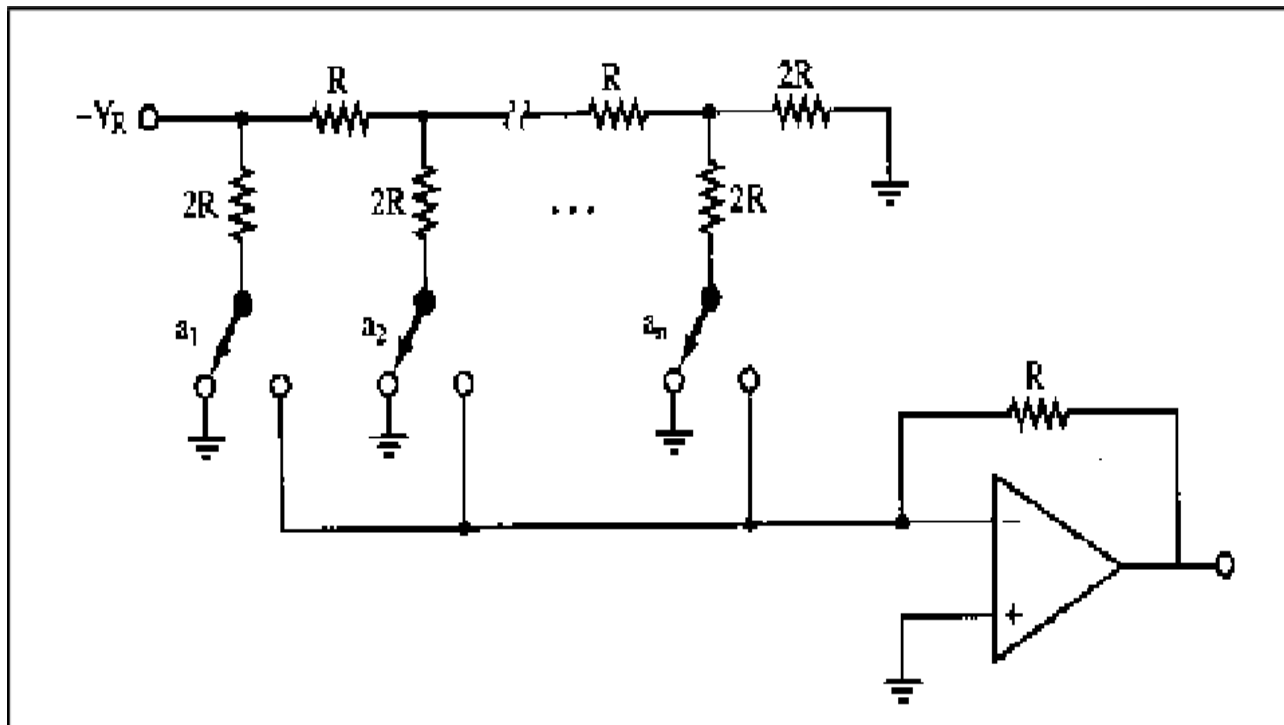
- Weighted resistor DAC
- R-2R ladder DAC
- Inverted R-2R ladder DAC
- IC 1408 DAC

DAC Techniques



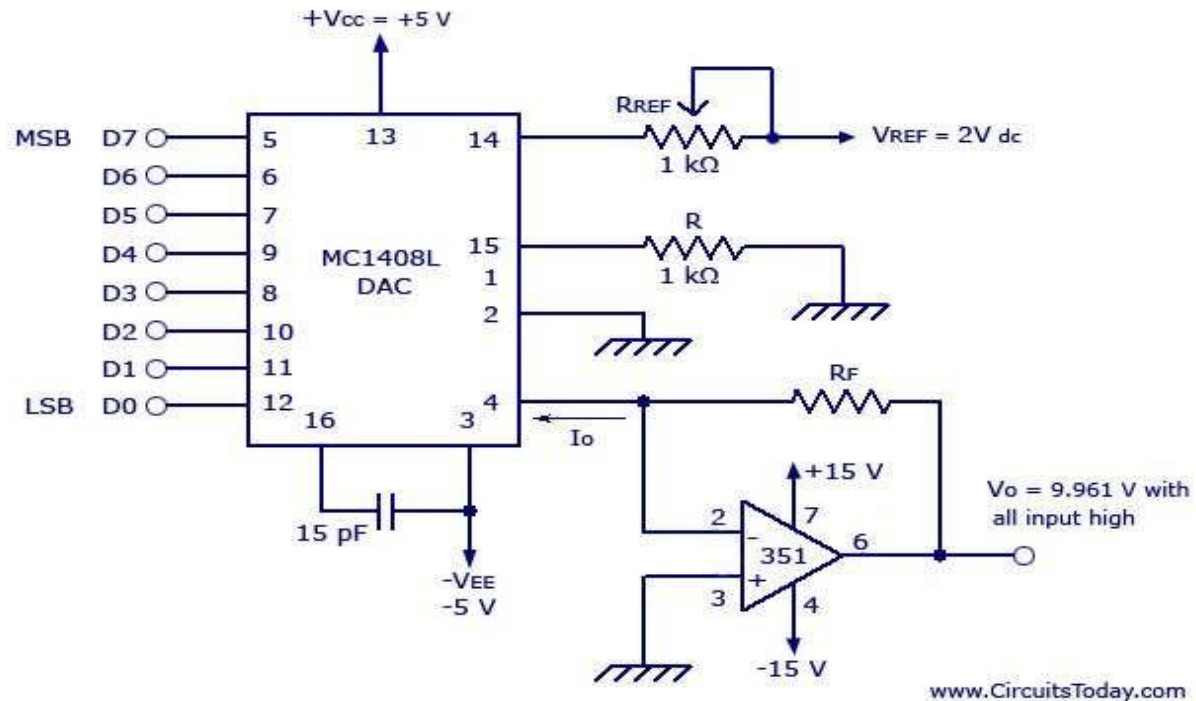
IC 1408 DAC & Inverted R-2R DAC

Inverted R-2R DAC



IC 1408 DAC & Inverted R-2R DAC

IC 1408 DAC



MC1408 D/A Converter With Current Output

IC 1408 DAC & Inverted R-2R DAC

IC 1408 DAC Specifications:

- Resolution
- Non-linearity or Linearity Error
- Gain error and Offset Error
- Settling Time

IC 1408 DAC Applications:

- Microcomputer interfacing
- CRT Graphics Generation
- Programmable Power Supplies
- Digitally controlled gain circuits
- Digital Filters

DAC Characteristics and specifications

DAC characteristics and specifications

DAC characteristics:

- Resolution
- Reference Voltage
- Speed
- Settling Time
- Linearity

DAC characteristics and specifications

Resolution:

- The change in output voltage for a change of the LSB.
- Related to the size of the binary representation of the voltage. (8-bit)
- Higher resolution results in smaller steps between voltage values

Reference Voltage:

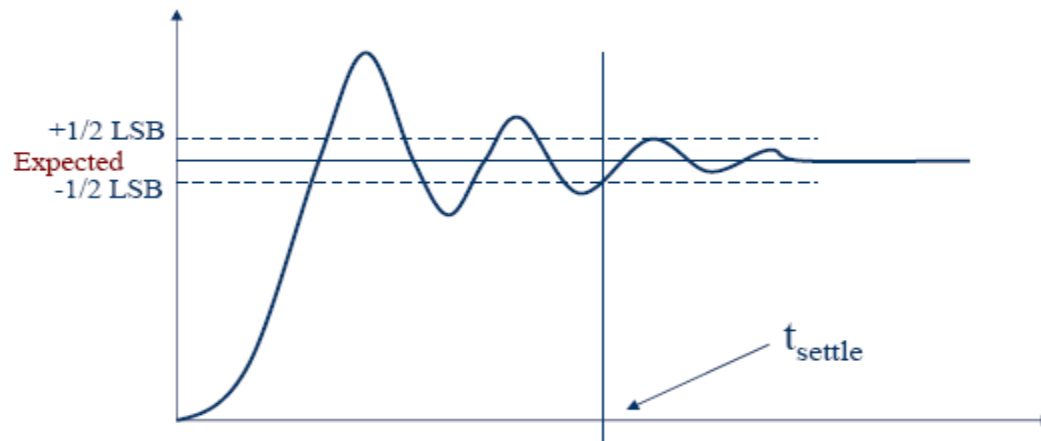
- Multiplier DAC
 - Reference voltage is a constant set by the manufacturer
- Non-Multiplier DAC
 - Reference voltage is variable
- Full scale Voltage
 - Slightly less than the reference voltage ($V_{\text{ref}} - V_{\text{LSB}}$)

Speed:

- Also called the conversion rate or sampling rate –rate at which the register value is updated.
- For sampling rates of over 1 MHz a DAC is designated as high speed.
- Speed is limited by the clock speed of the microcontroller and the settling time of the DAC.

Settling Time:

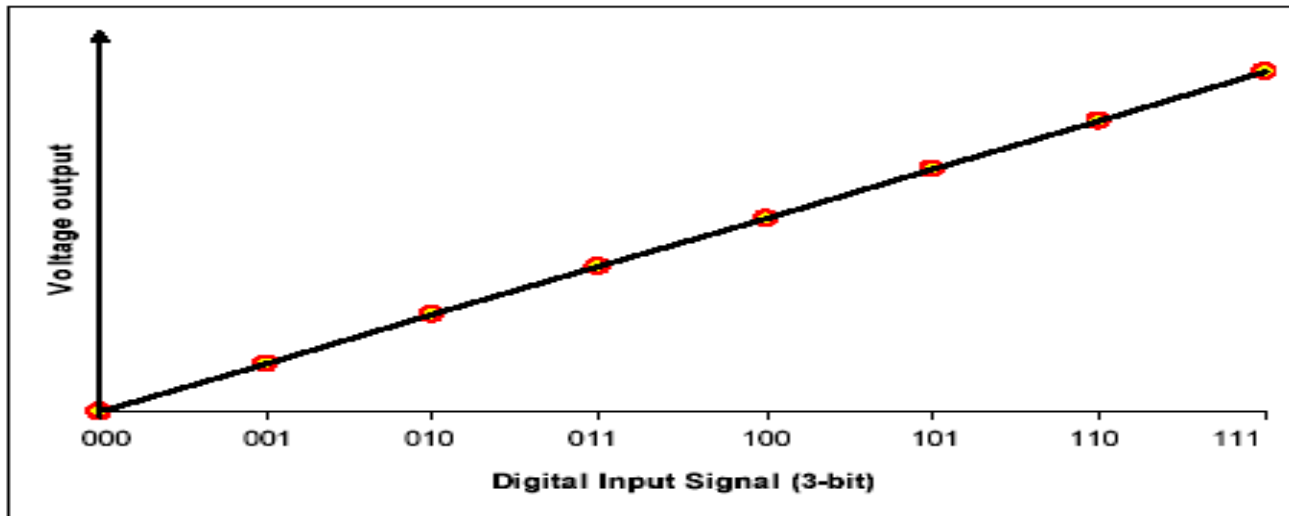
- Time in which the DAC output settles at the desired value $\pm \frac{1}{2} V_{\text{LSB}}$.
- Faster DACs decrease the settling time.



DAC characteristics and specifications

Linearity:

- Represents the relationship between digital values and analog outputs.
- Should be related by a single proportionality constant. (constant slope).



ADC Techniques:

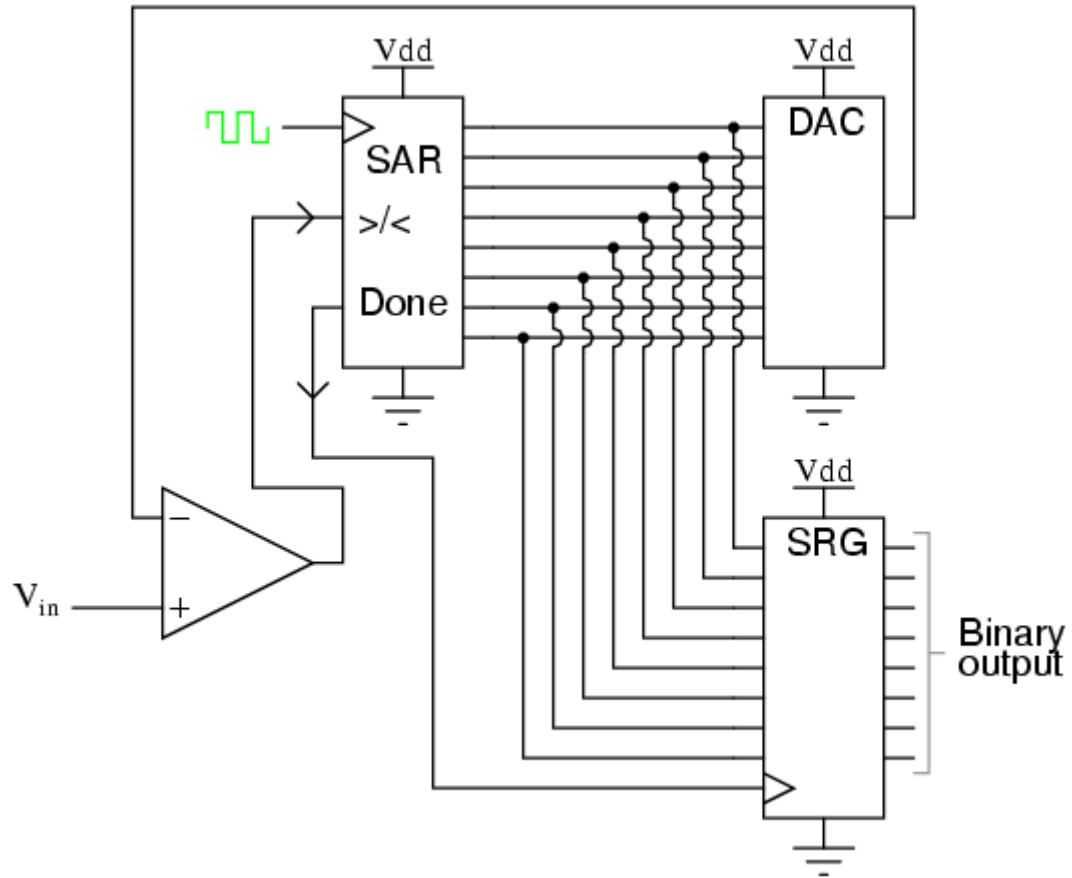
- Flash ADC
- Sigma-delta ADC
- Dual slope converter
- Successive approximation converter

Successive Approximation ADC

SUCCESSIVE APPROXIMATION

- A Successive Approximation Register (SAR) is added to the circuit
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the MSB and finishing at the LSB.
- The register monitors the comparators output to see if the binary count is greater or less than the analog signal input and adjusts the bits accordingly

SUCCESSIVE APPROXIMATION



Advantages

- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format.

Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to $\sim 5\text{Msamples/s}$

FLASH CONVERTERS & ADC CHARACTERISTICS

FLASH CONVERTERS

- Consists of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output

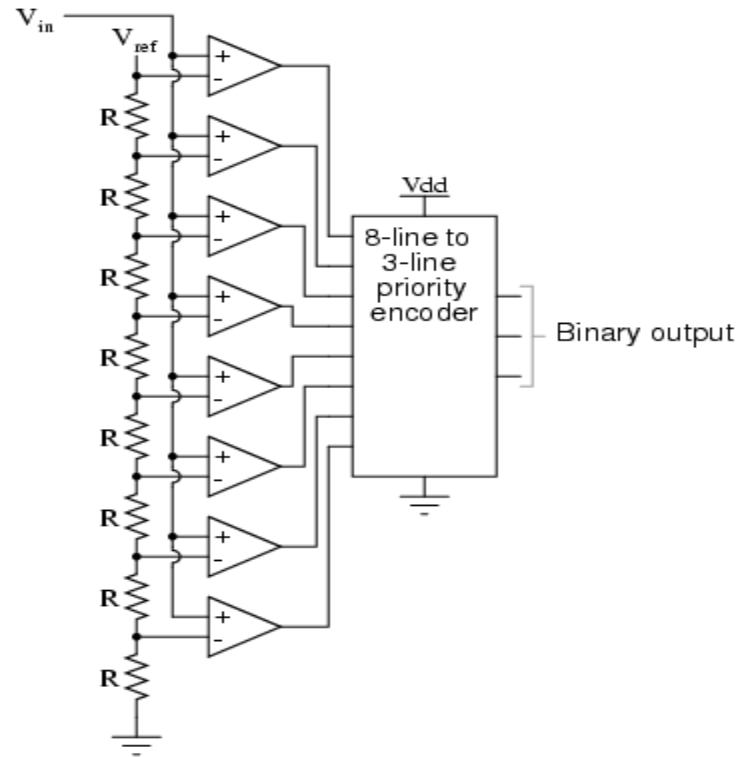
FLASH CONVERTER, ADC CHARACTERISTICS



FLASH CONVERTERS

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- The comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output

FLASH CONVERTERS



FLASH CONVERTER, ADC CHARACTERISTICS

FLASH CONVERTERS

- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.
- The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

FLASH CONVERTERS -Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
- limited only in terms of comparator and gate propagation delays

Disadvantages

- Lower resolution
- Expensive
- For each additional output bit, the number of comparators is doubled
 - i.e. for 8 bits, 256 comparators needed

ADC characteristics

- **Resolution**
- **Accuracy**
- **Sampling rate**
- **Aliasing**

Resolution

The resolution of the converter indicates the number of discrete values it can produce. It is usually expressed in bits. For example, an ADC that encodes an analogue input to one of 256 discrete values has a resolution of

Resolution can also be defined electrically, and expressed in volts.

FLASH CONVERTER, ADC CHARACTERISTICS

- **Accuracy** : Accuracy depends on the error in the conversion. If the ADC is not broken, this error has two components: quantization error and (assuming the ADC is intended to be linear) non-linearity. These errors are measured in a unit called the LSB, which is an abbreviation for least significant bit. In the above example of an eight-bit ADC, an error of one LSB is $1/256$ of the full signal range, or about 0.4%.

FLASH CONVERTER, ADC CHARACTERISTICS

Sampling rate

- The analogue signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analogue signal. The rate of new values is called the sampling rate or sampling frequency of the converter.

FLASH CONVERTER, ADC CHARACTERISTICS

Aliasing

- If the digital values produced by the ADC are, at some later stage in the system, converted back to analogue values by a digital to analogue converter or DAC, it is desirable that the output of the DAC be a faithful representation of the original signal.
- If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals called aliases will be produced at the output of the DAC.
- The frequency of the aliased signal is the difference between the signal frequency and the sampling rate.

FLASH CONVERTER, ADC CHARACTERISTICS

FLASH CONVERTERS -Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
- limited only in terms of comparator and gate propagation delays

Disadvantages

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 - i.e. for 8 bits, 256 comparators needed

FLASH CONVERTER, ADC CHARACTERISTICS

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Unit-V

DIGITAL IC APPLICATIONS



CLASSIFICATION OF IC 'S:

Based on mode of operation

Linear IC's

Digital IC's

Linear IC's: Linear IC's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers, and modulators that often require additional external components for satisfactory operation.

Digital IC's: Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.

CLASSIFICATION OF DIGITAL INTEGRATED CIRCUIT

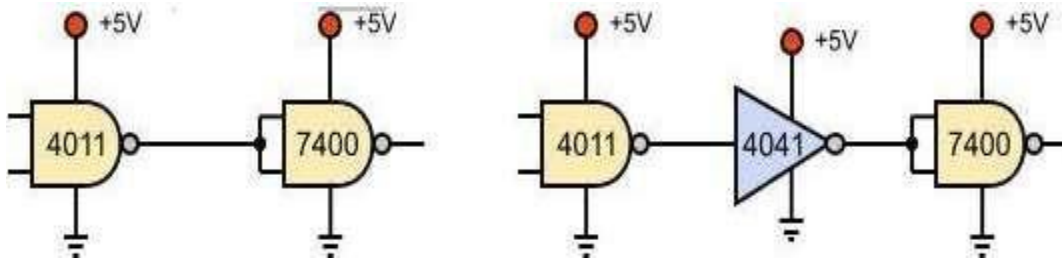
Classification of ICs based on complexity

- Medium Scale Integration or (MSI)
- Large Scale Integration or (LSI)
- Very-Large Scale Integration or (VLSI)
- Super-Large Scale Integration or (SLSI)
- Ultra-Large Scale Integration or (ULSI)

Logic delay, TTL/CMOS interfacing

CMOS DRIVING TTL AND CMOS DRIVING TTL

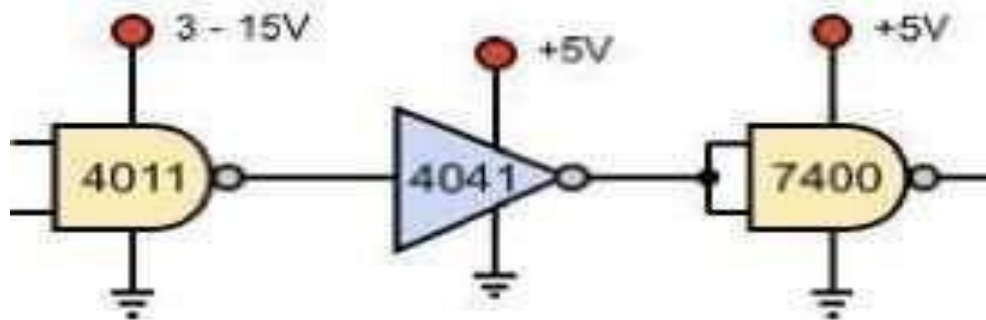
Interfacing a CMOS to a TTL under 5Volts power supply



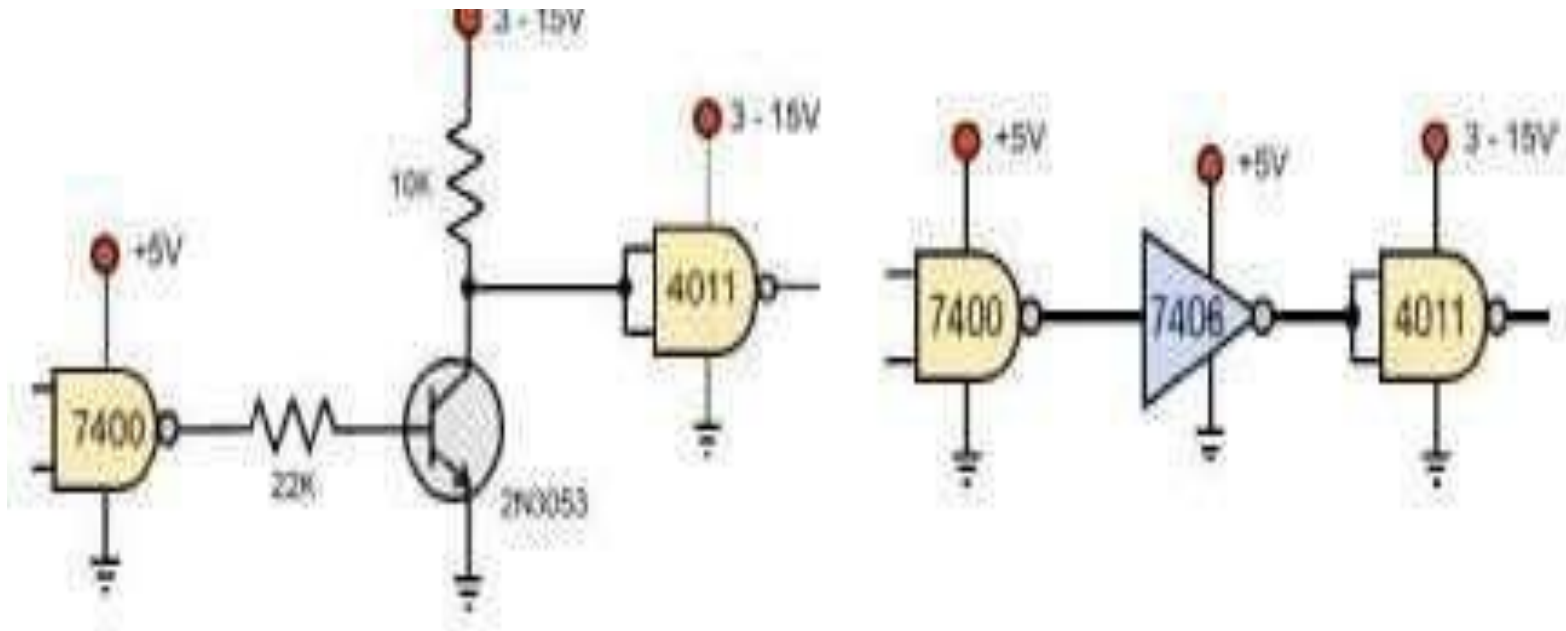
Logic delay, TTL/CMOS interfacing

Interfacing ICs with different power supply voltages:

Interfacing a CMOS to a TTL with different power supply voltages



Interfacing a TTL to a CMOS with different power supply voltages



Adders



Adders

The Half Adder

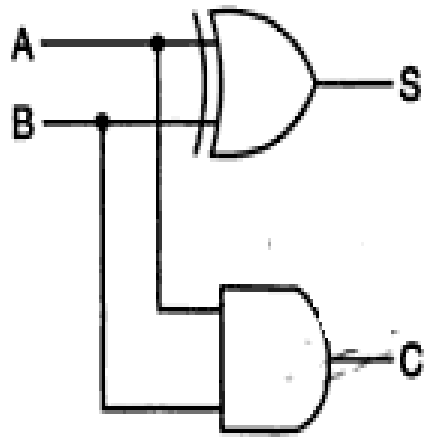
Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a) Truth table

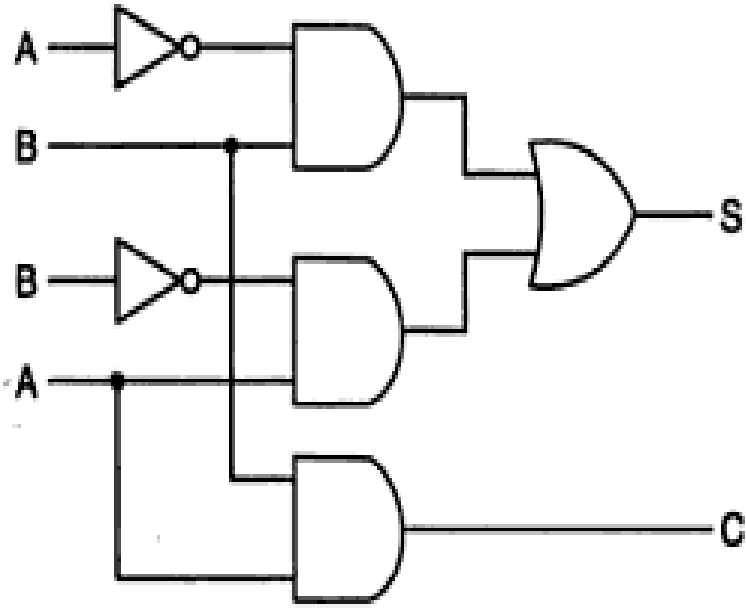


(b) Block diagram

ADDER



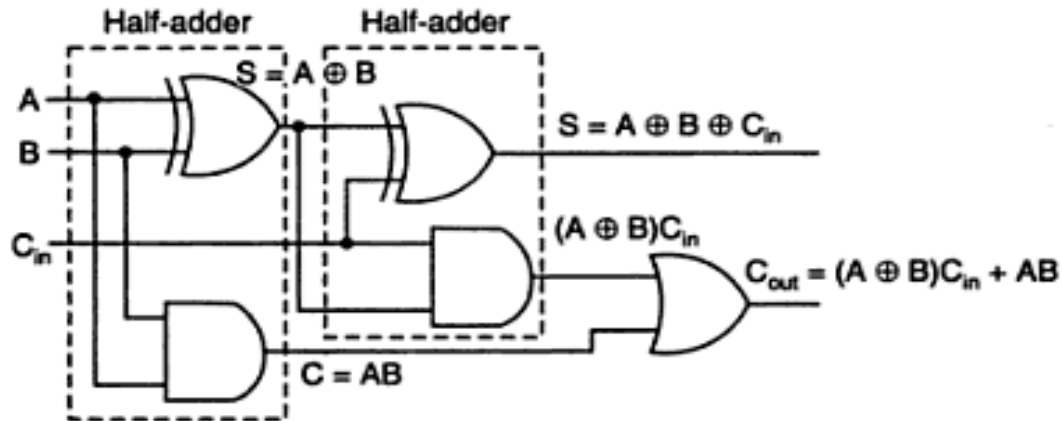
(a)



(b)

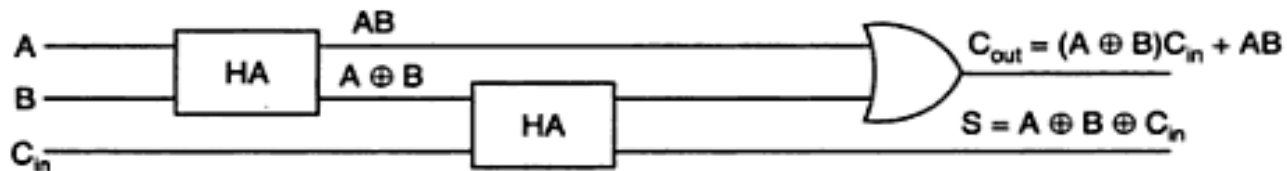
ADDER

The Full Adder:



Logic diagram of a full-adder using two half-adders.

The block diagram of a full-adder using two half-adders is :



Block diagram of a full-adder using two half-adders.

ADDER

Inputs			Sum	Carry
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Truth table



(b) Block diagram

Full-adder.

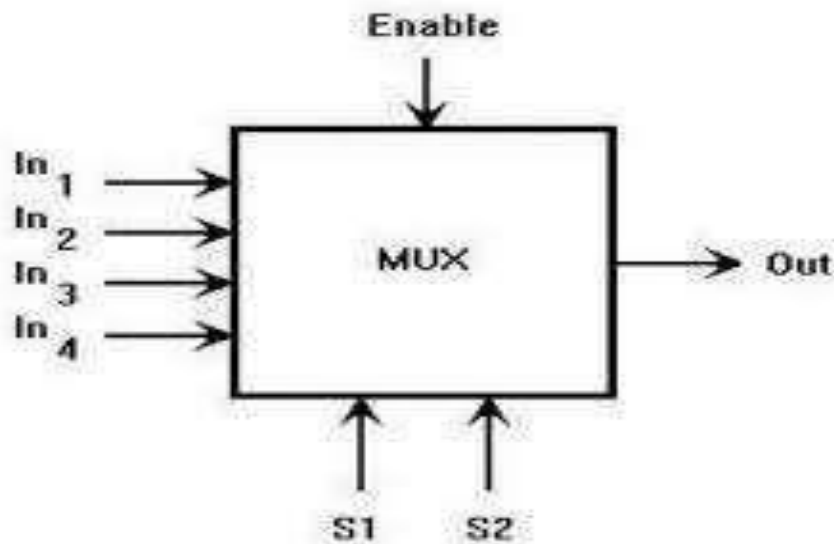
TYPES OF ADDERS

- Binary Parallel Adder
- Ripple carry adder
- The Look-Ahead –Carry Adder
- Serial Adder

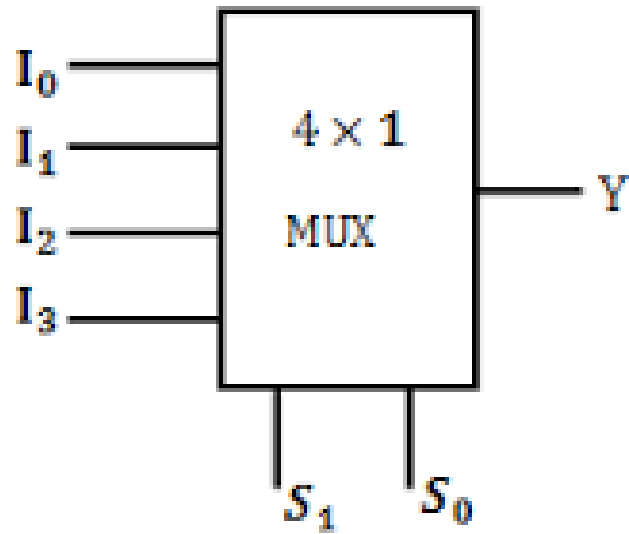
MULTIPLIXER AND DEMULTIPLIXER

Multiplexer:

Multiplexer is a digital switch. it allows digital information from several sources to be routed onto a single output line



MULTIPLIXER AND DEMULTIPLIXER



Truth table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

MULTIPLIXER AND DEMULTIPLIXER

Applications of multiplexer:

- The logic function generator
- Digital counter with multiplexed displays
- Data selection and data routing
- Parallel to serial conversion

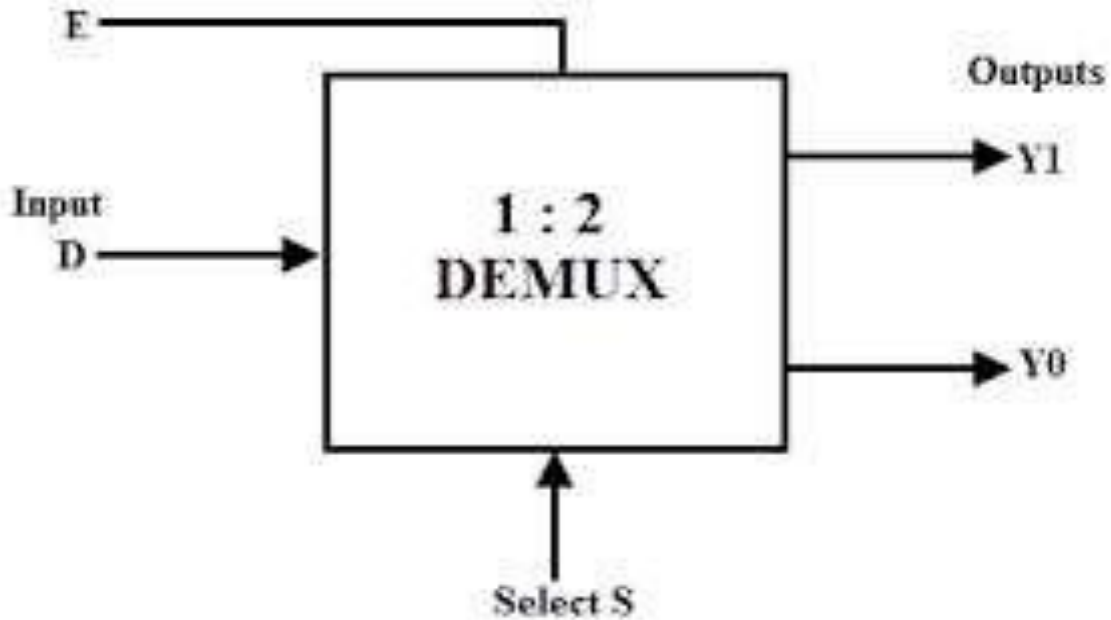
MULTIPLIXER AND DEMULTIPLIXER

A demultiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input. A demultiplexer is also called a data distributor.

Applications of Demultiplexer:

- Data distributor
- Security monitoring system
- Synchronous data transmission system

MULTIPLIXER AND DEMULTIPLIXER

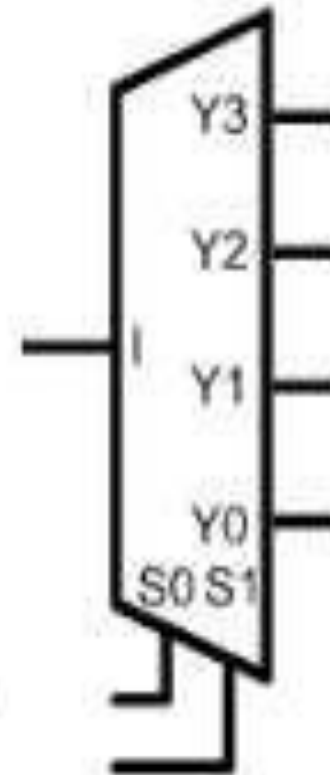


MULTIPLIXER AND DEMULTIPLIXER

SN74HC139 Demux Truth Table

INPUTS			OUTPUTS			
I (1G)	SELECT		Y0 (1Y0)	Y1 (1Y1)	Y2 (1Y2)	Y3 (1Y3)
	S1 (1B)	S0 (1A)				
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

1 = Vcc 0 = Ground X = don't care () = IC pin name



DECODER

Decoders

- The decoder is an electronic device that is used to convert digital signal to an analogue signal.
- It allows single input line and produces multiple output lines.
- The decoders are used in many communication projects that are used to communicate between two devices.
- The decoder allows N - inputs and generates 2^N power N -numbers of outputs.
- For example, if we give 2 inputs that will produce 4 outputs by using 4 by 2 decoder.

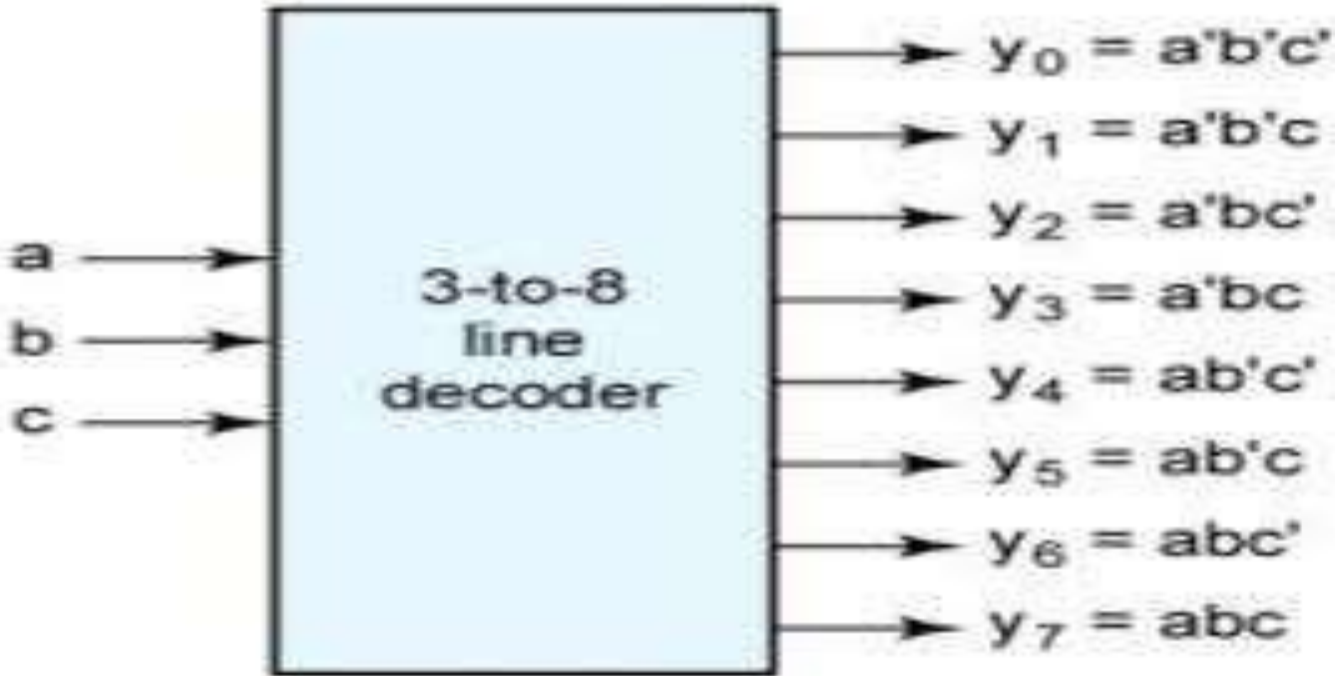
DECODER AND ENCODERS

2-to-4 line Decoder

In this type of encoders and decoders, decoders contain two inputs A0, A1, and four outputs represented by D0, D1, D2, and D3. As you can see in the truth table – for each input combination, one output line is activated.

Inputs		Output			
A	B	D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

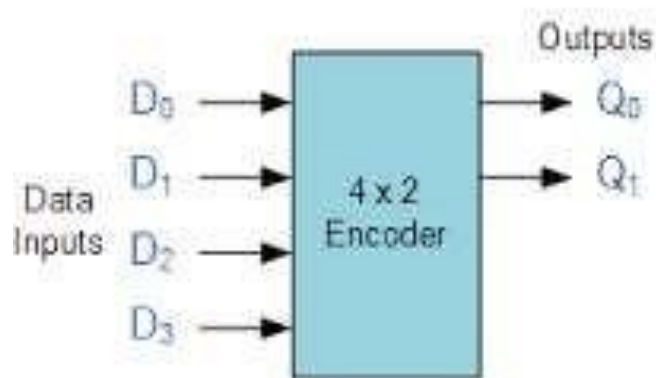
DECODER AND ENCODERS



Decoders and Encoder

Encoder:

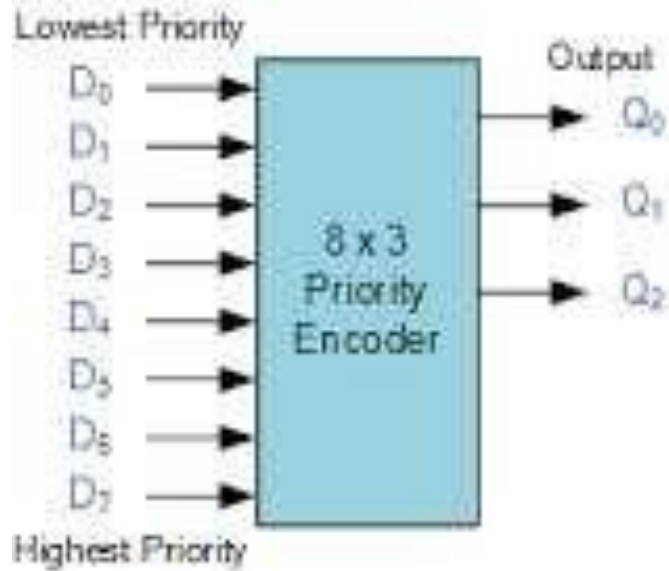
- An encoder is multiple input and multiple output combinational circuit it performs reverse operation of a decoder.



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Table

Decoders and Encoder



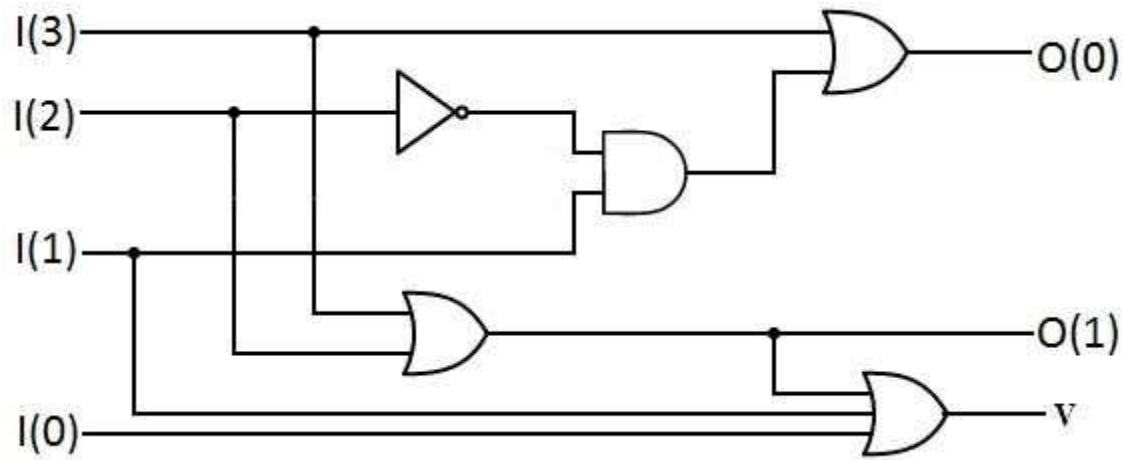
Inputs								Outputs		
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Q ₂	Q ₁	Q ₀
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

x = don't care

Priority Encoder

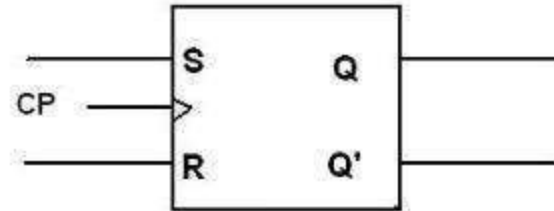
- **priority encoder** is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs.
- The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit.
- They are often used to control interrupt requests by acting on the highest priority encoder.

Decoders and Encoder

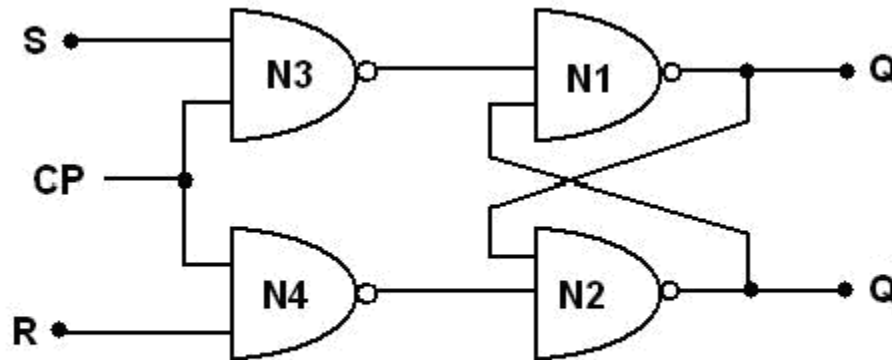


SR,JK,T AND D FLIPFLOP

RS Flip-flop:



b) Block diagram



a) Logic diagram

SR,JK,T AND D FLIPFLOP

Operation:

1. When $CP=0$ the output of N3 and N4 are 1 regardless of the value of S and R. This is given as input to N1 and N2. This makes the previous value of Q and Q' unchanged.
2. When $CP=1$ the information at S and R inputs are allowed to reach the latch and change of state in flip-flop takes place.
3. $CP=1, S=1, R=0$ gives the SET state i.e., $Q=1, Q'=0$.
4. $CP=1, S=0, R=1$ gives the RESET state i.e., $Q=0, Q'=1$.
5. $CP=1, S=0, R=0$ does not affect the state of flip-flop.
6. $CP=1, S=1, R=1$ is not allowed, because it is not able to determine the next state. This condition is said to be a —race condition||.

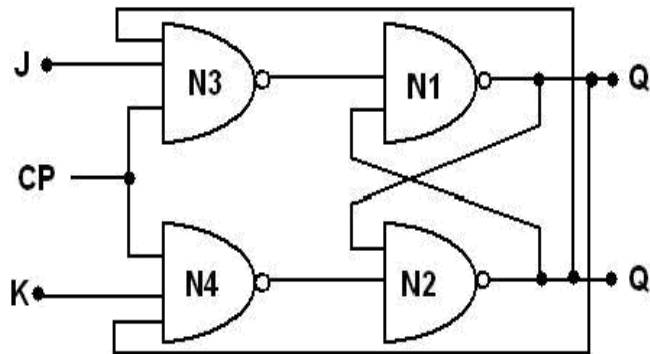
SR,JK,T AND D FLIPFLOP

Truth table

S	R	$Q_{(t+1)}$	Comments
0	0	Q_t	No change
0	1	0	Reset / clear
1	0	1	Set
1	1	*	Not allowed

SR,JK,T AND D FLIPFLOP

JK flip-flop (edge triggered JK flip-flop)



a) Logic diagram



b) Block diagram

SR,JK,T AND D FLIPFLOP

Truth table

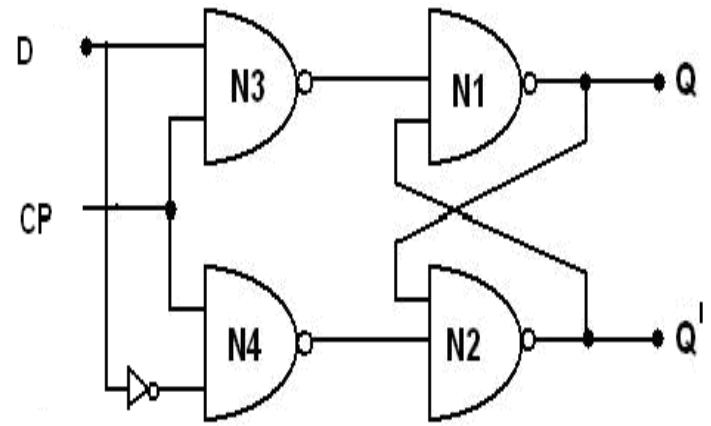
J	K	$Q_{(t+1)}$	Comments
0	0	Q_t	No change
0	1	0	Reset / clear
1	0	1	Set
1	1	Q'_t	Complement/ toggle.

SR,JK,T AND D FLIPFLOP

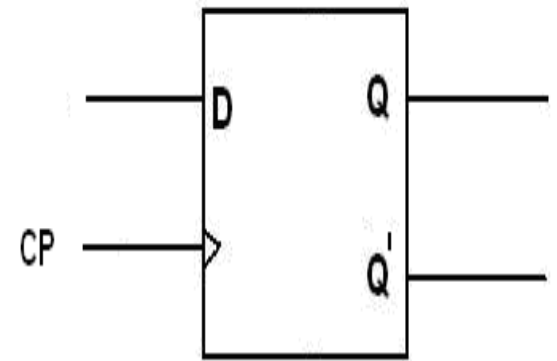
- When $J=0$, $K=0$ then both N3 and N4 will produce high output
- When $J=0$, $K=1$, N3 will get an output as 1 and output of N4 depends on the value of Q. The final output is $Q=0$, $Q'=1$ i.e., reset state
- When $J=1$, $K=0$ the output of N4 is 1 and N3 depends on the value of Q'. The final output is $Q=1$ and $Q'=0$ i.e., set state
- When $J=1$, $K=1$ it is possible to set (or) reset the flip-flop depending on the current state of output. If $Q=1$, $Q'=0$ then N4 passes '0' to N2 which produces $Q'=1$, $Q=0$ which is reset state. When $J=1$, $K=1$, Q changes to the complement of the last state. The flip-flop is said to be in the toggle state.

SR, JK, T, and D flip-flops

D flip-flop:



a) Logic diagram



b) Block diagram

SR,JK,T AND D FLIPFLOP

Operation:

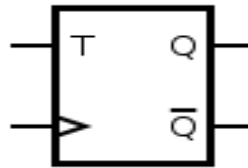
- When the clock is low both the NAND gates (N1 and N2) are disabled and Q retains its last value.
- When clock is high both the gates are enabled and the input value at D is transferred to its output Q. D flip-flop is also called —Data flip-flop||.

Truth table

CP	D	Q
0	x	Previous state
1	0	0
1	1	1

T flip-flop:

- If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed.
- If the T input is low, the flip-flop holds the previous value.



SR,JK,T AND D FLIPFLOP

T	Q	Q'
0	0	0
1	0	1
0	1	0
1	1	0

Counters

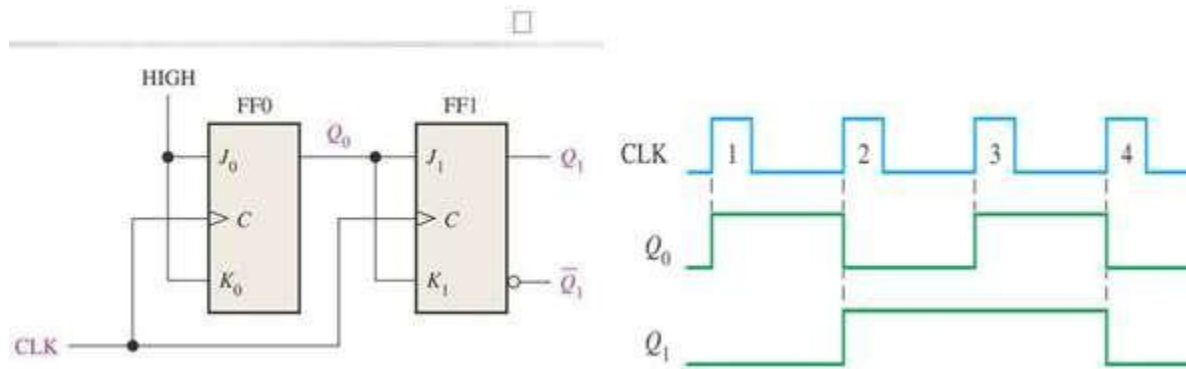
- 1) Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal.
- 2) A Digital counter is a set of flip flops whose state changes in response to pulses applied at the input to the counter.
- 3) Counters may be asynchronous counters or synchronous counters.
- 4) Asynchronous counters are also called ripple counters.

SYNCHRONOUS COUNTERS

- They are slow because each FF can change state only if all the preceding FFs have changed their state.
- If the clock frequency is very high, the asynchronous counter may skip some of the states.
- This problem is overcome in synchronous counters or parallel counters.
- Synchronous counters are counters in which all the flip flops are triggered simultaneously by the clock pulses.
- Synchronous counters have a common clock pulse applied simultaneously to all flip-flops.

SYNCHRONOUS COUNTERS

2-Bit Synchronous Binary Counter

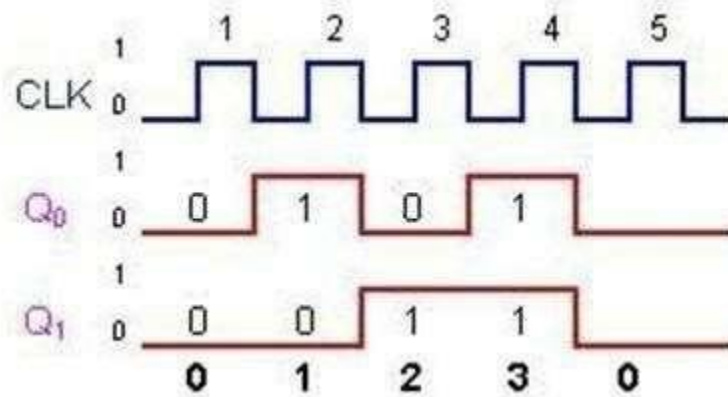
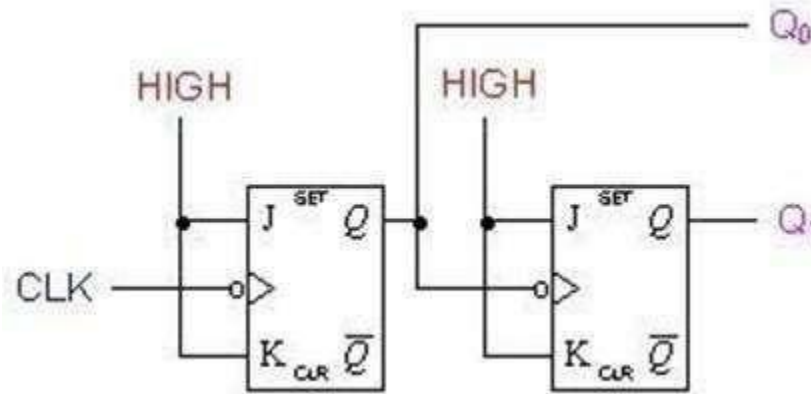


ASYNCHRONOUS COUNTERS

- An asynchronous (ripple) counter is a single JK-type flip-flop, with its J (data) input fed from its own inverted output.
- This circuit can store one bit, and hence can count from zero to one before it overflows (starts over from 0).
- This counter will increment once for every clock cycle and takes two clock cycles to overflow, so every cycle it will alternate between a transition from 0 to 1 and a transition from 1 to 0

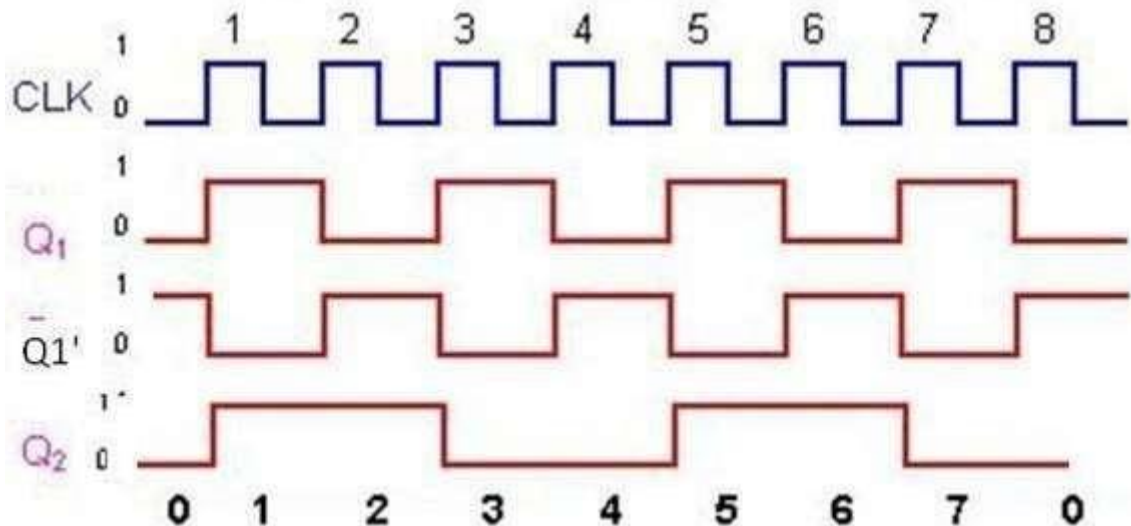
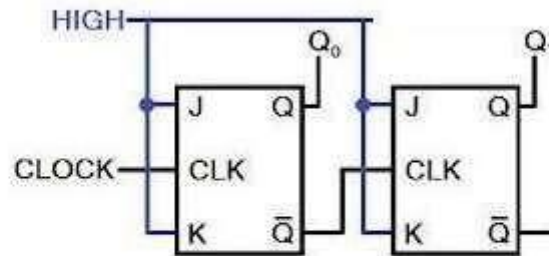
ASYNCHRONOUS COUNTERS

Two-bit ripple up-counter using negative edge triggered flip flop:



Asynchronous counters –Decade counter

Two-bit ripple down-counter using negative edge triggered flip flop:



ASYNCHRONOUS COUNTERS

- A decade counter is one of which goes through 10 unique combinations of output and then reset as the clock proceeds.
- We may use some sort of feedback in 4 bit binary counter to skip any six of the sixteen possible output state from 0000 to 1111 to get decade counter.
- A decade counter does not necessarily count from 0000 to 1001, it could count as 0000,0001,0010,1000,1010,1011,1110,0000,0001, and so on....

ASYNCHRONUS COUNTERS

After pulses	Count			
	Q4	Q3	Q2	Q1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	0	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	0	1	0	1
10	0	0	0	0

SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS



Shift registers:

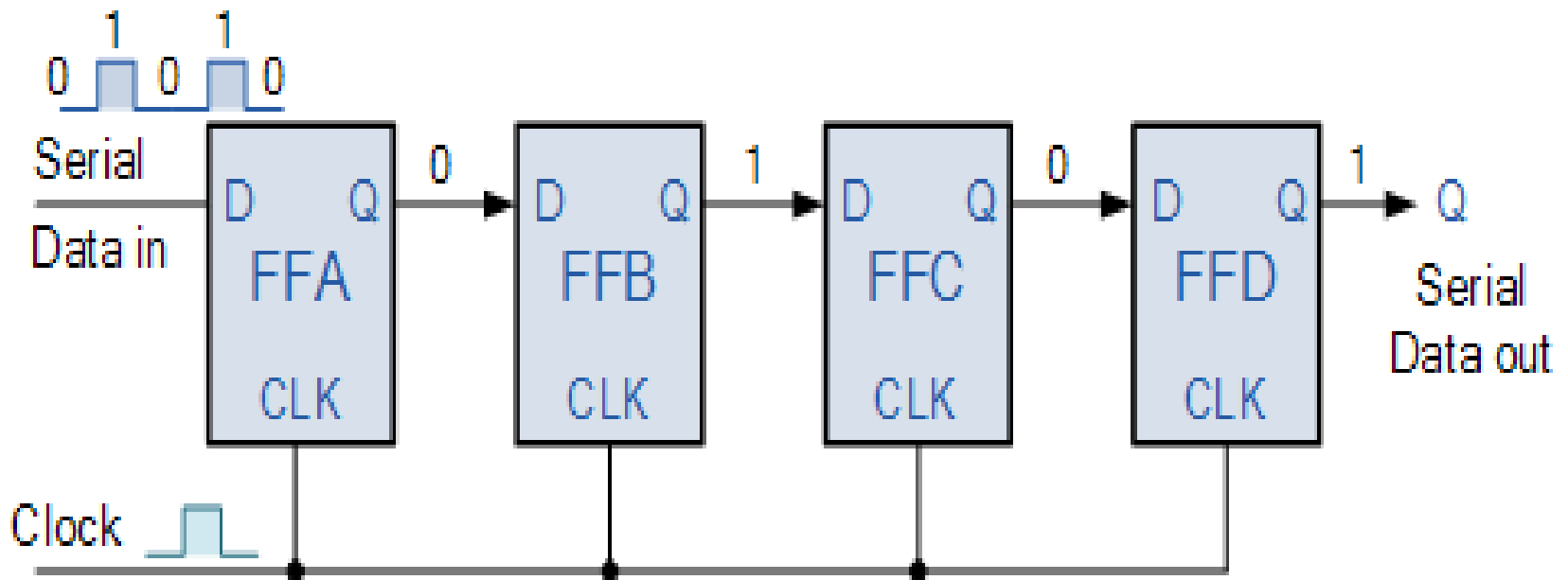
In digital circuits, a **shift register** is a cascade of flip-flops sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input

Types of shift registers.

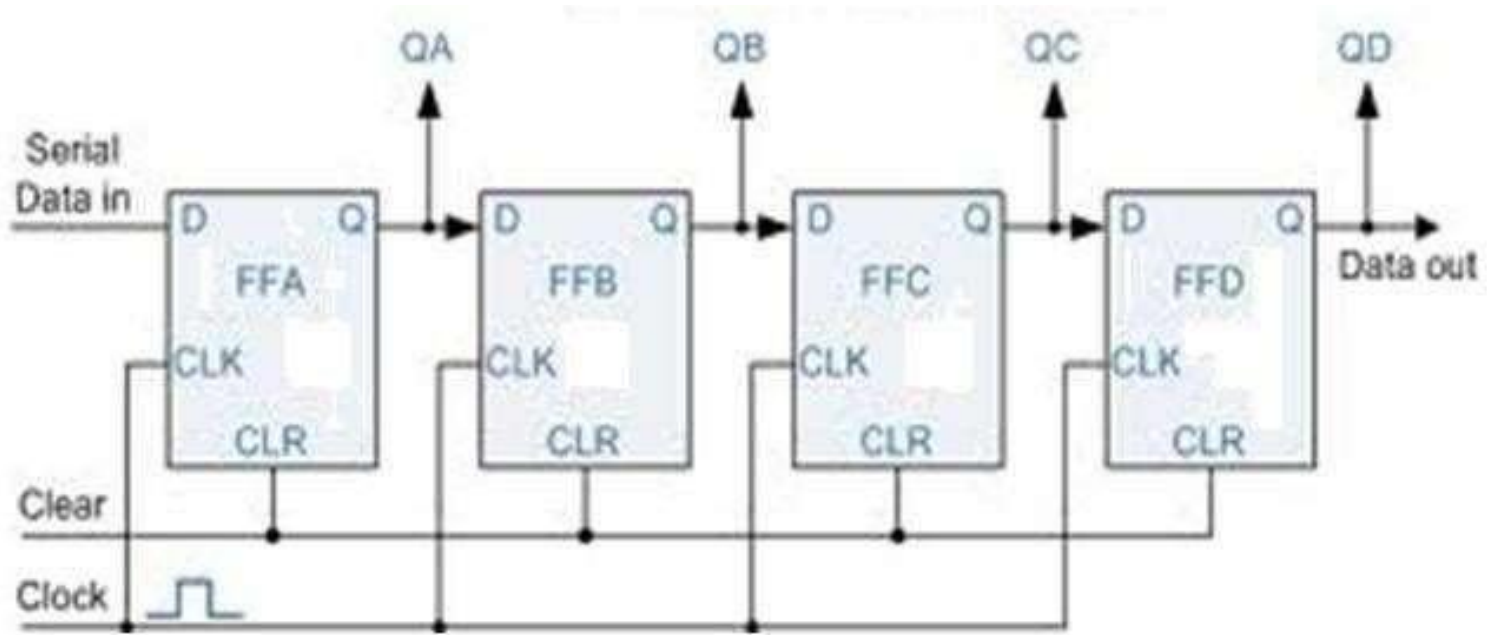
- Serial in, serial out, shift right, shift registers
- Serial in, serial out, shift left, shift registers
- Parallel in, serial out shift registers
- Parallel in, parallel out shift registers

SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS

Serial IN, serial OUT, shift right, shift left register:



Serial-in, parallel-out, shift register:



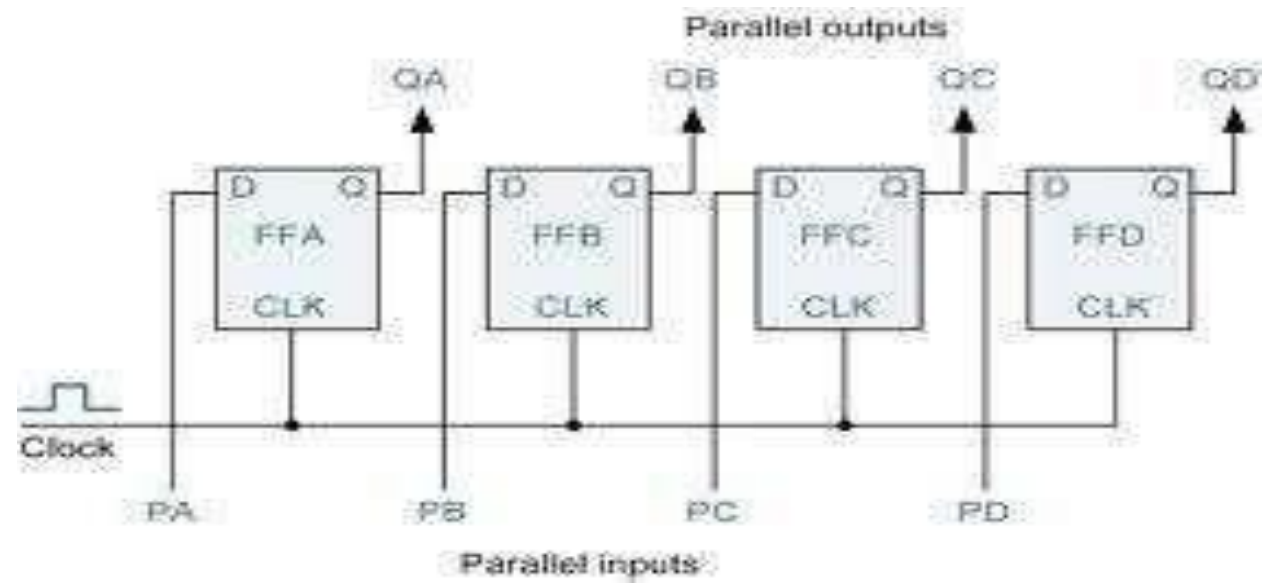
SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS

Applications of shift register:

- Delay line
- parallel to serial converter
- Serial to parallel converter
- Sequence generator
- Shift register counters

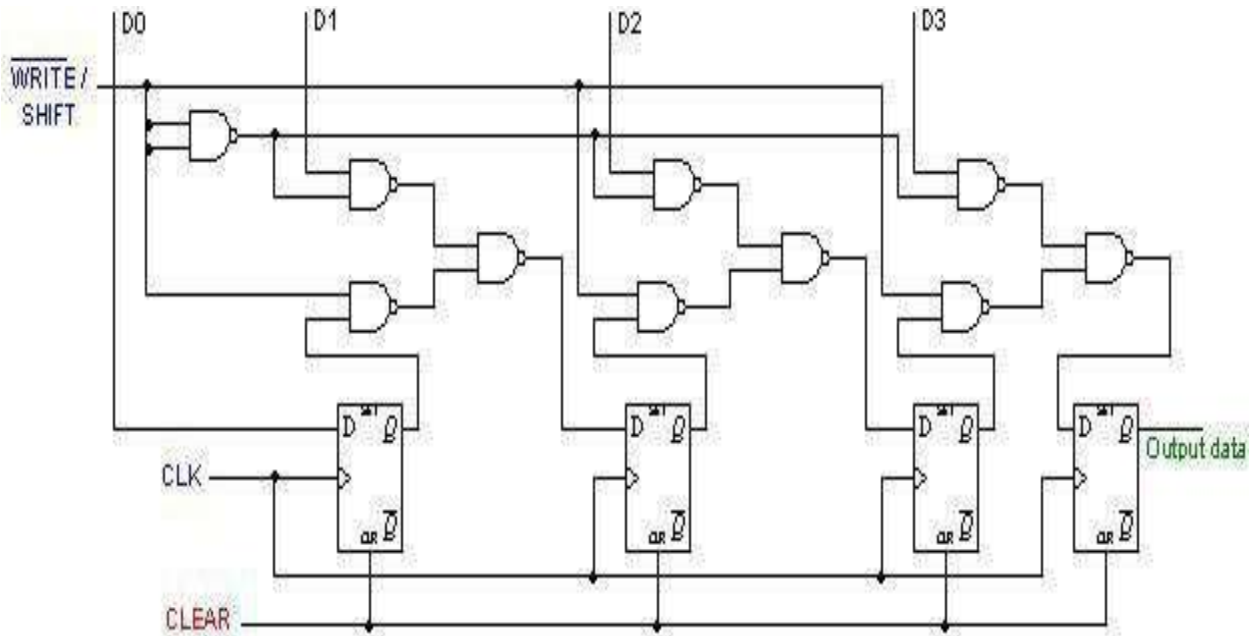
SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS

Parallel-in, parallel-out, shift register



SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS

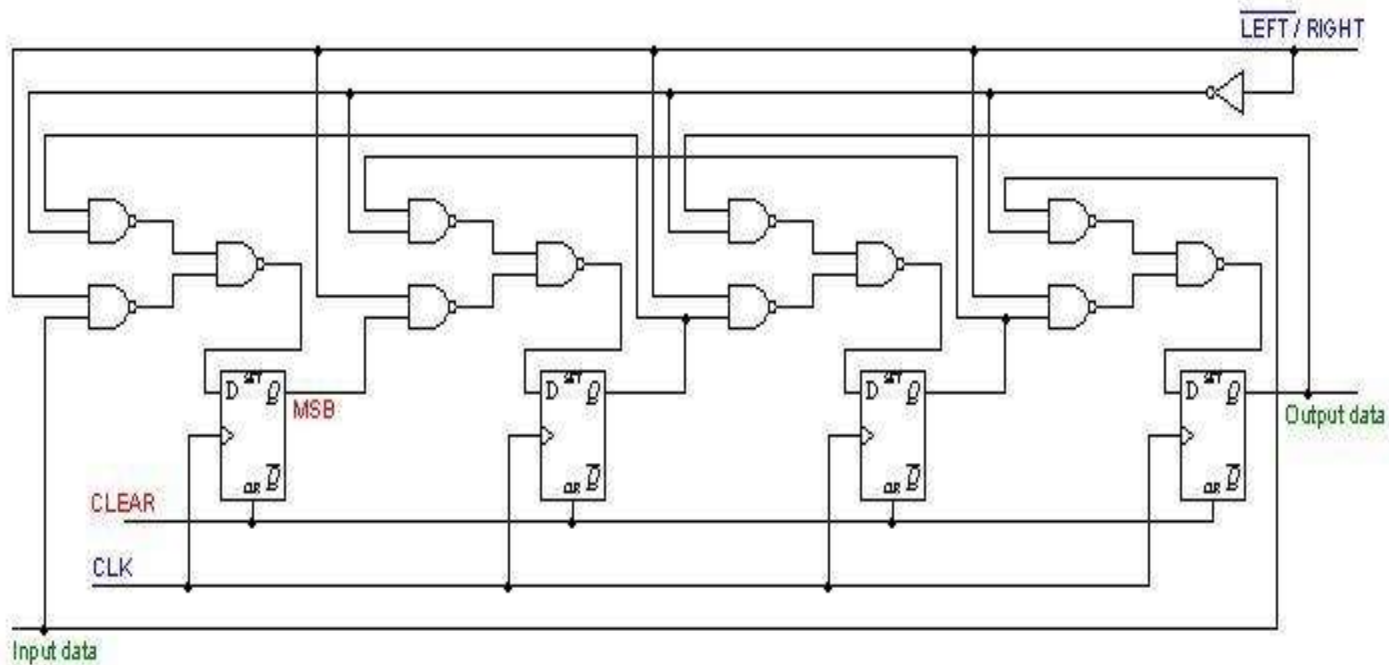
Parallel In - Serial Out Shift Registers



SHIFT REGISTERS AND UNIVERSAL SHIFT REGISTERS

Bidirectional shift register:

bidirectional shift register is one which the data bits can be shifted from left to right or from right to left.



RING COUNTER AND JOHNSON COUNTER

Shift register counters:

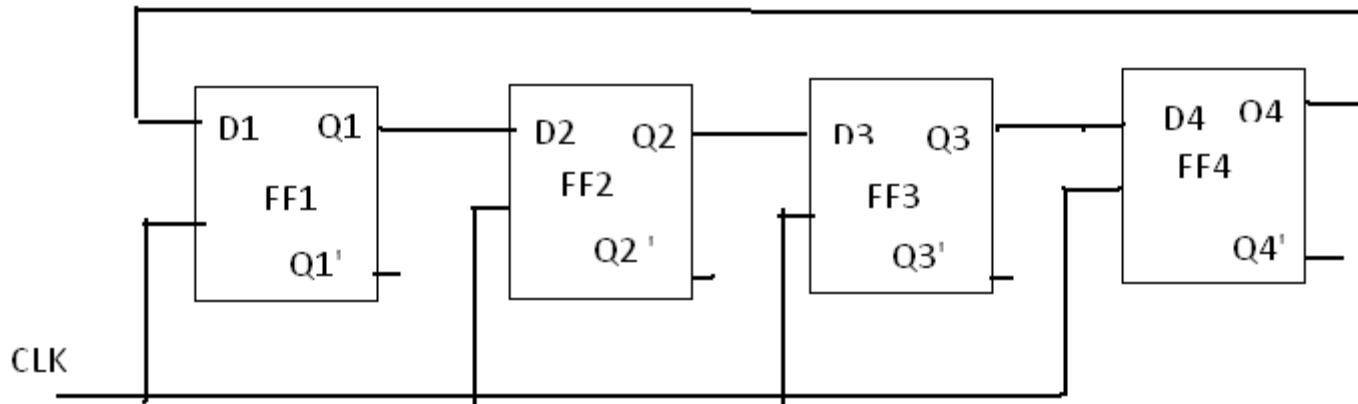
One of the applications of shift register is that they can be arranged to form several types of counters. The most widely used shift register counter is ring counter as well as the twisted ring counter.

Types of shift register counters

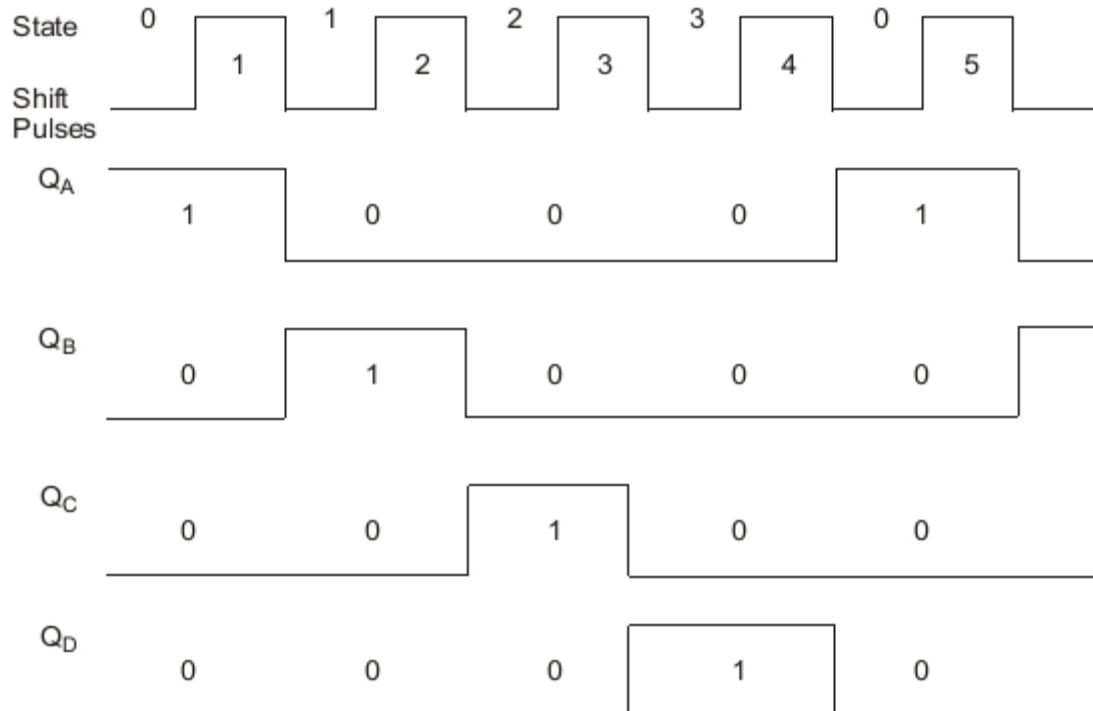
- Ring counter
- Johnson counters

RING COUNTER AND JOHNSON COUNTER

Ring counter

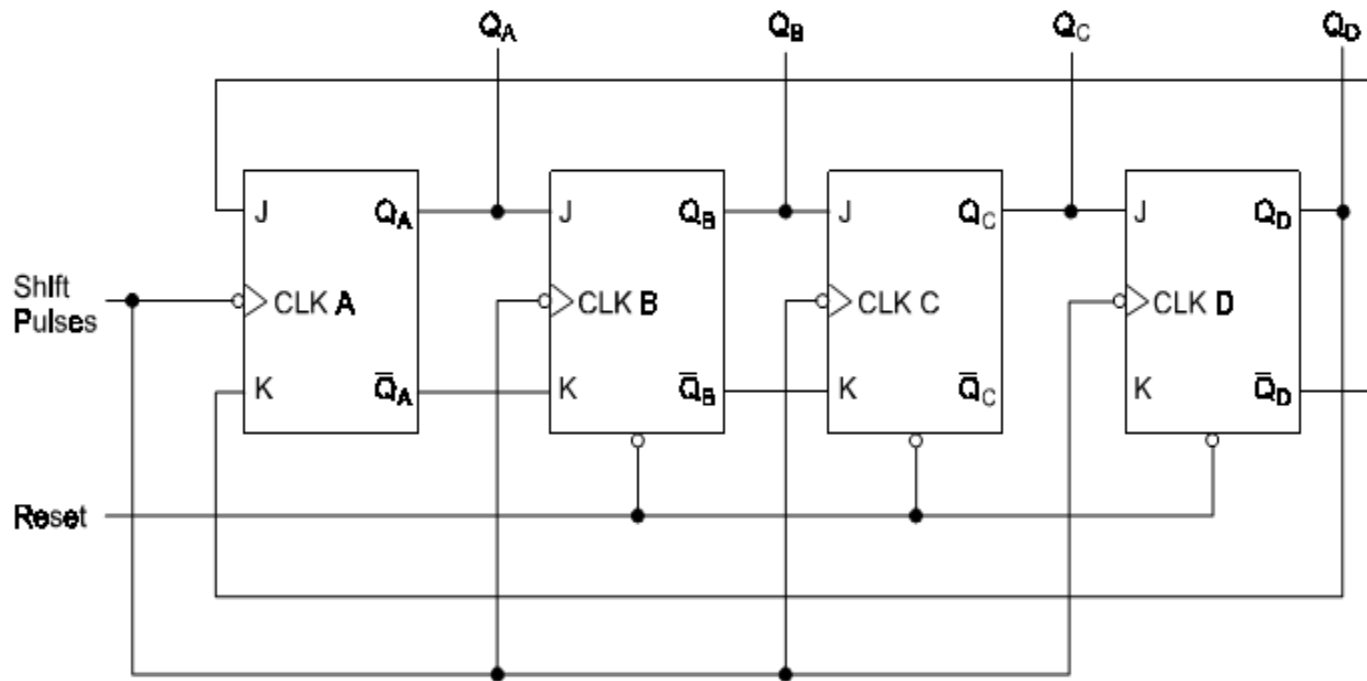


RING COUNTER AND JOHNSON COUNTER

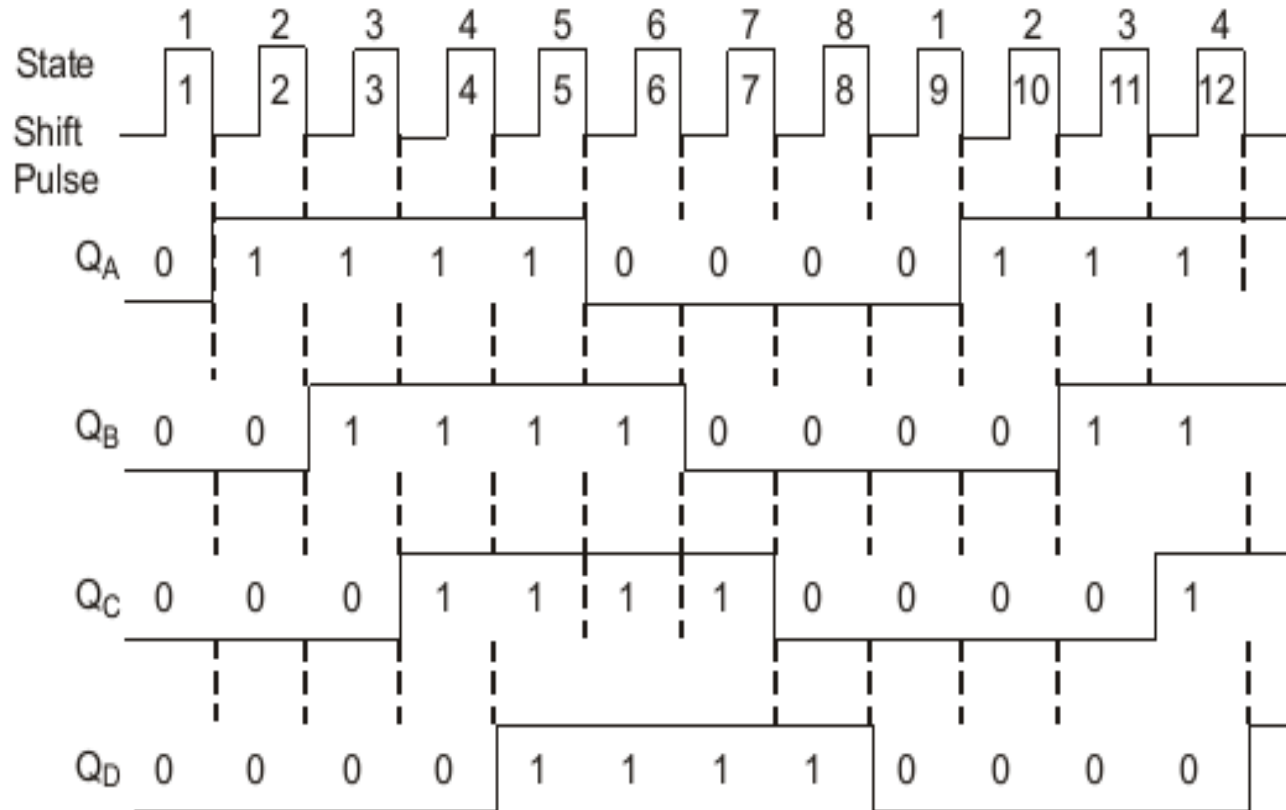


RING COUNTER AND JOHNSON COUNTER

Twisted Ring counter (Johnson counter):



RING COUNTER AND JOHNSON COUNTER





Thank you