INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**VLSI DESIGN**				
Course Code	AEC017				
Programme	B.Tech				
Semester	VII	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Ms. K S Indrani , Assistant Professor, ECE				
Course Faculty	Mr.V.R Seshagiri Rao , Associate Professor Dr. V Vijay, Associate Professor Dr. M Manisha, Associate Professor				

I. COURSE OVERVIEW:

The course focuses on basics VLSI design. The foundation in this course started with the fundamentals of MOSFET, Scaling issues, Short Channel Effects, and then gradually focuses on technology nodes and sub-threshold region of operation. Further, this course describes the fabrication process of MOS devices. A detailed overview is given about layout and its design rules of MOS devices. Layout of basic gates is implemented in this course. It further gives information on data path subsystem and array subsystems, several PLD's performance parameters of the circuits. This course provides the reliability issues of MOS devices. Basically this course drives the student interest towards circuit designing for various applications.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Digital System Design	4
UG	AEC008	V	Integrated Circuits Applications	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
VLSI Design	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✔	Quiz	✔	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
50 %	To test the analytical skill of the concept OR to test the application skill of the concept.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Quiz / Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Quiz / AAT**	
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8^{th} and 16^{th} week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting of two parts. Part–A shall have five compulsory questions of one mark each. In part–B, four out of five questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Quiz / Alternative Assessment Tool (AAT):

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are be answered by choosing the correct answer from a given set of choices (commonly four). Marks shall be awarded considering the average of two quizzes for every course. The AAT may include seminars,

assignments, term paper, open ended experiments, five minutes video and MOOCs.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Presentation on real-world problems
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Seminar
PO 3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Presentation on real-world problems
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Seminar
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Laboratory
PO11	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life long learning in the broadest context of technological change.	3	Creative innovative ideas

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Lectures and Assignments

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	3	-
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths, to be an entrepreneur, and a best for higher studies.	3	Guest lectures

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES:

The course should enable the students to:	
I	Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II	Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III	Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout.
IV	Focus in selecting appropriate building blocks of data path for given system.

IX. COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Explore the basic operations of MOSFET, parameters to be considered which effects the operation of MOS, effect of scaling on MOS devices, how to overcome draw back.	CLO 1	Understand fundamentals of MOS devices and its V-I characteristics.
		CLO 2	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
		CLO 3	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
		CLO 4	Understand the basic CMOS nano technology and the importance of it.
CO 2	Understand various VLSI design styles, fabrication process of MOS, able to analyze the inverter characteristics, understand the delay, noise margin and power dissipation of MOS transistor.	CLO 5	Understand the fabrications steps involved in the MOS transistor.
		CLO 6	Study various inverter characteristics of NMOS, CMOS.
		CLO 7	Understand the effect of delay, noise margin and power dissipation of MOS devices.
		CLO 8	Understand implementation of logic designs using MOS transistors series & parallel circuits.
		CLO 9	Study other logic families like pass transistor logic, Bi-CMOS logic and various pull-up networks.
CO 3	Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up.	CLO 10	Understand to implement layers using stick diagram along with the color representation.

COs	Course Outcome	CLOs	Course Learning Outcome
CO 3	Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up.	CLO 11	Study the design rules of transistors, wires , contacts and layouts with respect to width, length and spacing based on type of technology.
		CLO 12	Understand effects on VLSI Interconnects and electron migration.
		CLO 13	Study the latch up problems and reliability issues of CMOS.
CO 4	Understand various gate level designs, analyze various performance parameters like area, speed and capacitance and study the Fan-In and Fan-out.	CLO 14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.
		CLO 15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
		CLO 16	Understand the implementation strategies of VLSI design.
		CLO 17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
		CLO 18	Understand data path subsystem designs, array subsystem designs
CO 5	Understand design options for common datapath operators, various memories, low power memories. Analyze various timing issues, clocking strategies of VLSI designs and study various digital designs.	CLO 19	Understand the operation of various static and dynamic latches and registers.
		CLO 20	Analyze the timing issues and the clock strategies of VLSI designs.
		CLO 21	Understand the purpose and operation of Low power memory Circuits.
		CLO 22	Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

X. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
AEC017.01	CLO 1	Understand fundamentals of MOS devices and its V-I characteristics.	PO 1, PO 2	3
AEC017.02	CLO 2	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.	PO 1, PO 2	3
AEC017.03	CLO 3	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.	PO 1, PO 4	3
AEC017.04	CLO 4	Understand the basic CMOS nano technology and the importance of it.	PO4, PO5	3
AEC017.05	CLO 5	Understand the fabrications steps involved in the MOS transistor.	PO 1	2
AEC017.06	CLO 6	Study various inverter characteristics of NMOS, CMOS.	PO 1, PO 2	3
AEC017.07	CLO 7	Understand the effect of delay, noise margin and power dissipation of MOS devices.	PO 1	3

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
AEC017.08	CLO 8	Understand implementation of logic designs using MOS transistors series & parallel circuits.	PO 1, PO 3	3
AEC017.09	CLO 9	Study other logic families like pass transistor logic, Bi-CMOS logic and various pull-up networks.	PO 1	2
AEC017.10	CLO 10	Understand to implement layers using stick diagram along with the color representation.	PO 1, PO 3	3
AEC017.11	CLO 11	Study the design rules of transistors, wires, contacts and layouts with respect to width, length and spacing based on type of technology.	PO 1, PO 3	3
AEC017.12	CLO 12	Understand effects on VLSI Interconnects and electron migration.	PO 3, PO 4	3
AEC017.13	CLO 13	Study the latch up problems and reliability issues of CMOS.	PO 1, PO 2	3
AEC017.14	CLO 14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.	PO 1	3
AEC017.15	CLO 15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.	PO 1, PO 4	3
AEC017.16	CLO 16	Understand the implementation strategies of VLSI design.	PO 1, PO 4	3
AEC017.17	CLO 17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.	PO 1, PO 5 PO 11	3
AEC017.18	CLO 18	Understand data path subsystem designs, array subsystem Designs.	PO 1, PO 11	3
AEC017.19	CLO 19	Understand the operation of various static and dynamic latches and registers.	PO 1, PO 4	3
AEC017.20	CLO 20	Analyze the timing issues and the clock strategies of VLSI designs.	PO 1, PO 4	3
AEC017.21	CLO 21	Understand the purpose and operation of Low power memory Circuits.	PO 1, PO 4 PO 11	3
AEC017.22	CLO 22	Study various Synchronous and asynchronous circuit design; static and dynamic latches and registers.	PO 1, PO 4 PO 11	3

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (POs)								
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 11	PSO 1	PSO 2	PSO 3
CO 1	3	2		2	2		2	1	1
CO 2	3		2				3		
CO 3	3	1	2				3	1	1
CO 4	3			3	3	3	3	2	1

CO 5	3			3			3	3	

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XII. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2											2		
CLO 2	3	2											3		
CLO 3	3			2									3	2	
CLO 4				3	3								3	3	3
CLO 5	3												2		
CLO 6	3	3											3		
CLO 7	3												2		
CLO 8	3		3										2		
CLO 9	2												3		
CLO 10	3		2										3		
CLO 11	3		2										3		
CLO 12			3	3									3		
CLO 13	3	3											2	3	
CLO 14	3			2									3	3	
CLO 15	2			3									3		
CLO 16	3			3									3		3
CLO 17	2				3						3		3	3	3
CLO 18	3	2									3		2	3	
CLO 19	3			3									3	3	
CLO 20	3			3									3	3	
CLO 21	3			3							3		3	3	3
CLO 22	3			3							3		3	2	

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XIII. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 4,PSO 1	SEE Exams	PO 1, PO 2 PO 4,PSO 1	Assignments	-	Seminars	PO 1, PO 2 PO 4,PSO 1
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 1, PO 2 PO 4,PSO 1						

XIV. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XV. SYLLABUS

UNIT-I	MOSFETS
Fundamentals of MOSFETs; Weak & strong inversion conditions; Threshold voltage concept in MOSFETs; Current - voltage characteristics of a MOSFET; MOSFET parasitic; Trends & projections in VLSI design & technology; Scaling in MOS devices; Effects in scaling of MOS devices; BiCMOS technologies; CMOS nanotechnology.	
UNIT-II	**VLSI DESIGN STYLES**
NMOS, PMOS and CMOS fabrication Flow; Noise Margin; Inverter Threshold Voltage; NMOS inverter design and characteristics; CMOS inverter design and properties; Delay and power dissipation; Parallel & series equivalent circuits; Pass transistor; Various pull ups; Bi-CMOS inverters.	
UNIT-III	**VLSI PHYSICAL DESIGN**
Stick Diagrams; Physical design rules: 2 µm and lambda CMOS design rules for wires, contacts and transistors; Layout design; Euler's rule for physical design. VLSI Interconnects; Reliability issues in CMOS VLSI; Latching; Electromigration.	
UNIT-IV	**LOGIC DESIGN AND IMPLEMENTATION STRATEGIES**
Gate Level Design: Complex gates; Switch logic; Transmission gates; Static and dynamic CMOS design; Time delays; Driving large capacitive loads; Wiring capacitances; Fan-in and Fan-out; Choice of layers implementation strategies full custom and semi custom design; Standard cell design and cell libraries; Programmable logic devices; CPLDs; FPGA building block architectures; FPGA interconnect routing procedures; Speed and area tradeoff.	
UNIT-V	**SUB SYSTEM DESIGN**
Data Path Sub Systems: Sub system design; Shifters; Adders; ALUs; Multipliers; Parity generators; Comparators; Zero/one detectors; Counters Array Subsystems: SRAM; DRAM; ROM; Serial access Memories; Static and dynamic latches and registers; Timing issues; Clock strategies; Low power memory Circuits; Synchronous and asynchronous circuit design.	
Text Books:	
1. A. Pucknell, Kamran Eshraghian, "BASIC VLSI Design," Third Edition, Prentice Hall of India, 2007. ISBN: 978-81-203-0986-9 2. R. Jacob Baker, Harry W.LI. David E.Boyee, "CMOS Circuit Design, Layout and Simulation," Wiley-IEEE Press, USA, 2005. ISBN: 978-0-470-88132-3 3. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective," Second Edition, Phi Learning, 2009. ISBN: 9788120322578	

Reference Books:
1. N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Second Edition, Addision Wesley, 1993. ISBN: 978-81-317-1942-8
2. M.J. Smith, "Application Specific Integrated Circuits", Addisson Wesley, First edition, 1997. ISBN-13: 978- 0321602756
3. John P. Uyemura, "CMOS Logic Circuit Design," Springer, USA, 2007. ISBN: 0-7923-8452-0

XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Discuss Fundamentals of MOSFETs	CLO 1	T1-1.1-1.3
2	Illustrate Weak & strong inversion conditions	CLO 2	T1-1.4
3	Analyze Threshold voltage concept in MOSFETs.	CLO 2	T1-2.2
4	Discuss Current - voltage characteristics of a MOSFET, MOSFET parasitic.	CLO 1	R1-2.1-2.2
5	Discuss Trends & projections in VLSI design & technology.	CLO 3	R1-4.7
6-7	Analyze Scaling in MOS devices; Effects in scaling of MOS devices.	CLO 3	R1-4.8
8-9	Describe BiCMOS technologies, CMOS nanotechnology.	CLO 4	T1-2.12
10-11	Discuss NMOS, PMOS and CMOS fabrication Flow.	CLO 5	T1-1.7,1.8
12-13	Analyze Noise Margin; Inverter Threshold Voltage.	CLO 7	R1-2.5.3
14	Discuss NMOS inverter design and characteristics.	CLO 6	T1-2.6
15	Discuss CMOS inverter design and properties.	CLO 6	T1-2.10
16-17	Illustrate Delay and power dissipation of MOS.	CLO 7	R1-4.2,4.4
18-19	Understand Parallel & series equivalent circuits.	CLO 8	T1-3.2
20	Describe Pass transistor, Various pull ups.	CLO 9	T1-2.5,2.9
21	Discuss Bi-CMOS inverters.	CLO 9	T1-2.12.3
22-23	Explain Stick Diagrams; Physical design rules.	CLO 10	T1-3.1, 3.2.
24	2 μm and lambda CMOS design rules for wires.	CLO 11	T1-3.4,3.5
25-26	Explain contacts and transistors; Layout design.	CLO 11	T1-3.3
27	Discuss Euler's rule for physical design	CLO 11	T1-3.1,3.2
28	Discuss VLSI Interconnects.	CLO 12	R1-4.5
29	Explain Reliability issues in CMOS VLSI.	CLO 12	R1-4.7
30-31	Discuss Latching, Electromigration.	CLO 13	T1-2.13, R1-4.7
32	Illustrate Gate Level Design: Complex gates.	CLO 14	T1-6.3
33	Discuss Switch logic; Transmission gates.	CLO 14	T1-6.2

Lecture No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
34-35	Explain Static and dynamic CMOS design.	CLO 14	T1-6.3
36	Illustrate Time delays.	CLO 15	T1-4.6
37	Discuss Fan-in and Fan-out.	CLO 14	T1-4.11
38-39	Discuss Driving large capacitive loads, Wiring capacitances, Choice of layers.	CLO 15	T1-4.10, 4.11
40-41	Discuss implementation strategies full custom and semi custom design.	CLO 16	R1-6.3.7
42	Discuss Standard cell design and cell libraries.	CLO 16	R1-6.3.6
43	Discuss Programmable logic devices; CPLDs.	CLO 17	R1-6.3.2
44-45	Discuss FPGA building block architectures, FPGA interconnect routing procedures.	CLO 17	R1-6.3.4
46	Discuss Speed and area tradeoff of PLD's.	CLO 17	R1-6.6.7
47-48	Explain Data Path Sub Systems: Shifters; Adders.	CLO 18	R1-8.1,8.2
49-50	Explain ALUs; Multipliers.	CLO 18	R1-8.9
51-52	Explain Parity generators; Comparators.	CLO 18	R1-8.4
53-54	Explain Zero/one detectors; Counters.	CLO 18	R1-8.3,8.5
55-56	Explain Array Subsystems: SRAM, DRAM.	CLO 18	R1-9.1,9.2, 9.3
57	Discuss ROM; Serial access Memories.	CLO 18	R1-9.4,9.5
58-59	Discuss Static and dynamic latches and registers.	CLO 19	T3-7.2,7.3
60-61	Illustrate Timing issues , Clock strategies.	CLO 20	T3 -7.7
62	Discuss Low power memory Circuits.	CLO 21	T3
63	Discuss Synchronous and asynchronous circuit design.	CLO 22	T3

XVII. GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs	Relevance With PSOs
1	To understand the concepts of advanced VLSI design.	Seminars	PO1, PO2	PSO1
2	Concepts of nano technology	Seminars / NPTEL	PO1,PO3,PO4	PSO1
3	Encourage students to enter into Core domain.	By training	PO4,PO5	PSO2,PSO3

Prepared by:
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