INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad – 500043

Electronics and Communication Engineering

List of Laboratory Experiments

DIGITAL SYSTEM DESIGN LABORATORY								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
AECC06	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		0	0	2	1	30	70	100
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 36**				**Total Classes:36**		
Branch: ECE	**Semester: III**	**Academic Year: 2021-22**				**Regulation: UG20**		

Course overview:

The laboratory strives in exploring the logic design and related fields. Digital logic testers are used to provide students with practical training and familiarize themselves with the various functions of logic gates and using integrated components to complete circuitry functions and develop an interest in digital logic and enlighten them in the abilities of deduction. The lab allows students to conduct actual gate-level experiments on combinational and sequential circuits to increase student interest and develop skills to design digital gates using VHDL.

Course objectives:

The students will try to learn:

I. Simulation of the combinational logic circuits using HDL code.
II. Model the sequential circuits and simulate using HDL code.
III. Implementation of basic real time applications and verify the outputs using FPGA.

Course outcomes:

After successful completion of the course, students will be able to:

CO1: Apply the concept of Boolean algebra to verify the truth table of various expressions using logic gates in Hardware Description Language.

CO2: Make use of dataflow, structural and behavioral modelling styles of HDL for simulating the combinational logic circuits.

CO3: Analyze the SR flip flop, JK flip flop, D flip flop, T flip flops for functional simulation and timing analysis.

CO4: Build the universal shift registers, counters using the flip flops.

CO5: Examine a finite state machine for detection of sequence.

CO6: Design the real time applications like traffic light controller, chess clock controller FSM, elevator operations using FPGA kit.

WEEK NO	EXPERIMENT NAME	CO
WEEK – I	**REALIZATION OF A BOOLEAN FUNCTION** Design and simulate the HDL code to realize three and three variable Boolean functions	CO1
WEEK – II	**DESIGN OF DECODER AND ENCODER** Design and simulate the HDL code for the following combinational circuits a. 3 to 8 Decoder b. 8 to 3 Encoder (With priority and without priority)	CO2
WEEK – III	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER** Design and simulate the HDL code for the following combinational circuits a. Multiplexer b. De-multiplexer	CO2
WEEK – IV	**DESIGN OF CODE CONVERTERS** Design and simulate the HDL code for the following combinational circuits a. 4 - Bit binary to gray code converter	CO2

	b. 4 - Bit gray to binary code converter c. Comparator	
WEEK – V	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING** Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	**CO2**
WEEK – VI	**DESIGN OF 8-BIT ALU** Design a model to implement 8-bit ALU functionality	**CO2**
WEEK – VII	**HDL MODEL FOR FLIP FLOPS** Write HDL codes for the flip-flops - SR, D, JK, T	**CO3**
WEEK –VIII	**DESIGN OF COUNTERS** Write a HDL code for the following counters a. Binary counter b. BCD counter (Synchronous reset and asynchronous reset)	**CO4**
WEEK - IX	**HDL CODE FOR UNIVERSAL SHIFT REGISTER** Design and simulate the HDL code for universal shift register	**CO4**
WEEK - X	**HDL CODE FOR CARRY LOOK AHEAD ADDER** Design and simulate the HDL code for carry look ahead adder	**CO2**
WEEK - XI	**HDL CODE TO DETECT A SEQUENCE** Write a HDL code to detect the sequence 1010101 and simulate the code	**CO5**
WEEK - XII	**CHESS CLOCK CONTROLLER FSM USING HDL** Design a chess clock controller FSM using HDL and simulate the code	**CO6**
WEEK - XIII	**TRAFFIC LIGHT CONTROLLER USING HDL** Design a traffic light controller using HDL and simulate the code	**CO6**
WEEK - XIV	**ELEVATOR DESIGN USING HDL CODE** Write HDL code to simulate Elevator operations and simulate the code	**CO6**