INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad – 500043

Electronics and Communication Engineering

List of Laboratory Experiments

VLSI DESIGN LABORATORY								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
AECB29	**Core**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		0	0	3	1.5	30	70	100
Contact Classes: Nil	**Tutorial Classes: Nil**	**Practical Classes: 36**				**Total Classes:36**		
Branch: ECE	**Semester: VII**	**Academic Year: 2021-22**				**Regulation: R18**		

Course overview:

The art of VLSI circuit design is dynamic with advances in process technology and innovations in the electronic design automation (EDA) industry. The objective of this laboratory course is to demonstrate the various stages in VLSI design flow using cadence software. Hands on training on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design.

Course objectives:

The students will try to learn:

I. Modern tools for functional level to physical layout with verification at intermediate stages in the VLSI design flow in top-down approach.

II. Design and simulations of analog, digital and mixed circuits for optimum values of area over head, power and time delay.

III. The Chip design through a practical approach using advanced modern tools such as vivado and cadence for front end& back end.

Course outcomes:

After successful completion of the course, students should be able to:

CO1: Calculate the static, dynamic and noise margin parameters of CMOS inverter using the output and transfer characteristics of MOSFETs

CO2: Analyze complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays

CO3:Build 4 X 1 multiplexer and ring oscillator using multiplexer & inverter circuit symbols with necessary inter connections

CO4: Examine the conditions for optimum performance of latches and registers with the knowledge of digital system design.

CO5: Calculate bandwidth, gain, and common mode rejection ratio parameters for differential, MOSFET and casode amplifiers.

CO6:Build the stick diagrams, layouts of MOS circuits using design rule checks (DRC) and verification

WEEK NO	EXPERIMENT NAME	CO
WEEK – I	**MOSFET** To plot the, (i) output characteristics (ii) Transfer characteristics of an n-channel and p-channel MOSFET.	CO1
WEEK – II	**CMOS INVERTER** To design the static (VTC) and dynamic characteristics and layout of a digital CMOS inverter.	CO1
WEEK – III	**RING OSCILLATOR** To design and plot the output characteristics of a 3 stage ring oscillator using CMOS inverters.	CO2
WEEK – IV	**LOGIC GATES**	CO2

	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS design style.	
WEEK – V	**4X1 MULTIPLEXER** To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic and transmission gatelogics	**CO3**
WEEK – VI	**LATCHES** To design and plot the characteristics of a positive and negative latch using multiplexers.	**CO4**
WEEK – VII	**REGISTERS** To design and plot the characteristics of a master-slave positive and negative edge triggered registers based onmultiplexers.	**CO4**
WEEK –VIII	**DIFFERENTIAL AMPLIFIER** Design and simulation of a simple 5 transistor differential amplifier. Measure gain and Common mode rejection ratio.	**CO5**
WEEK - IX	**MOSFET COMMON SOURCE AMPLIFIER** Analysis of Frequency response of Common source amplifiers using n and p MOSFETs	**CO5**
WEEK - X	**MOSFET COMMON DRAIN AMPLIFIER** Analysis of Frequency response of Common drain amplifiers using n and p MOSFETs	**CO5**
WEEK - XI	**SINGLE STAGE CASCODE AMPLIFIER** Design and Simulation of Single Stage Cascode Amplifier.	**CO5**
WEEK - XII	**BASIC CURRENT MIRROR, CASCODE CURRENT MIRROR AMPLIFIER** Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier.	**CO6**
WEEK - XIII	**DESIGN OF NAND/NOR USING CNTFET** Design and plot the dynamic characteristics of 2-input NAND/ NOR logic gates using CNTFET.	**CO6**
WEEK - XIV	**DESIGN OF DIFFERENTIAL AMPLIFIER USING FINFET** Analysis of Frequency response of differential amplifiers using FinFET.	**CO6**