INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE DESCRIPTOR

Course Title	Analog and Digital Electronics Laboratory				
Course Code	AECB04				
Programme	B.Tech				
Semester	III	EEE			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	-	-	-	3	1.5
Chief Coordinator	Mr. P.Sandeep Kumar, Assistant Professor				
Course Faculty	Ms.M.Sreevani, Assistant Professor Ms. V. Bindusree, Assistant Professor Ms. K.C Koteswaramma, Assistant Professor Ms. P. Annapurna, Assistant Professor				

I. COURSE OVERVIEW:

This course introduces the laboratory practise of basics concepts of analog and digital electronics. The course teaches characteristics and applications of diodes,transistors with analysis of experimented results. The course also includes various combinational and sequential circuits with verification of their truth tables.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEEB07	II	Electrical Circuits Laboratory	1.5

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Analog and Digital Electronics Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✘	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	Laboratory		Total Marks
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):
One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	Performance	Calculations and Graph	Results and Error Analysis	Viva	Total
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program Outcomes (POs)	Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Calculations of the observations
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Exercise, Discussion
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Term observations
PO 6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	-	Exercise, Discussion

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

	Program Specific Outcomes (PSOs)	Strength	Proficiency assessed by
PSO 1	**Problem Solving Skills:** Able to utilize the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work.	2	Lab related Exercises
PSO 2	**Professional Skills:** To explore the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering, and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally.	-	-

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 3	**Modern Tools in Electrical Engineering:** To be able to utilize of technologies like PLC, PMC, process controllers, transducers and HMI and design, install, test, and maintain power systems and industrial applications.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Implement and study the characteristics of diodes and transistors.
II	Illustrate the concept of rectification using half wave and full wave rectifiers.
III	Design and construct different amplifier circuits.
IV	Build the concept of digital and binary system.
V	Design and analyze the combinational logic circuits.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB04.01	CLO 1	Understand the pn junction diode characteristics.	PO 1	3
AECB04.02	CLO 2	Understand the zener diode characteristics and voltage regulator.	PO 1	3
AECB04.03	CLO 3	Understand half wave and full wave rectifier with and without filter.	PO 1	3
AECB04.04	CLO 4	Analyze input and output CE characteristics	PO 2	2
AECB04.05	CLO 5	Analyze input and output CE characteristics	PO 2	2
AECB04.06	CLO 6	Understand the frequency response of CE amplifier.	PO 2	2
AECB04.07	CLO 7	Understand Boolean expressions using gates	PO 1	3
AECB04.08	CLO 8	Understand universal gates	PO 2	2
AECB04.09	CLO 9	Understand nand / nor gates	PO 2	2
AECB04.10	CLO 10	Understand adder/ subtractor	PO 2	2
AECB04.11	CLO 11	Understand binary to gray conversion	PO 2	2
AECB04.12	CLO 12	Verify truth tables and excitation tables	PO 1	3
AECB04.13	CLO 13	Realize shift register	PO 1	3
AECB04.14	CLO 14	Realize 8x1 multiplexer	PO 1	3

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB04.15	CLO 15	Realize 2 bit comparator	PO 1	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3				2								1		
CLO 2	2	3											1		
CLO 3	3				3								1		
CLO 4	2				2								2		
CLO 5					2								3		
CLO 6	2	2											1		
CLO 7		2			2								2		
CLO 8					2								1		
CLO 9		3			2								2		
CLO 10		2											1		
CLO 11					1								2		
CLO 12	3												2		
CLO 13	3												2		
CLO 14	3												2		
CLO 15	3												2		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 5	SEE Exams	PO 1, PO 2 PO 5	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2 PO 5	Student Viva	PO 1, PO 2 PO 5	Mini Project	-	Certification	-
Term Paper	-						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

LIST OF EXPERIMENTS	
Week-1	**PN JUNCTION DIODE CHARACTERISTICS**
Verification of V-I characteristics of PN diode and calculate static and dynamic resistance using Hardware.	
Week-2	**ZENER DIODE CHARACTERISTICS AND VOLTAGE REGULATOR**
Verification of V-I characteristics of Zener diode and perform Zener diode as a Voltage regulator using Hardware.	
Week-3	**HALF WAVE AND FULL WAVE RECTIFIER**
Verification of Half wave rectifier and Full wave rectifier without and with filters using hardware.	
Week-4	**TRANSISTOR CE CHARACTERISTICS**
Verification of Input and Output characteristics of CE configuration using hardware	
Week-5	**TRANSISTOR CB CHARACTERISTICS**
Verification of Input and Output characteristics of CB configuration using hardware	
Week-6	**FREQUENCY RESPONSE OF CE AMPLIFIER**
Determine the Gain and Bandwidth of CE amplifier using hardware.	
Week-7	**BOOLEAN EXPRESSIONS USING GATES**
Realization of Boolean Expressions using Gates	
Week-8	**UNIVERSAL GATES**
Design and realization of logic gates using universal gates	
Week-9	**NAND / NOR GATES**
Generation of clock using NAND / NOR gates	
Week-10	**ADDER/ SUBTRACTOR**
Design a 4 – bit Adder / Subtractor	
Week-11	**BINARY TO GRAY CONVERTER**
Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter	
Week-12	**TRUTH TABLES AND EXCITATION TABLES**
Verification of truth tables and excitation tables	
Week- 13	**SHIFT REGISTER**
Design and realization of an 8 bit parallel load and serial out shift register using flip-flops	
Week- 14	MULTIPLEXER

Design and realization of 8x1 using 2x1 MUX	
Week- 15	**2 BIT COMPARATOR**
Design and realization of 2 bit comparator	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No.	Topics to be covered	Course Learning Outcomes	References
1	Understand the pn junction diode characteristics.	CLO 1	R1:3.1
2	Understand the zener diode characteristics and voltage regulator.	CLO 2	R1:3.4
3	Understand half wave and full wave rectifier with and without filter.	CLO 3	R1:3.2
4	Analyze input and output CE characteristics	CLO 4	R1:4.2
5	Analyze input and output CB characteristics	CLO 5	R1:4.3
6	Understand the frequency response of CE amplifier.	CLO 6	R1:5.3
7	Understand Boolean expressions using gates	CLO 7	W4:1
8	Understand universal gates	CLO 8	W4:2
9	Understand nand / nor gates	CLO 9	W4:3
10	Understand adder/ subtractor	CLO 10	W4:4
11	Understand binary to gray conversion	CLO 11	W4:5
12	Verify truth tables and excitation tables	CLO 12	W4:6
13	Realize shift register	CLO 13	W4:7
14	Realize 8x1 multiplexer	CLO 14	W4:8
15	Realize 2 bit comparator	CLO 15	W4:9

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S NO	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Analysis of JFET amplifiers.	Seminars / NPTEL	PO 1, PO 2	PSO 1
2	Voltage regulators	Seminars / NPTEL	PO 1, PO 2	PSO 2

Prepared by:
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HOD, ECE