INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL SYSTEM DESIGN LABORATORY**				
Course Code	AECB10				
Programme	B.Tech				
Semester	III	ECE			
Course Type	Core				
Regulation	IARE - R18				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	-	-	-	3	1
Chief Coordinator	Mr. N Nagaraju, Assistant Professor				
Course Faculty	Dr. V Viajy, Professor Mrs. J Sravana, Assistant Professor Mrs. V Bindusree, Assistant Professor				

I. COURSE OVERVIEW:

This course gives knowledge about the design, analysis, simulation of circuits used as building blocks in Very Large Scale Integration (VLSI) devices. Students can apply the concepts learnt in the lectures towards design of actual VLSI subsystem all the way from specification, modeling, synthesis and physical design. This lab provides hands-on experience on implementation of digital circuit designs using HDL language, which are required for development of various projects and research work.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AECB07	III	Digital System Design	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital Systems Design Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✘	Seminars	✘	Mini Project	✔	Videos
✔	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):
One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	Performance	Calculations and Graph	Results and Error Analysis	Viva	Total
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Observations of the Timing diagrams
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Lab related Exercises
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Design Exercises

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems**.**	2	Lab related Exercises
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	-	-
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-	-	-

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
	wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.		

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Design of combinational circuits using Verilog Hardware Description Language.
II	Implementation of Sequential circuits using Verilog Hardware Description Language.
III	Demonstration of different case studies for Verilog HDL implementation.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AECB10.01	CLO 1	Understand the concept of Boolean functions using VHDL	PO 1, PO 2	3
AECB10.02	CLO 2	Understand the encoder and decoder using VHDL	PO 1, PO 2, PO 5	3
AECB10.03	CLO 3	Design of multiplexer and demultiplexer using VHDL	PO 1, PO 2	3
AECB10.04	CLO 4	Design of code converters using VHDL	PO 1, PO 2, PO 5	2
AECB10.05	CLO 5	Implement full adder and full subtractor using VHDL	PO 1, PO 2	2
AECB10.06	CLO 6	Construct the 8-bit ALU using VHDL	PO 1, PO 2, PO 5	2
AECB10.07	CLO 7	Implement the flip flops using VHDL	PO 1, PO 2	2
AECB10.08	CLO 8	Design of counters using VHDL	PO 1, PO 5	3
AECB10.09	CLO 9	Construct universal shift register using VHDL	PO 1, PO 5	3
AECB10.10	CLO 10	Design carry look ahead adder using VHDL	PO 1, PO 5	2
AECB10.11	CLO 11	Construct a VHDL code detect a sequence	PO 1, PO 2, PO 5	2
AECB10.12	CLO 12	Design Chess clock controller FSM using HDL	PO 1, PO 2, PO 5	2
AECB10.13	CLO 13	Design Traffic light controller using HDL	PO 1	3
AECB10.14	CLO 14	Construct Elevator design using HDL code	PO1, PO 2, PO 5	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2											2		
CLO 2	3	2			2								2		
CLO 3	3	2											2		
CLO 4	2	2			2								2		
CLO 5	2	2											2		
CLO 6	2	2			2								2		
CLO 7	2	2													
CLO 8	3				2								2		
CLO 9	3				2								2		
CLO 10	2				2										
CLO 11	2	2			2								2		
CLO 12	2	2			2								2		
CLO 13	3														
CLO 14	3	2			2										

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 5, PSO 1	SEE Exams	PO 1, PO 2 PO 5, PSO 1	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2 PO 5, PSO 1	Student Viva	PO 1, PO 2 PO 5, PSO 1	Mini Project	-	Certification	-

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

LIST OF EXPERIMENTS	
WEEK - l	**REALIZATION OF A BOOLEAN FUNCTION**
Design and simulate the HDL code to realize three and three variable Boolean functions	
WEEK-2	**DESIGN OF DECODER AND ENCODER**
Design and simulate the HDL code for the following combinational circuits a. 3 to 8 Decoder b. 8 to 3 Encoder (With priority and without priority)	
WEEK-3	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER**
Design and simulate the HDL code for the following combinational circuits a. Multiplexer b. De-multiplexer	
WEEK -4	**DESIGN OF CODE CONVERTERS**
Design and simulate the HDL code for the following combinational circuits a. 4 - Bit binary to gray code converter b. 4 - Bit gray to binary code converter c. Comparator	
WEEK -5	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING**
Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	
WEEK -6	**DESIGN OF 8-BIT ALU**
Design a model to implement 8-bit ALU functionality	
WEEK -7	**HDL MODEL FOR FLIP FLOPS**
Write HDL codes for the flip-flops - SR, D, JK, T	
WEEK -8	**DESIGN OF COUNTERS**
Write a HDL code for the following counters a. Binary counter b. BCD counter (Synchronous reset and asynchronous reset)	
WEEK-9	**HDL CODE FOR UNIVERSAL SHIFT REGISTER**
Design and simulate the HDL code for universal shift register	
WEEK-l0	**HDL CODE FOR CARRY LOOK AHEAD ADDER**
Design and simulate the HDL code for carry look ahead adder	
WEEK-l1	**HDL CODE TO DETECT A SEQUENCE**
Write a HDL code to detect the sequence 1010101 and simulate the code	

WEEK-l2	CHESS CLOCK CONTROLLER FSM USING HDL
Design a chess clock controller FSM using HDL and simulate the code	
WEEK-l3	**TRAFFIC LIGHT CONTROLLER USING HDL**
Design a traffic light controller using HDL and simulate the code	
WEEK-l4	**ELEVATOR DESIGN USING HDL CODE**
Write HDL code to simulate Elevator operations and simulate the code	

Text Books:

1. J Bhaskar , "VHDL Primer", 3rd edition.

Reference Books:

1 Samir Palnitkar , "Verilog HDL: "A Guide to Digital Design and Synthesis", Sun Microsystems Press, 2nd Edition, 2003.

2 T.R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", New Jersey, Wiley- IEEE Press, 2009. ISBN: 978-0-471-44148-9

3 Zainalabedin Navabi, "Verilog Digital System Design", TMH, 2nd Edition, 2008.

4 Peter Minns, Ian Elliott, " FSM-based Digital Design using Verilog HDL", John Wiley & Sons Ltd, 2008.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Understand the concept of Boolean functions using VHDL	CLO 1	T1
2	Understand the encoder and decoder using VHDL	CLO 2	T1
3	Design of multiplexer and demultiplexer using VHDL	CLO 3	T1
4	Design of code converters using VHDL	CLO 4	T1
5	Implement full adder and full subtractor using VHDL	CLO 5	T1
6	Construct the 8-bit ALU using VHDL	CLO 6	T1
7	Implement the flip flops using VHDL	CLO 7	T1
8	Design of counters using VHDL	CLO 8	T1
9	Construct universal shift register using VHDL	CLO 9	T1
10	Design carry look ahead adder using VHDL	CLO 10	T1

Week No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
11	Construct a VHDL code detect a sequence	CLO 11	T1
12	Design Chess clock controller FSM using HDL	CLO 12	T1
13	Design Traffic light controller using HDL	CLO 13	T1
14	Construct Elevator design using HDL code	CLO 14	T1

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	To improve standards and analyze the concepts.	NPTEL	PO 1, PO 2	PSO 1
2	Implement parallel and serial adders.	Seminars / NPTEL	PO 1, PO5	PSO 1
3	Encourage students to solve real time applications and prepare towards competitive examinations.	NPTEL	PO 1, PO2, PO5	PSO 1

Prepared by:
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