DIGITAL SYSTEM DESIGN LABORATORY

IV Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC103	Core	-	2	3	2	30	70	100
Contact Classes: Nil	Tutorial Classes: 24	Practical Classes: 45				Total Classes: 69		

OBJECTIVES:

The course should enable the students to:

I. Design of combinational circuits using Verilog Hardware Description Language.
II. Implementation of Sequential circuits using Verilog Hardware Description Language.
III. Demonstration of different case studies for Verilog HDL implementation.

COURSE LEARNING OUTCOMES (CLOs):

The students should enable to:

1. Knowledge and use of hardware description language (VHDL) for system modeling and simulation.
2. Describe and explain the operation of fundamental digital gates.
3. Minimize the Boolean expression using Boolean algebra and design it using logic gates.
4. Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder.
5. Analyze the operation of medium complexity standard combinational circuits like the multiplexer, demultiplexers.
6. Analyze the operation of medium complexity standard combinational circuits like the code converters.
7. Design complex digital systems at several level of abstractions; behavioral and structural, synthesis and rapid system prototyping.
8. Design complex digital system such as ALU.
9. Analyze the operation of a flip-flop and examine relevant timing diagrams.
10. Analyze the operation of counters and shift registers.
11. Develop and simulate register-level models of hierarchical digital systems.
12. Design and model complex digital system.
13. Consolidation of the design methodologies for combinational and sequential digital systems.
14. Implementation of digital systems on reconfigurable programmable logic devices (FPGA).
15. Analyze and synthesize digital modules and circuits for a wide application range.

LIST OF EXPERIMENTS

WEEK - I	**REALIZATION OF A BOOLEAN FUNCTION**

Design and simulate the HDL code to realize three and three variable Boolean functions

WEEK-2	**DESIGN OF DECODER AND ENCODER**

Design and simulate the HDL code for the following combinational circuits

a. 3 to 8 Decoder
b. 8 to 3 Encoder (With priority and without priority)

WEEK-3	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER**
Design and simulate the HDL code for the following combinational circuits a. Multiplexer b. De-multiplexer	
WEEK -4	**DESIGN OF CODE CONVERTERS**
Design and simulate the HDL code for the following combinational circuits a. 4 - Bit binary to gray code converter b. 4 - Bit gray to binary code converter c. Comparator	
WEEK -5	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING**
Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	
WEEK -6	**DESIGN OF 8-BIT ALU**
Design a model to implement 8-bit ALU functionality	
WEEK -7	**HDL MODEL FOR FLIP FLOPS**
Write HDL codes for the flip-flops - SR, D, JK, T	
WEEK -8	**DESIGN OF COUNTERS**
Write a HDL code for the following counters a. Binary counter b. BCD counter (Synchronous reset and asynchronous reset)	
WEEK-9	**HDL CODE FOR UNIVERSAL SHIFT REGISTER**
Design and simulate the HDL code for universal shift register	
WEEK-l0	**HDL CODE FOR CARRY LOOK AHEAD ADDER**
Design and simulate the HDL code for carry look ahead adder	
WEEK-l1	**HDL CODE TO DETECT A SEQUENCE**
Write a HDL code to detect the sequence 1010101 and simulate the code	
WEEK-l2	**CHESS CLOCK CONTROLLER FSM USING HDL**
Design a chess clock controller FSM using HDL and simulate the code	
WEEK-l3	**TRAFFIC LIGHT CONTROLLER USING HDL**
Design a traffic light controller using HDL and simulate the code	

WEEK-l4	ELEVATOR DESIGN USING HDL CODE

Write HDL code to simulate Elevator operations and simulate the code

Text Books:

1. Stephen Brown, Zvonko Vranesic, Fundamentals of Digital Logic Design with VHDL, TMH, 2nd Edition, 2009.
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Sun Microsystems Press, 2nd Edition, 2003.

Reference Books:

1. T.R. Padmanabhan, B. Bala Tripura Sundari, Design Through Verilog HDL, New Jersey, Wiley-IEEE Press, 2009.
2. Zainalabedin Navabi, Verilog Digital System Design, TMH, 2nd Edition, 2008.

Web References:

1. https://inst.eecs.berkeley.edu/~cs150/fa06/Labs/verilog-ieee.pdf
2. http://www.asic-world.com/ www.sxecw.edu.in

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 24 STUDENTS:

HARDWARE: Desktop Computer Systems 24 nos

SOFTWARE: Xilinx Vivado 2018.1