INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**VLSI DESIGN LABORATORY**				
Course Code	AEC117				
Programme	B.Tech				
Semester	VII	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Ms. K S Indrani, Assistant Professor				
Course Faculty	Dr. V Vijay, Associate Professor Ms. S Swathi, Assistant Professor				

I. COURSE OVERVIEW:

This laboratory course builds on the lecture course "VLSI Design" which is mandatory for all students of Electronics and Communication Engineering. The course aims at practical experience by analyzing different digital and analog circuits using Cadence tools. This course also provides measurement of different performance parameters of the circuits.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC013	IV	Digital system Design	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
VLSI Design Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✘	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	**Performance**	**Calculations and Graph**	**Results and Error Analysis**	**Viva**	**Total**
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Lab related Exercises
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Lab related Exercises
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Lab related Exercises

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Lab related Exercises
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	-	-
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Understand the basic concepts about MOS device and inverter characteristics.
II	Understand the fabrication steps of IC design and design flow of VLSI circuits.
III	Design the stick diagram and layout of a circuit.
IV	Design the different MOSFET amplifier circuits.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC117.01	CLO 1	To understand output characteristics of an n-channel and p-channel MOSFET	PO 1 PO 5	3
AEC117.02	CLO 2	To understand how plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.	PO 1 PO 2	3
AEC117.03	CLO 3	To understand how plot the output characteristics of a 3-inverter ring oscillator	PO 1 PO 5	3
AEC117.04	CLO 4	To understand how plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	PO 1 PO 2	2
AEC117.05	CLO 5	To understand how plot the characteristics of a 4x1 digital multiplexer using pass transistor logic	PO 5	2
AEC117.06	CLO 6	To understand how plot the characteristics of a positive and negative latch based on multiplexers.	PO 1 PO 2	2
AEC117.07	CLO 7	To understand how plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.	PO 2 PO 5	2
AEC117.08	CLO 8	To understand how Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR.	PO 5	2
AEC117.09	CLO 9	To design layout of NMOS and CMOS inverter.	PO 5	2
AEC117.10	CLO 10	To design the layout of 2-input NAND, NOR gates.	PO 2	2
AEC117.11	CLO 11	Analysis of Frequency response of Common source amplifiers	PO 5	1
AEC117.12	CLO 12	Analysis of Frequency response of Common drain amplifiers.	PO 1	3
AEC117.13	CLO 13	Design and Simulation of Single Stage Cascode Amplifier.	PO 5	2
AEC117.14	CLO 14	Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier	PO 5	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3				2								1		
CLO 2	2	3											1		
CLO 3	3				3								1		
CLO 4	2				2								2		
CLO 5					2								3		
CLO 6	2	2											1		
CLO 7		2			2								2		
CLO 8					2								1		
CLO 9		3			2								2		
CLO 10		2											1		
CLO 11					1								2		
CLO 12	3												2		
CLO 13	3												2		
CLO 14	3												2		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 5	SEE Exams	PO 1, PO 2 PO 5	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2 PO 5	Student Viva	PO 1, PO 2 PO 5	Mini Project	-	Certification	-
Term Paper	-						

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS :

LIST OF EXPERIMENTS	
Week-1	**MOSFET**
To plot the (i) output characteristics(ii) Transfer characteristics of an n-channel and p-channel MOSFET.	
Week-2	**CMOS INVERTER**
To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.	
Week-3	**RING OSCILLATOR**
To design and plot the output characteristics of a 3-inverter ring oscillator.	
Week-4	**LOGIC GATES**
To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	
Week-5	**4X1 MULTIPLEXER**
To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.	
Week-6	**LATCHES**
To design and plot the characteristics of a positive and negative latch based on multiplexers.	
Week-7	**REGISTERS**
To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.	
Week-8	**DIFFERENTIAL AMPLIFIER**
Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR.	
Week-9	**NMOS INVERTER AND CMOS INVERTER**
To design layout of NMOS and CMOS inverter.	
Week-10	**LAYOUT OF 2-INPUT NAND, NOR GATES**
To design the layout of 2-input NAND, NOR gates.	
Week-11	**COMMON SOURCE AMPLIFIER**
Analysis of Frequency response of Common source amplifiers.	
Week-12	**COMMON DRAIN AMPLIFIER**
Analysis of Frequency response of Common drain amplifiers.	
Week-13	**SINGLE STAGE CASCODE AMPLIFIER**
Design and Simulation of Single Stage Cascode Amplifier.	
Week-14	**BASIC CURRENT MIRROR, CASCODE CURRENT MIRROR AMPLIFIER**
Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier.	

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No.	Topics to be covered	Course Learning Outcomes	Reference
1	Basics of output characteristics of an n- channel and p-channel MOSFET.	CLO 1	T1-2.1 ,2.2
2	Basic operation and static (VTC) and dynamic characteristics of a digital CMOS inverter.	CLO 2	T1-2.1 ,2.2
3	Basic operation and output characteristics of a 3-inverter ring oscillator.	CLO 3	T1-14.2
4	Basic operation and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	CLO 4	T3-12.1
5	Basic operation and characteristics of a 4x1 digital multiplexer using pass transistor logic.	CLO 5	T3-15.1
6	Basic operation and the characteristics of a positive and negative latch based on multiplexers.	CLO 6	T3-13.3
7	Basic operation and the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.	CLO 7	T3-15.1
8	Basic operation , Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR.	CLO 8	T1-4.1,4.2
9	Basic operation and layout of NMOS and CMOS inverter.	CLO 9	T1-2.1 ,2.2
10	Basic operation and design the layout of 2-input NAND, NOR gates.	CLO 10	T3-12.1
11	Basic operation and Frequency response of Common source Amplifiers.	CLO 11	T1-3.2
12	Basic operation and Frequency response of Common drain Amplifiers.	CLO 12	T1-3.3
13	Basic operation , design and Simulation of Single Stage Cascode Amplifier.	CLO 13	T1-5.1,5.2
14	Basic operation and Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier	CLO 14	T1-5.1,5.2

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S NO	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	To improve standards and analyze the concepts.	Seminars	PO 1, PO 2	PSO 1
2	Conditional probability, Sampling distribution, correlation, regression analysis and testing of hypothesis	Seminars / NPTEL	PO 2, PO5	PSO 1
3	Encourage students to solve real time applications and prepare towards competitive examinations.	NPTEL	PO 5	PSO 1

Prepared by:
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