INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

COMPUTER SCIENCE AND ENGINEERING

COURSE DESCRIPTOR

Course Title	ELECTRICAL AND ELECTRONICS ENGINEERING LAB				
Course Code	AEE101				
Programme	B. Tech				
Semester	II	CSE | IT			
Course Type	Foundation				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Mr. K Lingaswamy, Assistant Professor, EEE				
Course Faculty	Mr. K Lingaswamy, Assistant Professor, EEE Ms. Lekha chandran, Associate Professor,EEE Mr. P Mabu Hussain, Assistant Professor, EEE Mr. N Shivaprasad, Assistant Professor, EEE				

I. COURSE OVERVIEW:

Electrical and electronics engineering laboratory is introduced to get the practical experience on with identification of all the electrical components. It also aims to get the knowledge of the different electronic devices like diodes, rectifiers, transistors and to measure the electrical quantities with different measuring devices and CRO

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AHS006	I	Engineering Physics	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
ELECTRICAL AND ELECTRONICS ENGINEERING LAB	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✘	LCD / PPT	✔	Seminars	✘	Mini Project	✔	Videos
✔	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):
One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	**Performance**	**Calculations and Graph**	**Results and Error Analysis**	**Viva**	**Total**
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		**Strength**	**Proficiency assessed by**
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Calculations
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Videos
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Characteristic curves

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Analyzing theorems procedure
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	MATLAB simulation

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand, analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based systems of varying complexity.	-	-
PSO 2	**Problem-Solving Skills:** The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.	2	Presentation on real-world problems
PSO 3	**Successful Career and Entrepreneurship:** The ability to employ modern computer languages, environments, and platforms in creating innovative career paths to be an entrepreneur, and a zest for higher studies.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Analyze basic electrical circuits by implementing different circuits.
II	Apply circuit theorems to evaluate the behavior of electrical circuits.
III	Gain knowledge on semiconductor devices like diode and transistor
IV	Interpret different transistor configurations

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEE101.1	CLO 1	Apply Kirchhoff's current and voltage laws to linear electrical circuits using hardware	PO 1, PO 2	3
AEE101.2	CLO 2	Verification of superposition theorem using hardware	PO 1, PO 2	2
AEE101.3	CLO 3	Verification of Thevenin's theorem using hardware	PO 2, PO 3	2
AEE101.4	CLO 4	Verification of Norton's theorem using hardware.	PO 2, PO 3	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEE101.5	CLO 5	Verification of maximum power transfer theorem using hardware	PO 1, PO 4	3
AEE101.6	CLO 6	Apply Kirchhoff's current and voltage laws to linear electrical circuits using digital simulation	PO 1, PO 2, PO 5	3
AEE101.7	CLO 7	Verification of superposition and Thevenin's theorem using digital simulation.	PO 1, PO 2, PO 5	2
AEE101.8	CLO 8	Verification of Norton's theorem and maximum power transfer theorem using digital simulation.	PO 1, PO 2, PO 5	2
AEE101.9	CLO 9	Understand the PN junction diode characteristics	PO 1, PO 2	2
AEE101.10	CLO 10	Understand the zener diode characteristics	PO 1, PO 2	2
AEE101.11	CLO 11	Build half wave and full wave rectifier circuits	PO 1, PO 2, PO 3	2
AEE101.12	CLO 12	Understand transistor common base characteristics	PO 1, PO 2	2
AEE101.13	CLO 13	Understand transistor common emitter characteristics	PO 1, PO 2	2
AEE101.14	CLO 14	Explore the knowledge and skills of employability to succeed in national and international level competitive examinations.	PO 1, PO 2, PO 3, PO 4, PO 5	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2												3	
CLO 2	3	2													
CLO 3		2	2												
CLO 4		2	2											2	
CLO 5	3			2										2	
CLO 6	2	2			2									2	
CLO 7	2	2			2									2	
CLO 8	2	2			2									1	
CLO 9	2	2												1	
CLO 10	2	2												1	
CLO 11	2	2	2											1	
CLO 12	2	2												1	
CLO 13	2	2												1	
CLO 14	2	2	2	2	2									1	

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2 PO 3, PO 4, PO 5	SEE Exams	PO 1, PO 2 PO 3, PO 4 , PO 5	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2 PO 3, PO 4, PO 5	Student Viva	PO 1, PO 2 PO 3, PO 4, PO 5	Mini Project	-	Certification	-

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

LIST OF EXPERIMENTS	
Week-1	**KIRCHOFF'S LAWS**
Practical verification of Kirchhoff's current law and voltage law.	
Week-2	**SUPERPOSITION THEOREM**
Illustration of superposition theorem.	
Week-3	**THEVENIN'S THEOREM**
Obtain the equivalent circuit of the given electrical network using Thevenin's theorem.	
Week-4	**NORTON'S THEOREM**
Practical verification of Norton's theorem and obtain the equivalent circuit.	
Week-5	**MAXIMUM POWER TRANSFER THEOREM**
Verification of maximum power transfer theorem.	
Week-6	**KVL AND KCL**
Verification of KVL and KCL using digital simulation	
Week-7	**DIGITAL SIMULATION OF THEOREMS**
Superposition theorem and Thevenins theorem using digital simulation	
Week-8	**NORTON'S THEOREM AND MAXIMUM POWER TRANSFER THEOREM**
Norton's theorem and maximum power transfer theorem using digital simulation.	
Week-9	**P-N JUNCTION DIODE**
Volt Ampere characteristics of p-n junction diode.	
Week-10	**ZENER DIODE**
Understand the zener diode characteristics	
WeeK-11	**RECTIFIERS**
Build half wave and full wave rectifier circuits	
Week-12	**COMMON BASE TRANSISTOR**
Understand transistor common base characteristics	
Week-13	**COMMON EMITTER TRANSISTOR**
Understand transistor common emitter characteristics	
Text Books:	
1. A Chakrabarthy, "Electric Circuits", DhanipatRai & Sons, 6th Edition, 2010.	

2. C L Wadhwa "Electrical Circuit Analysis including Passive Network Synthesis", New Age International, 2nd Edition, 2009.
3. J P J Millman, C C Halkias, Satyabrata Jit, Millman's, "Electronic Devices and Circuits", Tata McGraw Hill, 2nd Edition, 1998.

Reference Books:

1. A Sudhakar, Shyammohan S Palli, "Circuits and Networks", Tata McGraw-Hill, 4th Edition, 2009.
2. R. L. Boylestad , Louis Nashelsky,"Electronic Devices and Circuits", PEI/PHI, 9th Edition, 2006.
3. A. K. Theraja, "Textbook of Electrical Technology", S. Chand, 1st Edition, 2014..
4. David A Bell, "Electric circuits", Oxford University Press, 7th Edition, 2009.

Web References:

1. https://www.nptel.ac.in/Courses/117106108
2. https://www.gnindia.dronacharya.info/EEEDept/labmanuals.html
3. https://www.textofvideo.nptel.iitm.ac.in
4. https://www.textofvideo.nptel.iitm.ac.in/

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Apply Kirchhoff's current and voltage laws to linear electrical circuits using hardware	CLO 1	T1:2.1, R1:1.6
2	Verification of superposition theorem using hardware	CLO 2	T1:3.1, R1:2.8
3	Verification of Thevenin's theorem using hardware	CLO 3	T1:3.2, R1:2.11
4	Verification of Norton's theorem using hardware.	CLO 4	T1:3.3, R1:3.4
5	Verification of maximum power transfer theorem using hardware	CLO 5	T1:3.4, R1:3.10
6	Apply Kirchhoff's current and voltage laws to linear electrical circuits using digital simulation	CLO 6	T1:2.1, R1:3.10
7	Verification of superposition and Thevenin's theorem using digital simulation.	CLO 7	T1:3.1, R1:3.10
8	Verification of Norton's theorem and maximum power transfer theorem using digital simulation.	CLO 8	T1:3.4, R1:7.1
9	Understand the PN junction diode characteristics	CLO 9	T3:7.6, R2:7.4
10	Understand the zener diode characteristics	CLO 10	T3:7.7, R2:7.6
11	Build half wave and full wave rectifier circuits	CLO 11	T3: 7.7, R2:7.3
12	Understand transistor common base characteristics	CLO 12	T3:7.7.7, R2:7.3
13	Understand transistor common emitter characteristics	CLO 13	T3:7.7.7, R2:7.5

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Include more DC Electrical network theorems	Guest lectures	PO 1, PO 5	PSO 2

Prepared by:
Mr. K Lingaswamy, Assistant Professor, EEE

HOD, FRESHMAN ENGINEERING