INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE DESCRIPTOR

Course Title	**INTEGRATED CIRCUITS APPLICATIONS LABORATORY**				
Course Code	AEC106				
Programme	B.Tech				
Semester	V	ECE | EEE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	-	-	-	3	2
Chief Coordinator	Mrs. J.Sravana, Assistant Professor				
Course Faculty	Ms. J.Sravana, Assistant Professor Mr. B. Naresh, Assistant Professor				

I. COURSE OVERVIEW:

This laboratory course builds on the lecture course "Integrated Circuits Applications "which is mandatory for all students of electronics and communication engineering. The course aims at practical experience with the characteristics and theoretical principles of linear and digital integrated circuits.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Digital System Design	4
UG	AEC006	IV	Pulse and Digital Circuits	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Integrated Circuits Applications Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✘	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to Day Performance	Final internal lab Assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	Performance	Calculations and Graph	Results and Error Analysis	Viva	Total
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Calculations of the observations
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Lab related Exercises
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Design Exercises

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Problem Solving:** Exploit the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work	2	Lab related Exercises
PSO 2	**Professional Skills:** Identify the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering, and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally.	-	-
PSO 3	**Modern Tools in Electrical Engineering:** Comprehend the technologies like PLC, PMC, process controllers, transducers and HMI and design, install, test, maintain power systems and industrial applications.	-	-

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OUTCOMES (COs):

The course should enable the students to:	
I	Discuss the analysis of Op-Amp for different configurations and its properties.
II	Analyze and design the linear and non linear applications of Op-Amp.
III	Design the various filters using Op-Amp and analysis of Multivibrators using 555 Timer.

IV	Describe the various ADC and DAC techniques.
V	Explore the concepts of Combinational and sequential logic circuits using digital IC's.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
AEC106.01	CLO 1	Understand the performance of an inverting, non-inverting amplifier and differential amplifiers.	PO 1, PO 2	3
AEC106.02	CLO 2	Demonstrate an integrator and differentiator using IC 741.	PO 1, PO 2	3
AEC106.03	CLO 3	Calculate and verify the cut off frequencies of active low pass and high pass filters using IC 741.	PO 1, PO 2	3
AEC106.04	CLO 4	Measure the time periods of an astable multivibrators using IC 555.	PO 1, PO 2	2
AEC106.05	CLO 5	Measure the time periods of monostable multivibrators using IC 555.	PO 1, PO 2	2
AEC106.06	CLO 6	Determine the triggering points of schimitt trigger using NE555 Timer.	PO 1, PO 2	2
AEC106.07	CLO 7	Analyze the characteristics of phase locked loop and verify the operation of instrumentation amplifier .	PO 1, PO 2	2
AEC106.08	CLO 8	Verify functionality of multiplexer and demultiplexer.	PO 1, PO 5	3
AEC106.09	CLO 9	Verify functionality of encoder and decoder.	PO 1, PO 5	3
AEC106.10	CLO 10	Verify functionality of various flip-flops.	PO 1, PO 5	2
AEC106.11	CLO 11	Verify functionality of counters and realize using flip-flops.	PO 1, PO 5	2
AEC106.12	CLO 12	Verify functionality of shift registers and realize using flip-flops.	PO 1, PO 5	2

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3	2											2		
CLO 2	3	2											2		
CLO 3	3	2											2		
CLO 4	2	2											2		

Course Learning Outcomes (CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 5	2	2											2		
CLO 6	2	2											2		
CLO 7	2	2													
CLO 8	3				2								2		
CLO 9	3				2								2		
CLO 10	2				2										
CLO 11	2				2								2		
CLO 12	2				2								2		

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO1, PO2 PO5,PSO1	SEE Exams	PO1, PO2 PO5,PSO1	Assignments	-	Seminars	-
Laboratory Practices	PO1, PO2 PO5,PSO1	Student Viva	PO1, PO2 PO5,PSO1	Mini Project	-	Certification	-

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

LIST OF EXPERIMENTS	
Week-1	**INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS**
To construct and test the performance of an Inverting, Non-inverting amplifier and Differential amplifier using IC 741.	
Week-2	**INTEGRATOR AND DIFFERENTIATOR**
To construct and test the performance of an Integrator and Differentiator using IC 741.	
Week-3	**SECOND ORDER ACTIVE LOWPASS, HIGHPASS AND BANDPASS FILTERS**
To design and verify the operation of the Active low pass, High pass and Band pass filters using IC 741.	
Week-4	**ASTABLE MULTIVIBRATORS AND SCHMITT TRIGGER USING 555**
To design and construct an astable multivibrators and Schmitt trigger using IC 555.	

Week-5	**MONOSTABLE MULTIVIBRATORS 555**
To design and construct Monostable multivibrators using IC 555.	
Week-6	**SCHMITT TRIGGER USING 555**
To design and construct schimitt trigger using NE555 Timer.	
Week-7	**PLL USING IC 565**
Verifying characteristics of PLL.	
Week-8	**INSTRUMENTATION AMPLIFIER**
To design and verify the operation of instrumentation amplifier using IC 741.	
Week-9	**MULTIPLEXER AND DEMULTIPLEXER**
Verify Functionality of multiplexer and demultiplexer.	
Week-10	**ENCODER AND DECODER**
Verify Functionality of encoder and decoder.	
WeeK-11	**REALISATION OF DIFFERENT FLIP-FLOPS USING LOGIC GATES**
Verify Functionality of flip-flops.	
Week-12	**4 BIT COUNTERS**
Verify Functionality of counters.	
Week-13	**SHIFT REGISTERS**
Verify Functionality of shift registers	

Text Books:

1. D. Roy Chowdhury, "Linear Integrated Circuits", New age international (p) Ltd, 2nd Edition, 2003.
2. Ramakanth A. Gayakwad, "Op-Amps & linear ICs", PHI, 3rd Edition,2003.
3. John F. Wakerly, "Digital Design Principles and Practices", Prentice Hall, 3rd Edition, 2005.

Reference Books:

1. Salivahanan, "Linear Integrated Circuits and Applications", TMH, 1st Edition, 2008.

Web References:

1. http://www.ee.iitkgp.ac.in
2. http://www.citchennai.edu.in

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No.	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Understand the performance of an inverting, non-inverting amplifier and differential amplifier .	CLO 1	T1:2.2 T2:1.2-1.7
2	Plot the response for different time constants of an integrator and differentiator using IC 741.	CLO 2	T1:2.5 R1:3.4
3	Calculate and verify the cut off frequencies of active low pass and high pass filters using IC 741.	CLO 3	T1:2.4
4	Measure the time periods of an astable multivibrators using IC 555.	CLO 4	T2:1.12-1.13
5	Measure the time periods of mono stable multivibrators using IC 555.	CLO 5	T2:1.12-1.13
6	Determine the triggering points of schimitt trigger using NE555 Timer.	CLO 6	T1:3.2
7	Analyze the characteristics of phase locked loop using IC 565.	CLO 6	T1:3.3-3.4
8	Demonstrate and verify the operation of instrumentation amplifier using IC 741.	CLO 7	T1:8.2-8.5
9	Verify functionality of multiplexer and demultiplexer.	CLO 8	T1:8.5 R1:6.8
10	Verify functionality of encoder and decoder and realize using logic gates.	CLO 9	T1:10.3 R1:5.4
11	Verify functionality of various flip-flops and realize using logic gates.	CLO 10	T3:3.12 R1:12.7
12	Verify functionality of counters and realize using flip flops.	CLO 11	T3:7.2
13	Verify functionality shift registers and realize using flip flops.	CLO 12	T3:8.4

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S. No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	To improve standards and analyze the concepts.	NPTEL	PO 1, PO 2	PSO 1
2	Implement parallel and serial adders.	Seminars / NPTEL	PO 1, PO5	PSO 1
3	Encourage students to solve real time applications and prepare towards competitive examinations.	NPTEL	PO 1, PO2, PO5	PSO 1

Prepared by:
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