INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

ELECTRONICS ANDCOMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING**				
Course Code	BESB02				
Programme	M.Tech (ES)				
Semester	I	ECE			
Course Type	Core				
Regulation	**IARE - R18**				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	3	2
Chief Coordinator	Dr. P Munaswami, Professor, ECE				
Course Faculty	Mr. K.Chaitanya, Assistant Professor, ECE				

I. COURSE OVERVIEW:

This course starts by introducing some basic ideas of ARM Cortex-M3 Processor and LPC 17XX Microcontroller architectures and their features. Subsequently the course covers Programmable DSP Processor architecture. As we progress with the course students will be familiarized with the programming models of Microcontrollers and P-DSPs and their applications in real world.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC013	VI	Microprocessors and Microcontrollers	4
UG	AEC012	VI	Digital Signal Processing	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Microcontrollers And Programmable Digital Signal Processing	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✔	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✔	Seminars	✘	Mini Project	✘	Videos
✘	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make- examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weight age in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with „either‟ „or‟ choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept.
30 %	To test the analytical skill of the concept.
20 %	To test the application skill of the concept.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper.

Table 1: Assessment pattern for CIA

Component	**Theory**		**Total Marks**
Type of Assessment	**CIE Exam**	**Technical Seminar and Term Paper**	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):
Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:
Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	Independently carry out research/investigation and development work to solve practical problems	2	Quiz
PO 3	Apply advanced level knowledge, techniques, skills and modern tools in the field of Embedded Systems.	2	Assignments
PO 6	Understand the importance of embedded technologies and design new innovative products for solving society relevant problems	3	Seminars
PO 7	Recognize the need to engage in lifelong learning through Continuing education and research.	2	Term paper

3= High; 2 = Medium; 1 = Low

VII COURSE OBJECTIVES:

The course should enable the students to:

I	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
II	Identify and characterize architecture of Programmable DSP Processors.
III	Develop small applications by utilizing the ARM processor core and DSP processor based platform.

VIII COURSE OUTCOMES (COs):

COs	Course Outcome	CLOs	Course Learning Outcome
CO 1	Analyze the characteristics of ARM Cortex-M3 processor.	CLO 1	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.
		CLO 2	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.
		CLO 3	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.
CO 2	Understand the various Exceptions and Interrupts in Cortex-M3 processor.	CLO 4	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions
		CLO 5	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.
		CLO 6	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.
CO 3	Study the features of LPC 17xx microcontrollers based on Cortex-M3 processor.	CLO 7	Describe the LPC 17xx microcontroller- Internal memory, GPIOs, Timers.
		CLO 8	Study the features of ADC, UART and other serial interfaces.
		CLO 9	Understand the concepts of PWM, RTC, WDT
CO 4	Identify and analyze the characteristics Programmable DSP Processors.	CLO 10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.

COs	Course Outcome	CLOs	Course Learning Outcome
		CLO 11	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.
		CLO 12	Understand the Introduction to TI DSP processor family.
CO 5	Understand the TMS320C6000 series DSP Processor architectures.	CLO 13	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.
		CLO 14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.
		CLO 15	Describe the Code Composer Studio for application development for digital signal processing, On chip Peripherals, Processor benchmarking.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB02.01	CLO 1	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.	PO1	3
BESB02.02	CLO 2	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.	PO1	2
BESB02.03	CLO 3	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.	PO3	2
BESB02.04	CLO 4	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions	PO1 PO6	2
BESB02.05	CLO 5	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.	PO1 PO7	2
BESB02.06	CLO 6	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	PO3	3
BESB02.07	CLO 7	Describe the LPC 17xx microcontroller-Internal memory, GPIOs, Timers.	PO7	3
BESB02.08	CLO 8	Study the features of ADC, UART and other serial interfaces.	PO1	2
BESB02.09	CLO 9	Understand the concepts of PWM, RTC, WDT.	PO3 PO6	2
BESB02.10	CLO 10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	PO1 PO7	2
BESB02.11	CLO 11	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.	PO1	2
BESB02.12	CLO 12	Understand the Introduction to TI DSP processor family.	PO6	2
BESB02.13	CLO 13	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.	PO1	2

CLO Code	CLO's	At the end of the course, the student will have the ability to:	PO's Mapped	Strength of Mapping
BESB02.14	CLO 14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.	PO3	3
BESB02.15	CLO 15	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.	PO1	2

3= High; 2 = Medium; 1 = Low

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

Course Outcomes (COs)	Program Outcomes (PO)			
	PO 1	PO 3	PO 6	PO 7
CO 1	3	2		
CO 2	2	3	2	2
CO 3	2	2	2	3
CO 4	2		2	2
CO 5	2	3		

3= High; 2 = Medium; 1 = Low

XI. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES:

CLOs	POs			
	PO 1	PO 3	PO 6	PO 7
CLO 1	3			
CLO 2	2			
CLO 3		2		
CLO 4	2		2	
CLO 5	2			2
CLO 6		3		
CLO 7				3
CLO 8	2			
CLO 9		2	2	
CLO 10	2			2
CLO 11	2			
CLO 12			2	
CLO 13	2			
CLO 14		3		
CLO 15	2			

3= High; 2 = Medium; 1 = Low

XII. ASSESSMENT METHODOLOGIES–DIRECT:

CIE Exams	PO 1, PO 3 PO 6, PO 7	SEE Exams	PO 1, PO 3 PO 6, PO 7	Assignments	PO 3	Seminars	PO 6
Laboratory Practices	-	Student Viva	-	Mini Project	-	Certification	-
Term Paper	PO 6						

XIII. ASSESSMENT METHODOLOGIES–INDIRECT:

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIV. SYLLABUS:

UNIT – I	**SYSTEMS ARM CORTEX-M3 PROCESSOR**	**Classes: 09**
ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.		
UNIT – II	**EXCEPTIONS AND INTERRUPTS**	**Classes: 09**
Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.		
UNIT – III	**LPC 17XX MICROCONTROLLER**	**Classes: 09**
LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC. UART and other serial interfaces, PWM, RTC, WDT.		
UNIT – IV	**PROGRAMMABLE DSP (P-DSP) PROCESSORS**	**Classes: 09**
Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.		
UNIT – V	**VLIW ARCHITECTURE**	**Classes: 09**
VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking.		
Text Books:		
1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 3rd Edition,2014 2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition, 2011.		
Reference Books:		
1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.		

2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Educations.
3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley Publications.

XV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Lecture No.	Topic Outcomes	Topics to be covered	Reference
1-3	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.	ARM Cortex-M3 processor: Applications Programming model – Registers Operation modes, Exceptions and Interrupt, Reset Sequence	T1: 1.1, 1.5,2.2 2.3, 3.7
4-7	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.	Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes Permissions, Bit-Band Operations	T1: 4.1 5.2,5.5
8- 11	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.	Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces	T1: 6.1
12-17	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions	Exceptions,Types,Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions	T1: 7.1, 7.2 7.4,7.5
18-20	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.	Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller	T2: 7.6,8.1
21-22	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	Basic Configuration, SYSTICK Timer, Interrupt Sequences Exits, Tail Chaining, Interrupt Latency	T1: 8.2, 8.5 9.1,9.2, 9.7
23-27	Describe the LPC 17xx microcontroller-Internal memory, GPIOs, Timers.	LPC17xx microcontroller-Internal memory, GPIOs, Timers.	R4: 8.4,8.10,8.21
28-32	Study the features of ADC, UART and other serial interfaces	ADC, UART, Other serial interfaces	R4: 8.14, 8.16,8.17
33-35	Understand the concepts of PWM, RTC, WDT	PWM,RTC, WDT	R4: 8.228.28,8.27
36-39	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	Programmable DSP Processors ,Harvard architecture Multi-port memory Multi-port memory	T2: 2.1 2.2,2.4
40-42	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.	Architectural structure of P-DSP,Architectural structure of P-DSP,MAC unit, Barrel shifters	T2: 3.1,2.1,10.7
43-46	Understand the Introduction to TI DSP processor family.	Introduction to TI DSP processor family	T2: 2.5
47-49	Study the VLIW architecture and	VLIW architecture and	T2: 2.5,13.4

Lecture No.	Topic Outcomes	Topics to be covered	Reference
	TMS320C6000 series, architecture study, data paths, cross paths.	TMS320C6000 series Architecture study, data paths, cross paths	
50-52	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.	Introduction to Instruction level architecture of C6000 family Assembly Instructions memory addressing, Arithmetic, logical operations	T2: 13.3 13.6,13.5
53-55	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.	Code Composer Studio Code Composer Studio for application development for digital signal processing on chip peripherals Processor benchmarking	T2:13.11, 2.8,14.12

XVI. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed Actions	Relevance With POs
1	Design examples of ARM Cortex-M3 processor.	Project	PO 1, PO 3, PO 7
2	Program modelling	Seminars / Guest Lectures / NPTEL	PO 1,PO 3, PO 6
3	Case studies of different DSP applications.	Seminars / Guest Lectures / NPTEL	PO 1, PO 3,PO 6

Prepared by:
Mr. K Chaitanya, Assistant Professor

HOD, ECE