# COURSE CONTENT

| DESIGN FOR TESTABILITY | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **I Semester: M.TECH – ES** | | | | | | | | |
| **Course Code** | **Category** | **Hours / Week** | | | **Credits** | **Maximum Marks** | | |
| **BESD09** | **ELECTIVE** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| | | 3 | - | - | 3 | 40 | 60 | 100 |
| **Contact Classes: 48** | **Tutorial Classes: Nil** | **Practical Classes: Nil** | | | | **Total Classes: 48** | | |
| **Prerequisite:** | | | | | | | | |

## I. COURSE OVERVIEW:

This course is intended to give fundamental knowledge on different types of testing. Understand different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits. This course covers complete knowledge about different methods of simulation and algorithms associated with testing. These courses also covers advanced testing built in self test and boundary scan testing.

## II. COURSES OBJECTIVES:

**The students will try to learn**

I. The different techniques available for VLSI testing and fault models to the logic circuits.
II. The high level testability measures and various scan based testing.
III. Various test Pattern generation techniques for BIST and Boundary scan standard.

## III. COURSE OUTCOMES:

**At the end of the course students should be able to:**

CO 1 Acquire verification knowledge and Fault modeling to test analog and digital circuits
CO 2 Design for testability rules and techniques.
CO 3 Learn the algorithms for fault simulation
CO 4 Utilize the scan architectures for different digital circuits.
CO 5 Acquire the knowledge of design of built-in-self test.
CO 6 Acquire the knowledge of language for boundary scan test

## IV. COURSE CONTENT:

**MODULE – I: INTRODUCTION TO TESTING (09)**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

**MODULE –II: LOGIC AND FAULT SIMULATION (09)**

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

**MODULE –III: TESTABILITY MEASURES (09)**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**MODULE –IV: BUILT-IN SELF-TEST (09)**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

**MODULE –V: BOUNDARY SCAN STANDARD (09)**

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions

## V. TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic PublishersC.A. Balanis, "Antenna Theory", John Wiley and Sons, 2nd Edition, 2001

## VI. REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House.
2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press