INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal - 500 043, Hyderabad, Telangana

COURSE CONTENT

ADVANCED DIGITAL SYSTEM DESIGN								
III Semester: ES								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
BESE31	**Elective**	3	0	0	3	40	60	100
Contact Classes: 45	**Tutorial Classes: Nil**	**Practical Classes: Nil**				**Total Classes: 45**		
Prerequisite: Digital System Design.								

I. COURSE OVERVIEW:

This course introduces the fundamental concepts and basic building blocks of digital circuits. It focuses on number systems designing of optimized combinational and sequential circuits, memories, programmable logic devices and the key concepts of hardware description language (VHDL). The applications include in the area of VLSI design, microprocessors, microcontrollers and embedded systems.

II. COURSES OBJECTIVES:

The students will try to learn

I. The analysis and design of clocked synchronous and asynchronous sequential circuits, including state diagrams, state tables, state reduction, and modeling techniques using ASM charts.
II. Digital circuit modeling using Verilog HDL, covering various modeling styles—gate level, dataflow, behavioral, and structural—and applying these to design combinational and sequential systems.
III. The fault detection, diagnosis, and testability algorithms such as the D-algorithm, Boolean difference method, and design-for-testability (DFT) schemes for ensuring reliable circuit operation.
IV. How to design and implement finite state machines and digital systems using PLDs, PALs, PLAs, and FPGAs, with an emphasis on Xilinx FPGA architecture and synthesis tools.

III. COURSE OUTCOMES:

At the end of the course students should be able to:

CO1 Outline binary arithmetic operations and optimize Boolean functions using Karnaugh and tabulatmethod.
CO2 ke use of basic logic gates to realize the combinational logic circuits used in conventional electro circuits
CO3 ɾrpret the knowledge of flip-flops and latches in synchronous and asynchronous modules for mem Storing.
CO4 Develop Mealy/Moore models and state diagrams for the complex sequential circuit applications.
CO5 ntify the different logic families, memories and programmable logic devices for understanding architectural blocks of FPGA.
CO6 nonstrate the different modelling styles and data types in VHDL for implementing combinational sequential circuits.

IV. COURSE CONTENT:

MODULE - I: SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of clocked synchronous sequential circuits and modelling- state diagram, state table, state table assignment reduction-design of synchronous sequential circuits design of iterative circuits, ASM chart and realization using ASM.

Verilog HDL Coding Style: Overview of Digital Design with Verilog HDL, Hierarchical Modeling Concepts, Basic Concepts of Modules and Ports, Gate Level Modeling, Dataflow Modeling, Behavioral Modeling, Tasks and Functions, Useful Modeling Techniques.

MODULE –II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of asynchronous sequential circuit, flow table reduction-races-state assignment transition table and problems in transition table, design of asynchronous sequential circuit, static, dynamic and essential hazards, mixed operating mode asynchronous circuits, designing vending machine controller.

MODULE –III: FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9)

Fault table method-path sensitization method, Boolean difference Method - D algorithm, tolerance Techniques.

The compact algorithm, fault in PLA, test generation, DFT schemes, built in self, test.

MODULE –IV: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9)

Programming logic device families, designing a synchronous sequential circuit using PLA/PAL, designing ROMwith PLA, realization of finite state machine using PLD, FPGA, Xilinx FPGA, Xilinx 4000.

MODULE –V: SYSTEM DESIGN USING VERILOG (9)

Hardware modelling with Verilog HDL, logic system, data types and operators for modelling in Verilog HDL, behavioral descriptions in Verilog HDL, HDL based synthesis, synthesis of finite state machines, structural modelling, compilation and simulation of Verilog code, test bench, realization of combinational and sequential circuits using Verilog, registers, counters, sequential machine, serial adder, multiplier, divider, design of simple microprocessor, introduction to system Verilog.

V. TEXT BOOKS:

1. Chandrakasan, teal, design of High, performance Microprocessor Circuits, IEEE Press, 2001.
2. Harris, Skew-tolerant Circuit Design, Morgan Kaufmann, 2000.
3. Bernstein, teal, high Speed CMOS Design Styles, Kluwer Academic Publishers, 1998.
4. Weste and D. Harris, CMOS VLSI Design, Addison, Wesley, 4th Edition, 2010.

VI. REFERENCE BOOKS:

1. Charles H. Roth jr., “Fundamentals of Logic Design” Thomson Learning, 2013.
2. M.D. Ciletti, modeling, synthesis and Rapid Prototyping with the Verilog HDL, prentice Hall, 1999.
3. M.G. Arnold, Verilog Digital, computer Design, prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India, 2001.
5. Parag k. Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002.
6. Parag k. Lala “Digital System Design Using PLD” B S Publications, 2003.

VII. MATERIALS ONLINE

1. Course template
2. Tutorial question bank
3. Assignments
4. Model question paper - I
5. Model question paper - II
6. Lecture notes
7. Power point presentations
8. Early Lecture Readiness Videos