INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

ATTAINMENT OF COURSE OUTCOMES (COs) – ACTION PLAN

Name of the Faculty	**Ms.M.Lavanya**	Department	**CSE**
Regulations	**R16**	Batch	**2017 -2021**
Course Name	**Digital Logic Design**	Course Code:	**AEC020**
Semester	**III**	Target Value	**70% (2.1 on 3 Scale)**

Attainment of COs:

	Course Outcomes	Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1	Understand the different forms of number representations and binary codes in digital logic circuits.	2	2.5	2.1	Target attained
CO2	Make use of Boolean postulates, theorems and k-map for obtaining minimized Boolean expressions.	1.3	2.4	1.5	Target not attained
CO3	Implement the combinational logic circuits using the logic gates.	1.3	2.5	1.5	Target not attained
CO4	Utilize the functionality and characteristics of flip-flops and latches for designing sequential circuits.	2.3	2.5	2.3	Target attained
CO5	Construct the synchronous and asynchronous modules using flip-flops used for memory storing applications.	0.9	2.5	1.2	Target not attained
CO6	Extend the knowledge of memories and programmable logic devices for understanding the architectural blocks of FPGA.	2.3	2.4	2.3	Target attained

Action taken report:
CO2: Exercise on K-Map and minimization of Boolean expressions to be given during tutorial sessions.
CO3: Need to discuss elaboratively how to use logic gates in designing combinational circuits.
CO5: Expert lecture from industry to be organized on construction of Synchronous and Asynchronous modules so that student can understand importance flip flops for memory storing applications.

Lavanya
Course Coordinator

Mentor

HOD

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