



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad -500 043

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

ATTAINMENT OF COURSE OUTCOMES (COS) – ACTION PLAN

Name of the Faculty	Ms. M. Lavanya	Department	CSE
Regulations	R16	Batch	2017-2021
Course Name	Digital Logic Design Laboratory	Course Code	AEC116
Semester	III	Target Value	60% (1.8 on 3 Scale)

Attainment of COs:

Course Outcomes		Overall Attainment	Observation
CO1	Identify the functionality of Boolean expression using logic gates such as AND, OR, NOT, NAND, NOR, XOR and XNOR gates.	3	Target attained
CO2	Build combinational circuits such as adder, subtractor, multiplexers and comparators realization using low level elementary blocks.	3	Target attained
CO3	Analyze the operation of medium complexity standard combinational circuits like the code converters used to minimize the boolean expressions.	3	Target attained
CO4	Analyze the operation of a flip-flop and examine relevant timing diagrams	3	Target attained
CO5	Design complex digital system such as ALU to perform arithmetic and bitwise operators.	3	Target attained
CO6	Build the universal shift registers, counters using the flip flops..	3	Target attained

Lavanya
Course Coordinator

B9
Mentor

Hodhul
HOD

Head of the Department
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