

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	Ms.B Laksmiprasanna	Department:	ECE 2016-2020 AEC013	
Regulation:	IARE-R16	Batch:		
Course Name:	Microprocessors and Microcontrollers	Course Code:		
Semester:	VI	Target Value:	60% (1.8)	

Attainment of Cos.

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observations
CO1	Outline the functional components of microprocessors and microcontrollers for understanding the operation of architectures.	3.00	2.40	2.9	Attained
CO2	Make use of addressing modes and instruction set of target microprocessors and microcontrollers for writing an assembly language programs to perform a task.	1.60	2.30	1.7	Not attained
CO3	Demonstrate the internal architecture and modes of operation of peripheral devices for interfacing memory and I/O devices.	0.90	2.40	1.2	Not attained
CO4	Illustrate the interrupt handling mechanism in microprocessors and microcontrollers using interrupt controller.	1.60	2.30	1.7	Not attained
CO5	Choose an appropriate data transfer scheme and hardware for data transfer between the devices.	0.90	2.30	1.2	Not attained
CO6	Develop microprocessor and microcontroller-based applications using necessary input and output devices.	0.90	2.30	1.2	Not attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

In this Course, the CO2, CO3, CO4, CO5, and CO6 requires additional attention and it is improved by

1. Conducting Guest lectures on addressing modes and instruction set of target microprocessors and microcontrollers for writing an assembly language programs. 2. Additional inputs will be provided on the internal architecture and modes of operation of peripheral devices for interfacing

memory and I/O devices for better understanding.

3. Giving assignments and conducting tutorials on data transfer scheme and hardware for data transfer between the devices for more practice

4. Practice tests are conducted on interrupt handling and data transfer schemes.

B.I Paganha

Ballagane.
Mentor

Head of the Department

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