

## INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043

## **ELECTRONICS AND COMMUNICATION ENGINEERING**

## ATTAINMENT OF COURSE OUTCOME- ACTION TAKEN REPORT

Name of the Faculty:	Dr V. Vijay	Department:	ECE	
Regulation:	IARE-R16	Branch:	2017-2021	
Course Name:	Digital System Design	Course Code:	AEC002	
Semester:	III	Target Value:	60% (1.8)	

## Attainment of COs:

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observations	
CO1	Outline binary arithmetic operations and optimize Boolean functions using Karnaugh and tabulation method.	3	2.5	2.9	Attainment target reached	
CO2	Apply combinational circuits for realization of basic building blocks of conventional electronic circuits.	2.3	2.5	2.3	Attainment target reached	
CO3	Interpret the knowledge of flip-flops and latches in synchronous and asynchronous modules for memory storing applications.	0.6	2.5	1	Attainment target is not yet reached	
CO4	Extend the logic design techniques for ECL, TTL and CMOS methodologies for designing the fundamental gate level modelling.	0.6	2.5	1	Attainment target is not yet reached	
CO5	Analyze the characteristics of logic families and PLDs to enhance the design skills in digital integrated circuits.	0.6	2.5	1	Attainment target is not yet reached	
CO6	Evaluate synthesis and simulation of VHDL modules for implementing combinational and sequential circuits for computer aided design tools.	0.6	2.6	1	Attainment target is not yet reached	

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

CO 3: Additional inputs are provided on flip-flops and latches sum of products and product of sums forms.

CO 4: Additional inputs are provided for ECL, TTL, and CMOS techniques.

CO 5: Additional inputs are provided on design of combinational circuits using conventional AND, OR, NOT, NAND, NOR and

EX-OR gates.

CO 6: Conducting Guest lectures on VHDL modules.

Course Coordinator

Mentor

DIOD

Head of the Department
Electronics and Communication Engineering
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