

(Autonomous)

Dundigal, Hyderabad - 500043, Telangana

ELECTRONICS AND COMMUNICATION ENGINEERING

ATTAINMENT OF COURSE OUTCOME - ACTION TAKEN REPORT

Name of the faculty:	Ms. KS INDRANI	Department:	Electronics and Communication Engineering			
Regulation:	IARE - R20	Batch:	2020-2024			
Course Name:	VLSI Design Laboratory	Course Code:	AECC54			
Semester:	VII	Target Value:	60% (1.8)			

Attainment of COs:

Course Outcome		Direct Attainment	Indirect Attainment	Overall Attainment	Observation
CO1	Make use of the static, dynamic and noise margin parameters of CMOS circuits for calculating figure of merit	3.00	0.00	3	Attained
CO2	Analyze complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays	3.00	0.00	3	Attained
CO3	Utilize existing small building block and circuit symbols with necessary inter connections to realize complex designs	3.00	0.00	3	Attained
CO4	Examine the conditions for optimum performance of lathes and registers with the knowledge of digital system design	3.00	0.00	3	Attained
CO5	Identify bandwidth, gain, and common mode rejection ratio parameters for cascode amplifiers to protect amplifier from miller effect, impact of short channel effects with the design of CNTFET and FINFET.	3.00	0.00	3 .	Attained
CO6	Apply the design rule check and Layout versus schematic check on layout of MOS circuits to verify spacing rules between layers.	3.00	0.00	3	Attained

Action Taken Report: (To be filled by the concerned faculty / course coordinator)

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