

INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 COURSE DESCRIPTION

Branch	ELECT	ELECTRONICS AND COMMUNICATION ENGINEERING						
Course Title	EMBEL	EMBEDDED SYSTEM DESIGN						
Course Code	BESB01	BESB01						
Program	M.Tech(H	M.Tech(EMBEDDED SYSTEMS)						
Semester	Ι	Ι						
Course Type	Profession	Professional Core						
Regulation	R18							
		Theory		Pra	ctical			
Course Structure	Lecture	Lecture Tutorials Credits Laboratory Credits						
	3 - 3							
Course Coordinator	Dr. V Padmanabha Reddy, Professor							

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	-	-	Microprocessors and Microcontrollers

II COURSE OVERVIEW:

This course is allows the students to learn the fundamentals of embedded system hardware and firmware design. It focuses on basics of embedded systems, embedded firmware design approaches, development languages and system design. The knowledge acquired from this course will enable the students to implement embedded hardware projects and models for engineering and scientific applications.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Embedded System Design	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	PPT		Chalk & Talk	x	Assignments	x	MOOC
x	Open Endeded Experiments	\checkmark	Seminars	x	Mini Project	x	Videos
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with either or choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept
30 %	To test the analytical skill of the concept
20 %	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	The	Total Marks	
Type of Assessment	CIE Exam Seminar and Term		10tai Marks
		Paper	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

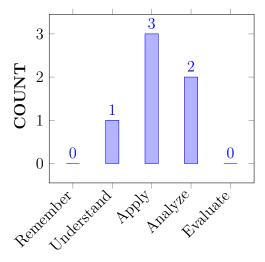
Ι	Introduce the difference between embedded systems and general purpose systems.
II	Optimize hardware designs of custom single-purpose processors
III	Compare different approaches in optimizing general-purpose processors.
IV	Introduce different peripheral interfaces to embedded systems.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Demonstrate the concepts of embedded systems and formalisms	Understand
	for System design.	
CO 2	Identify the suitable hardware and memory technology for	Apply
	different applications to meet the ever growing needs of the	
	embedded applications.	
CO 3	Select the other components required for interfacing I/O devices	Apply
	with embedded systems.	
CO 4	Categorize the embedded firmware design approaches and	Analyze
	development languages used for programming embedded devices.	
CO 5	Make use an appropriate Real-time operating system and software	Apply
	tools for embedded system based design.	
CO 6	Detect the task communication and synchronization methods to	Analyze
	access multiple concurrent threads and tasks	

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to
	solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of
	the program. The mastery should be at a level of higher than the
	requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer
	skillful at designing embedded systems for effective use in communications,
	IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively,
	creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in life long learning through continuing
	education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 3	Demonstrate the importance of embedded technologies and design innovative products for solving society relevant problems.	3	SEE/CIE/AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	2	SEE/CIE/AAT
PO 6	Recognize the need to engage in life long learning through continuing education and research.	1	SEE/CIE/AAT

3 = High; 2 = Medium; 1 = Low

X MAPPING OF EACH CO WITH PO(s):

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO1	-	-	\checkmark	\checkmark	-	-	
CO2	-	-	\checkmark	\checkmark	-	-	
CO3	-	-	\checkmark	\checkmark	-	-	
CO4	-	-	\checkmark	\checkmark	-	\checkmark	
CO5	-	-	\checkmark	\checkmark	-	\checkmark	
CO6	-	-	\checkmark	\checkmark	-	\checkmark	

XI JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge , understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions to get the solution development and communicate effectively in writing / orally societal problems .	4
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO2	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO3	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge , understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO4	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas .	1

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO5	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems .	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas.	1
CO6	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO6	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas .	1

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – PO/ PSO MAPPING:

COURSE		PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6		
	6	6	9	10	7	8		
CO 1	-	-	4	5	-	-		
CO 2	-	-	6	5	_	-		
CO 3		-	5	5	-	-		
CO 4	-	-	5	5	-	1		
CO 5	-	-	6	5	-	1		
CO 6	-	-	6	5	-	1		

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO/ PSO :

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO 1	-	-	44.4	50	-	-	
CO 2	-	-	66.6	50	-	-	
CO 3		-	55.5	50	-	-	
CO 4	-	-	55.5	50	-	12.5	
CO 5	-	-	66.6	50	-	12.5	
CO 6	-	-	66.6	50	-	12.5	

XIV COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation. $\boldsymbol{0} - 0 \leq C \leq 5\%$ – No correlation

 $1 -5 < C \le 40\% - Low/Slight$

2 - 40 % < C < 60% –Moderate

3	- 60%	\leq	C <	100% –	Substantial	/High
---	-------	--------	-----	--------	-------------	-------

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	-	-	2	2	-	-
CO 2	-	-	3	2	-	-
CO 3	-	-	2	2	-	-
CO 4	-	-	2	2	-	1
CO 5	-	-	3	2	-	1
CO 6	-	-	3	2	-	1
TOTAL	-	-	15	12	-	3
AVERAGE	-	-	2.5	2	-	1

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	\checkmark	Seminars	\checkmark	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XVI ASSESSMENT METHODOLOGY INDIRECT:

		\checkmark	End Semester OBE Feed Back
--	--	--------------	----------------------------

XVII SYLLABUS:

MODULE I	INTRODUCTION TO EMBEDDED SYSTEMS
	Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.
MODULE II	TYPICAL EMBEDDED SYSTEM
	Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.
MODULE III	EMBEDDED FIRMWARE
	Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.
MODULE IV	RTOS BASED EMBEDDED SYSTEM DESIGN
	Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling
MODULE V	TASK COMMUNICATION
	Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS

TEXTBOOKS

1. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley Publications, 3rd Edition, 2006

REFERENCE BOOKS:

- 1. Raj Kamal, "Embedded Systems", TMH, 2 nd Edition, 2008.
- 2. Shibu K.V, "Introduction to Embedded Systems, McGraw Hill, 3rd Edition, 2012.
- 3. Lyla, "Embedded Systems", Pearson Education , 2 nd Edition, 2013.

WEB REFERENCES:

- 1. http://www.nptelvideos.in/2012/11/embedded-systems.html
- 2. https://embedded system.com
- 3. https://www.youtube.com/watch?v=hELr9-7aAG8

COURSE WEB PAGE:

1. https://lms.iare.ac.in/index?route=course/details&course_id=1192

XVIII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference T1: 4.1
	OBE DISCUSSION		
1	Course Description on Outcome Based Education(OBE): Course Objectives,Course Outcomes(CO),Program Outcomes(PO) and CO-PO Mapping	-	-
	CONTENT DELIVERY (THEORY)		
lecture No.	Topics to be covered	Course Out- comes	Reference
1.	Definition of Embedded System,	CO1	R2:1.1
2.	Embedded Systems Vs General Computing Systems	CO1	R2:1.2
3.	History of Embedded Systems	CO1	R2:1.3
4.	Classification of embedded systems	CO1	R2:1.4
5.	Major Application Areas and Purpose of Embedded Systems	CO1	R2: 1.5,1.6
6.	Characteristics and Quality Attributes of Embedded Systems	CO1	R2:3.1
7.	Core of the Embedded System: General Purpose and Domain Specific Processors	CO2	R2:2.1
8.	ASICs	CO2	R2:2.1.2
9.	PLDs	CO2	R2:2.1.3
10.	Commercial Off-The-Shelf Components (COTS)	CO2	R2:2.1.4
11.	Memory: ROM, RAM	CO2	R2:2.2
12.	Memory according to the type of Interface	CO2	R2: 2.2.3
13.	Memory Shadowing	CO2	R2:2.2.4
14.	Memory selection for Embedded Systems	CO2	R2:2.2.5
15.	Sensors and Actuators	CO2	R2:2.3
16.	Communication Interface:	CO2	R2:2.4
17.	Onboard and External Communication Interfaces.	CO2	R2:2.4.1
18.	Reset Circuit	CO3	R2:2.6.1
19.	Brown-out Protection Circuit	CO3	R2:2.6.2
20.	Oscillator Unit, Real Time Clock	CO3	R2:2.6.3
21.	Watchdog Timer	CO3	R2:2.6.4
22.	Embedded Firmware Design Approaches	CO4	R2:9.1
23.	Embedded Firmware Development Languages	CO4	R2:9.2
24.	Operating System Basics	CO5	R2:10.1
25.	Types of Operating Systems	CO5	R2:10.2

Tasks	CO5	R2:10.3				
Process	CO5	R2:10.3				
Threads	CO5	R2:10.3				
Multiprocessing	CO5	R2:10.4				
Multitasking	CO5	R2:10.4				
Task Scheduling	CO5	R2:10.5				
Shared Memory concept	CO6	R2:10.7				
Message Passing	CO6	R2:10.7				
Remote Procedure Call and Sockets	CO6	R2:10.7				
Task Synchronization	CO6	R2:10.8				
Task Communication Issues	CO6	R2:10.7				
Task Synchronization Issues	CO6	R2:10.8				
Task Synchronization Techniques	CO6	R2:10.8				
Task Synchronization Techniques Semaphores	CO6	R2:10.8				
Device Drivers	CO6	R2:10.9				
How to Choose an RTOS.	CO6	R2:10.10				
DISCUSSION OF QUESTION BANK						
Introduction to Embedded Systems	CO1	R2:1.1				
Typical Embedded System	CO2	R2:2.1				
Embedded Firmware	CO3,4	R2:2.6,9.1				
RTOS based Embedded System Design	CO 5	R2:10.1				
Task Communication	CO6	R2: 10.7				
	ProcessThreadsMultiprocessingMultitaskingTask SchedulingTask SchedulingShared Memory conceptMessage PassingRemote Procedure Call and SocketsTask SynchronizationTask Synchronization IssuesTask Synchronization IssuesTask Synchronization TechniquesTask Synchronization TechniquesDevice DriversHow to Choose an RTOS.DISCUSSION OF QUESTION BANKIntroduction to Embedded SystemsTypical Embedded SystemEmbedded FirmwareRTOS based Embedded System Design	ProcessCO5ThreadsCO5MultiprocessingCO5MultitaskingCO5Task SchedulingCO5Shared Memory conceptCO6Memory conceptCO6Memore Procedure Call and SocketsCO6Task SynchronizationCO6Task Synchronization IssuesCO6Task Synchronization TechniquesCO6Task Synchronization Techniques SemaphoresCO6Device DriversCO6How to Choose an RTOS.CO6DISCUSSION OF QUESTION BANKCO1Typical Embedded SystemCO2Embedded FirmwareCO3,4RTOS based Embedded System DesignCO 5				

Signature of Course Coordinator

HOD,ECE

ANNEXURE - I

KEY ATTRIBUTES FOR ASSESSING PROGRAM OUTCOMES

PO Number	NBA Statement / Key Competencies Features (KCF)	No. of KCF's
PO 1	 Independently carry out research / investigation and development work to solve practical problems. 1. Independence 2. Self driven 3. Quality of work 4. Problem identification and implementation 5. Demonstrate the solutions 6. Budget 	6
PO 2	 Write and present a substantial technical report / document. 1. Demonstrate and communicate effectively in writing report and document/ present orally. 2. Clarity (writing/ presentation) 3. Grammar/ punctuation (writing) 4. References 5. Speaking/ Presenting 6. Subject knowledge while preparing report 	6
PO 3	 Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program. 1. Knowledge, understanding and demonstrations of embedded applications in real time scenario. 2. Ability to demonstrate and communicate effectively in writing / orally societal problems. 3. Analyze and design innovative products 4. Problem formulation and abstraction 5. Use creativity to establish innovative solutions 6. Experimental design 7. Manage the design process and evaluate outcomes using modern tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 	9

PO 4	 Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications. 1. Understand the need of users with the importance of considerations such as IoT and Robotics 2. Scientific principles and methodology 3. Problem formulation and abstraction 4. Use creativity to establish innovative solutions 5. Experimental design 6. Manage the design process and evaluate outcomes 7. Computer software / simulation packages / diagnostic equipment / technical library resources / literature search tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 10. Under take research and development projects in the field of Embedded Systems 	10
PO 5	 Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team. Maturity – requiring only the achievement of goals to drive their performance Self-direction (take a vaguely defined problem and systematically work to resolution) Individual performance is used during the classroom periods, in the hands-on labs, and in the design projects. Knowledge of management techniques which may be used achieve engineering objectives Meeting deadlines and producing solutions Work with all level of people in the team. Demonstrate ability to work well with a team 	7
PO 6	 Recognize the need to engage in lifelong learning through continuing education and research. Project management and research orientation/ Ph.D Strengthen in embedded and advanced engineering areas Continuing education efforts through literature and courses Personal development Plan tasks and resources, manage risk and produce deliverables Meeting deadlines and producing solutions Work with all levels of people in team Demonstrated ability to work well with a team 	8



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043

COURSE DESCRIPTION

Department	Electronics	Electronics and Communication Engineering			
Course Title	Microcontr	Microcontrollers and Programmable Digital Signal Processing			
Course Code	BESB02	BESB02			
Program	M.Tech-Emb	M.Tech-Embedded Systems			
Semester	Ι	Ι			
Course Type	Core	Core			
Regulation	R18				
		Theory		Prae	ctical
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits
	3	-	3	-	-
Course Coordinator	Dr. S China Venkateswarlu, Professor				

I COURSE OVERVIEW:

This course is intended to provide fundamentals of ARM Cortex-M3 Processor and LPC 17XX Microcontroller architectures and their features. It includes the architectures of the Cortex-M3, instruction set summary, Programmable DSP processor. It is used in the applications of microcontrollers programming models and programmable digital signal processors.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	
B.Tech	-	- Digital Signal Processing		
B.Tech	-	-	Microprocessors and Microcontrollers	

III MARKS DISTRIBUTION:

Subject	SEE	CIE	Total Marks
	Examination	Examination	
Microcontrollers and	70 Marks	30 Marks	100
Programmable Digital Signal			
Processing			

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Power Point	\checkmark	Chalk & Talk	х	Assignments	x	MOOC
	Presentations						
x	Open Ended	\checkmark	Seminars	x	Mini Project	x	Videos
	Experiments						
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
20%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Technical Seminar	100ai Marks
	and Term Pap		
CIA Marks	CIA Marks 25		30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

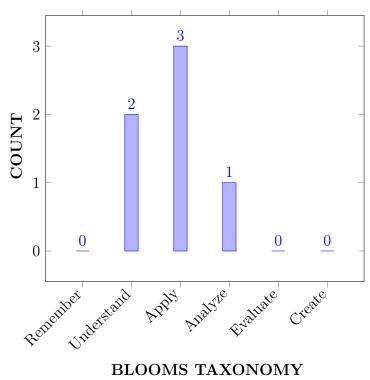
Ι	The programming models of ARM processors core-based System on Chip with several features / peripherals based on requirements of embedded applications.
II	The architectural view of various Programmable DSP Processors
III	The design and development of embedded applications by utilizing the ARM processor core and DSP processor-based platform.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Illustrate the Internal architecture and memory operations of	Understand
	ARM Cortex M3 processor for interfacing microprocessor	
	applications	
CO 2	Analyze Exceptions handler mechanism to minimize interrupt	Analyze
	latency using Nested Vectored Interrupt Controller	
CO 3	Construct the high level of integration in embedded	Apply
	applications using LPC 17XX Microcontroller	
CO 4	Demonstrate various computational building blocks of	Understand
	programmable DSP architectures using interfacing of memory and	
	I/O peripherals	
CO 5	Identify the CPU architecture, peripherals, and development	Apply
	tools for the TMS320C6000 digital signal processors	
CO 6	Develop the application for digital signal processing using code	Apply
	composer studio tool	

COURSE KNOWLEDGE COMPETENCY LEVEL



VIII PROGRAM OUTCOMES:

_

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to
	solve practical problems.
PO 2	Write and present a substantial technical report / document
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the
	program. The mastery should be at a level of higher than the requirements in
	the appropriate bachelor program
PO 4	Apply the skills and knowledge needed to serve as a professional engineer
	skilful at designing embedded systems for effective use in communications,
	IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively,
	creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in lifelong learning through continuing
	education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	2	CIE/SEE/AAT
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program	2	CIE/SEE/AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	3	CIE/SEE/AAT

X MAPPING OF EACH CO WITH PO(s), PSO(s):

COURSE		PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6		
CO1	\checkmark	-	\checkmark	\checkmark	-	-		
CO2	\checkmark	-	-	-	-	-		
CO3	\checkmark	-	\checkmark	\checkmark	-	-		
CO4	\checkmark	-	-	\checkmark	-	-		
CO5	\checkmark	-	-	\checkmark	-	-		
CO6	\checkmark	-	\checkmark	\checkmark	_	-		

XI JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING -DIRECT:

Course Out- comes	PO'S	Justification for mapping (Students will be able to)	No. of Key com- petencies matched.
CO1	PO 1	Understand the concepts of ARM Cortex-M3 processor by applying Scientific principles and methodology , Use creativity to establish architecture , identify Problem formulation for interfacing problems , Implement different applications by using arm processor.	6
	PO 3	Analyze the given problem statement and formulate the kernel, and other components in embedded systems and use creativity to establish innovative solutions for embedded system , Interpret the result on various applications	4
	PO 4	Develop ARM Cortex-M3 processor for various Problems in pre processors , implement advanced arm processor for real time applications	3
CO2	PO 4	Illustrate the concepts (knowledge) of task scheduling types for Soft real-time operating system and Hard Real-Time operating systems by using mathematics, science, engineering fundamentals to the solution of complex engineering problems	6
CO3	PO 1	Illustrate components of real time operating systems (knowledge) to integrate the software and hardware components (mathematical model) the design of reliable embedded system by applying the principles of mathematical model and science	5
	PO 3	Construct the high level of integration in embedded applications using LPC 17XX Microcontroller	4
	PO 4	Independently carry out research / investigation and development work to solve practical problems.	3
CO4	PO 1	Analyze (problem statement) finite state machine by applying solutions for complex engineering problems and design system components.	6
CO5	PO 1	Create (Engineering knowledge) semaphore token for the execution of one or more threads in mutual exclusion by applying the principles of mathematics, science.	5
	PO 4	Identify the given problem statement and solve it using synchronization or mutual exclusion by applying mathematical properties.	3
CO6	PO 1	Understand (knowledge) asynchronous communications protocol in operating systems by applying its mathematical properties.	6

PO 3	Analyze the given problem statement and formulate the kernel, and other components in embedded systems and use creativity to establish innovative solutions for embedded system , Interpret the result on various applications	4
PO 4	Understand (knowledge) asynchronous communications protocol in operating systems by applying its mathematical properties.	3

Note: For Key Attributes refer Annexure - I

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAP-PING:

COURSE		PROGRAM OUTCOMES								
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6				
	10	7	9	6	6	8				
CO 1	3	-	4	6	-	-				
CO 2	-	-	-	6	-	-				
CO 3	3	-	4	5	-	-				
CO 4	-	-	-	6	-	-				
CO 5	3	-	-	5	-	-				
CO 6	3	-	4	5	-	-				

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO, PSO):

COURSE		PROGRAM OUTCOMES							
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6			
	10	7	9	6	6	8			
CO 1	50	-	44.4	60	-	-			
CO 2	-	-	-	60	-	-			
CO 3	50	-	44.4	50	-	-			
CO 4	-	-	-	60	-	-			
CO 5	50	-	-	50	-	-			
CO 6	50	-	44.4	50	-	-			

XIV COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

- $\boldsymbol{0}$ $0 \leq C \leq 5\%$ No correlation
- ${\it 1}$ -5 <C ≤ 40% – Low/ Slight
- $\pmb{\mathcal{2}}$ 40 % < C < 60% – Moderate
- $\boldsymbol{3}$ $60\% \leq C < 100\%$ Substantial /High

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO 1	2	-	2	3	-	-	
CO 2	-	-	-	3	-	-	
CO 3	2	-	2	2	-	-	
CO 4	-	-	-	3	-	-	
CO 5	2	-	-	2	-	-	
CO 6	2	-	2	2	-	-	
TOTAL	8	-	6	15	-	-	
AVERAGE	2	-	2	2.5	-	-	

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	-
Quiz	z - Tecl		-	Certification	-
Term Paper \checkmark		Seminars \checkmark		Student Viva	-
Laboratory Practices	•		-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XVI ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	\checkmark	End Semester OBE Feedback
-	Assessment of activities / Modeling a	and E	xperimental Tools in Engineering by Experts

XVII SYLLABUS:

MODULE I	ARM CORTEX-M3 PROCESSOR		
	ARM Cortex-M3 processor: Applications, Programming model – Registers,		
	Operation modes, Exceptions and Interrupts, Reset Sequence Instruction		
Set, Unified Assembler Language, Memory Maps, Memory			
	AccessAttributes, Permissions, Bit-Band Operations, Unaligned and		
	ExclusiveTransfers, Pipeline, Bus Interfaces		
MODULE II	EXCEPTIONS AND INTERRUPT		
	Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending		
	behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested		
	Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer,		
	Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency		
MODULE III	LPC 17XX MICROCONTROLLER		
	LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC.		
	UART and other serial interfaces, PWM, RTC, WDT.		
MODULE IV	PROGRAMMABLE DSP (P-DSP) PROCESSORS		

	Programmable DSP (P-DSP) Processors: Harvard architecture, Multiport memory, architectural structure of PDSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.
MODULE V	VLIW ARCHITECTURE
	VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations code composer Studio for application development for digital signal processing, on chip peripherals, processor benchmarking.

TEXTBOOKS

- 1. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3", Elsevier, 3rd Edition, 2014.
- 2. Venkatramani B, Bhaskar M, —Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition, 2011.

REFERENCE BOOKS:

- 1. Sloss Andrew N, Symes Dominic, Wright Chris, —"ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publications
- 2. Steve furber, —"ARMSystem-on-ChipArchitecture", Pearson Education.
- 3. Frank Vahid and Tony Givargis, —"Embedded System Design", Wiley Publications

COURSE WEB PAGE:

1. https://www.iare.ac.in/?q=courses/electronics-and-communication-engineeringautonomous/Microcontrollers and Programmable Digital Signal Processing

XVIII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
	OBE DISCUSSION		
1	Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Outcomes (PO) and CO - PO Mapping	-	https://lms. iare.ac.in/ index?route= course/ details& course_id= 354
	CONTENT DELIVERY (THEO	\mathbf{RY})	
2	Understanding the ARM Cortex-M3 processor: Applications, Programming model.	CO 1	T1: 1.1-1.5
3	Registers Operation modes	CO 1	T1: 3.2-3.5
4	Exceptions and Interrupt, Reset Sequence	CO 1	T1: 3.5-3.7
5	Study the Instruction Set	CO 1	T1: 4.1-4.2

0		00.1	T 1 4 2 4 2
6	Unified Assembler Language	CO 1	T1: 4.2-4.3
7	Memory Maps	CO 1	T1: 4.3-4.4
8	Memory Access Attributes	CO 1	T1:5.1-5.2
9	Permissions, Bit-Band Operations	CO 1	T1:5.2,5.5
10	Discuss the unaligned and exclusive transfers.	CO 1	T1: 6.1-6.2
11	Pipeline, Bus Interfaces.	CO 1	T1: 6.1-6.2
12	Examine the various Exceptions, Types	CO 2	T1: 7.1-7.2
13	Priority, Vector Tables	CO 2	T1: 7.1-7.2
14	Interrupt Inputs and Pending behavior,	CO 2	T1: 7.4-7.5
15	Fault Exceptions	CO 2	T1: 7.4-7.5
16	Discuss the Supervisor and Pendable Service Call,	CO 2	T2: 7.6-8.1
17	Nested Vectored Interrupt Controller.	CO 2	T2: 7.6-8.1
18	Understand the Basic Configuration, SYSTICK Timer	CO 2	T1: 8.2-8.5
19	Interrupt Sequences, Exits	CO 2	T1:9.1-9.2
20	Tail Chaining, Interrupt Latency.	CO 2	T1: 9.1-9.2
21	Describe the LPC 17xx microcontroller- Internal memory,	CO 3	R2:8.4,8.10
22	General purpose input and output(GPIOs)	CO 3	R2:8.4-10
23	Working of Timers	CO 3	R2:8.4
24	Study the features of ADC,	CO 3	R2: 8.14-8.16
25	Universal asynchronous receiving and transmission(UART)	CO 3	R2: 8.14-8.16
26	Other serial interfaces	CO 3	R2: 8.16,8.17
27	Understand the concepts of PWM,	CO 3	R2:8.22
28	Real time clock	CO 3	R2:8. 27
29	Watch dog timers	CO 3	R2:8. 28
30	Describe the Programmable DSP (P-DSP) Processors	CO 4	T2: 2.1-2.2
31	Harvard architecture model	CO 4	T2:2.2-2.4
32	Multi port memory organization	CO 4	T2: 2.1-2.4
33	Study the features of architectural structure of P-DSP- MAC unit	CO 4	T2:3.1-2.1
34	Barrel shifters with examples	CO 4	T2: 2.5
35	Understand the Introduction to TI DSP processor family.	CO 4	T2: 2.5
36	Study the VLIW architecture	CO 4	T2: 2.5,13.4
37	TMS320C6000 series architecture study,	CO 4	T2: 2.5,13.4
38	TMS320C6000 family architecture study,	CO 5	T2: 2.5-2.6
39	Understand data paths	CO 5	T2: 13.3
40	Crosses paths interfacing	CO 5	T2:13.6-13.5

41	Introduction to Instruction level architecture of C6000 family.	CO 5	T2: 13.3-13.4
42	Assembly Instructions memory addressing	CO 6	T2: 13.5
43	Arithmetic, logical operations.	CO 6	T2:13.6
44	Code Composer Studio for application development for DSP	CO 6	T2:13.11-12
45	Understand on chip peripherals.	CO 6	T2:13.11-12
46	Processor benchmarking	CO 6	T2:13.12-14
	PROBLEM SOLVING/ CASE ST	UDIES	
47	Problems on registers, operation modes	CO 1	T1: 1.1-1.5
48	Problems on memory maps, memory access attributes	CO 1	T1: 3.2-3.5
49	Problems on priority, vector tables	CO 2	T1: 7.1-7.2
50	Problems on interrupt sequences, interrupt latency.	CO 2	T1: 7.1-7.2
51	Problems on LPC 17xx microcontroller- internal memory	CO 3	R2:8.4,8.10
52	Problems on , PWM, RTC	CO 3	R2:8.4 - 10
53	Problems on barrel shifters	CO 4	T2: 2.1-2.4
54	Problems on data paths, cross paths	CO 5	T2: 2.5-2.6
55	Problems on arithmetic, logical operations	CO 6	T2:13.11-12
56	Systems ARM cortex-m3 processor	CO 1	T1: 1.1-1.5
57	Exceptions and interrupts	CO 2	T1: 7.1-7.2
58	LPC 17xx microcontroller	CO 3	R2:8.4-10
59	Programmable DSP processors	CO 4	T2: 2.1-2.4
60	VLIW architecture	CO 5	T2: 2.5-2.6
	DISCUSSION ON QUESTION B	ANK	
61	Systems ARM cortex-m3 processor	CO 1	T1: 1.1-1.5
62	Exceptions and interrupts	CO 2	T1: 7.1-7.2
63	LPC 17xx microcontroller	CO 3	R2:8.4-10
64	Programmable DSP processors	CO 4	T2: 2.1-2.4
65	VLIW architecture	CO 5	T2: 2.5-2.6

Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 ELECTRONICS AND COMMUNICATIONENGINEERING COURSE DESCRIPTION

Course Title	WIRELESS	WIRELESS LANS AND PANS						
Course Code	BESB03	BESB03						
Program	M.Tech	M.Tech						
Semester	I	I ES						
Course Type	CORE	CORE						
Regulation	R18							
		Theory		Prac	tical			
Course Structure	Course Structure Lecture Tutorials Credits Laboratory Credits							
3 - 3								
Course Coordinator	Mr. N Papa I	Rao, Assistant I	Professor					

I COURSE OVERVIEW:

This course intended to provide wireless network communication over short distances using radio or infrared signals instead of traditional network cabling. The basic knowledge of the wireless system, IEEE standards, network architecture, and its protocols. It focuses on data transmission among devices such as computers, smartphones, tablets, and personal digital assistants.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	-	-	Analog Communications
B.Tech	-	-	Digital Communications

III MARKS DISTRIBUTION:

${f Subject}$	SEE Examination	CIE Examination	Total Marks
Wireless Lans and pans	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✓	Power Point Presentations	√	Chalk & Talk	x	Assignments	x	MOOC
x	Open Ended Experiments	√	Seminars	x	Mini Project	x	Videos
x	Others		-				

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
20%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	TI	neory	Total Marks	
Type of Assessment	CIE Exam	Technical Seminar and Term Paper	10tai Marks	
CIA Marks	25	5	30	

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

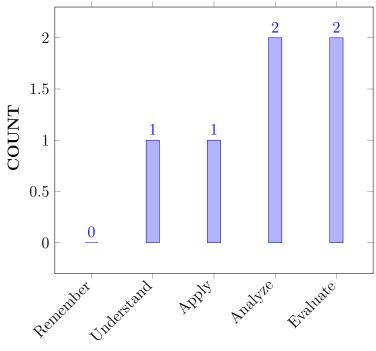
VI COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Recall the generations of cellular systems for understanding the	Understand
	connectivity of wireless communication networks.	
CO 2	Organize the random-access protocols to decrease collision and	Apply
	avoid crosstalk.	

CO 3	Justify the importance of wireless LANs for connecting different	Evaluate
	devices through wireless communication to form an area network.	
CO 4	Estimate the wireless PANs for interconnecting electronic	Evaluate
	devices within an individual person's workspace.	
CO 5	Analyze the traffic engineering used to carry traffic flows that	Analyze
	vary from those chosen automatically by the routing protocol.	
CO 6	Interpret the wireless networking standards and protocols for	Analyze
	wireless transmission approved by IEEE.	

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VII HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency
			Assessed by
PO 1	Independently carry out research / investigation	3	CIE/Quiz/AAT
	and development work to solve practical		
	problems.		
PO 2	Write and present a substantial technical report	2	CIE/Quiz/AAT
	/ document.		
PO 3	Demonstrate a degree of mastery over the area	2	CIE/Quiz/AAT
	as per the specialization of the program. The		
	mastery should be at a level of higher than the		
	requirements in the appropriate bachelor		
	program		

PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	2	CIE/Quiz/AAT
PO 6	Recognize the need to engage in lifelong learning through continuing education and research.	2	CIE/Quiz/AAT

 $\mathbf{3} = \mathbf{High}; \, \mathbf{2} = \mathbf{Medium}; \, \mathbf{1} = \mathbf{Low}$

VIII MAPPING OF EACH CO WITH PO(s):

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO 1	\checkmark	-	\checkmark	1	-	-	
CO 2	\checkmark	\checkmark	-	-	-	✓	
CO 3	\checkmark	\checkmark	-	✓	-	-	
CO 4	\checkmark	\checkmark	-	-	-	-	
CO 5	\checkmark	-	-	✓	-	-	
CO 6	\checkmark	-	1	-	-	-	

IX JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING -DIRECT:

COURSE OUTCOMES	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key Competencies
CO 1	PO1	Understand and Analyze First and Second Generation Cellular Systems with architectures. science to engineering problems.	1
	PO3	Knowledge, understanding and demonstrations of embedded applications in real time scenario. science to engineering problems.	4
CO 2	PO1	Understand the concept of Cellular Communications from 1G to 3G (knowledge) of architectures of AMPs, GSM and GPRS. considering design parameters.	2
	PO2	Understand the concept of Cellular Communications from 1G to 3G by(Reference) of Random access protocals considering design parameters.	2
	PO4	Explain Wireless 4G systems and Wireless Spectrum of 4G (knowledge) with increased bandwidth and speed. principles of mathematics and science for solving complex engineering problems.	4
CO3	PO2	Understand the radio wave propagation and formulate to the propagation mechanisms using principles of mathematics and engineering science.	3

	PO4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications formulate to the propagation mechanisms using principles of mathematics and engineering science.	3
CO 4	PO1	Distinguish Random Access Methods of Pure ALOHA and Slotted ALOHA analyzing complex engineering problems using the principles of mathematics, engineering science.	2
	PO2	Understand the channel path loss models problem statement and finding the solution implementation of fading operations by analyzing complex engineering problems	2
	PO6	Identify parameters of mobile multipath channels forsolvingcomplex engineeringproblemsgenerates by applyingmathematics, scienceandengineering fundamentals by life long study.	3
CO5	PO1	Outline (Knowledge) WLAN Topologies of infrastructure and adhoc mode of operations. applying mathematics, science for engineering problems.	2
CO 6	PO1	Analyze (Understand) the various wireless local area networks by applying solutions of complex engineering problems.	2
	PO2	Understand the data transfercharacteristics of architecture for problem formulation to determine modern processors and memories using mathematics principles.	1
	PO5	Understand the concept of modern wireless local area networks for high throughput networks process using complex engineering activities.	5

X TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO) MAPPING:

COURSE	Program Outcomes/ No. of Key Competencies Matched					
OUTCOMES	1	2	3	4	5	6
CO 1	1	-	1	2	-	-
CO 2	2	3	-	-	-	2
CO 3	2	2	-	2	-	-
CO 4	2	1	-	-	-	-
CO 5	3	-	-	2	-	-
CO 6	1	-	2	-	-	-

XI PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO):

COURSE		PROGRAM OUTCOMES						
OUTCOMES	1	2	3	4	5	6		
CO 1	16.7	-	33.3	50	-	-		
CO 2	33.3	33.3	-	-	-	50		
CO 3	50	50	-	50	-			
CO 4	33.3	33.3	-	-	-	-		
CO 5	33.3	-	-	50	-	-		
CO 6	33.3	-	50	-	-	-		

XII COURSE ARTICULATION MATRIX (PO mapping):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

- $\boldsymbol{\theta}$ $0 \le C \le 5\%$ No correlation
- $\pmb{2}$ 40 % < C < 60% – Moderate
- $1-5 < C \le 40\% Low/Slight$
- $\boldsymbol{3}$ 60% \leq C < 100% Substantial /High

COURSE		PROGRAM OUTCOMES						
OUTCOMES	1	2	3	4	5	6		
CO 1	1	-	1	2-	-	-		
CO 2	2	-	-	-	-	2		
CO 3	2	3	-	2	-	-		
CO 4	2	2	-	-	-	-		
CO 5	3	1	-	2	-	-		
CO 6	1	-	2	-	-	-		
TOTAL	11	6	3	6	-	2		
AVERAGE	1.8	2	1.5	2	-	2		

XIII ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	PO 1,PO 2,PO5	SEE Exams	PO 1,PO 2,PO6	Seminars	PO 1
Laboratory Practices	-	Student Viva	-	Certification	-
Term Paper	PO 1,PO 2, PO 5	5 Minutes Video		Open Ended Experiments	-
Assignments					

XIV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	_
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	\checkmark	Seminars	\checkmark	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XV SYLLABUS:

MODULE I	WIRELES SYSTEM and RANDOM-ACCESS PROTOCOLS
	Introduction, frequency reuse, channel assignment strategies, handoff strategies; Prioritizing handoffs, practical handoff considerations, interference and system capacity; Co-channel interference and system capacity, channel planning for wireless systems, adjacent channel interference, power control for reducing interference, trunking and grade of service, improving coverage and capacity in cellular systems; Cellsplitting, sectoring.
MODULE II	WIRELESS LANS
	Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology.
MODULE III	THE IEEE802.11 STANDARD FOR WIRELESS LANS
	Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE802.11eMACprotocol.
MODULE IV	WIRELESS PANS
	Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatter net formation.
MODULE V	THE IEEE802.15 WORKING GROUP FOR WPANS
	The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra-wideband.

TEXTBOOKS

1. 1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.

- 2. 2. Wireless Communications and Networking-VijayK.Garg, Morgan Kaufmann Publishers,2009.
- 3. KavehPahlvan, Prashant Krishnamurthy, "Principle of wireless networks", A United Approach^{||}, Pearson Education, 2004.
- 4. Andrea Goldsmith, "Wireless Communications", Cambridge University Press, 2005.

REFERENCE BOOKS:

- 1. 1. Wireless Networks Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.
- 2. 2. Wireless Communication-Marks Ciampor, Jeorge Olenewa, Cengage Learning, 2007.
- 3. Mark Ciampa Jorge Olenewa, "wireless communication and Networking", IE, 2009.
- 4. X.Wang, H.V.Poor ,Wireless communication system, Pearson Education, 2004.
- 5. JochenSchiller," Mobile Communication", Pearson Education, 2nd Edition, 2003.

XVI COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference T1: 4.1
1	Understand and analyze first and second generation cellular systems.	CO 1	T1-5.1- 5.2
2	Cellular communications from 1G to3G.	CO 1	T1-5.1- 5.2
3	Wireless 4G systems.	CO 1	T1-5.1- 5.2
4	The wireless Spectrum.	CO 2	T1-5.2
5	Analyze Cellular Communications from 1G to 3G.	CO 2	T1-5.1
6	Random Access Methods	CO 2	T1-6.1
7	Pure ALOHA	CO 3	T1-6.2
8	Slotted ALOHA,	CO 2	T1-6.3
9	Carrier Sense Multiple Access (CSMA).	CO 3	T1-6.2
10	Carrier Sense Multiple Access with Collision Detection.	CO 3	T1-6.4
11	Carrier Sense Multiple Access with Collision Avoidance.	CO 3	T1-6.4
12	Explain Wireless 4G systems, The Wireless Spectrum.	CO 4	T1-6.4
13	importance of Wireless LANs.	CO 4	T1-6.5
14	WLAN Topologies.	CO 4	T1-6.4
15	Transmission Techniques: Wireless Networks.	CO 4	T6.4
16	Transmission Techniques: Wired Networks.	CO 4	T1-6.5
17	Log-distance path loss model, Ericsson Multiple Break point Model, Attenuation Factor Model.	CO 4	T1-7.1.1
18	Describe Carrier Sense Multiple Access (CSMA).	CO 5	T1-7.1.1

19	comparison of wired and Wireless LANs.	CO 5	T1- .7.1,7.2
20	Carrier Sense Multiple Access with Collision Detection (CSMA/CD).	CO 5	T1-7.2
21	Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).	CO 5	T1-7.3
22	WLAN Technologies: Infrared technology.	CO 6	T1-7.2
23	UHF narrowband technology.	CO 6	T1- 7.3,7.4
24	Coherence Bandwidth, Doppler Spread and Coherence Time.	CO 6	T1-7.4
25	Explain WLAN Topologies and analyze transmission techniques.	CO 6	T1-6.12
26	Spread Spectrum technology,	CO 6	T1-9.4
27	Network Architecture.	CO 6	T1-9.6
28	Physical layer, The Medium access control layer.	CO 6	T1-4.2
29	Describe importance of Wireless Local Area Networks.	CO 6	T1-5.11
30	MAC Layer issues.	CO 4	T1-
			7.1,7.2
31	Hidden terminal problem.	CO 3	T1- 7.3,7.4
32	Reliability, Collision avoidance.	CO 4	T1- 7.6,7.7
33	congestion avoidance.	CO 5	T1-7.7.2
34	Congestion control.	CO 4	T1-7.8
35	Explain Network architecture and analyze MAC layer issues.	CO 5	T1- 8.1,8.2
36	Security.	CO 5	T1-8.2
37	The IEEE 802.11e MAC protocol.	CO3	T1-8.5
38	The IEEE 802.11e MAC protocol. Introduction,	CO 4	T1-8.6
39	importance of wireless PANs,	CO4	T1 8.5
40	Describe importance of Wireless Private Area Networks.	CO 6	T1-8.9.
41	Technical overview, the Bluetooth specifications	CO 6	R1 7.2
42	WLAN topologies, WLAN standard IEEE 802.11	CO 5	R1 7.1
43	QoS and Dynamics Slot Assignment, Scatter net formation., The IEEE 802.15.3, The IEEE 802.15.4, ZigBee components and network topologies.	CO6	R3-7.1
44	Comparison of IEEE 802.11 a,b,g and n standards	CO6	R1:7.3
45	IEEE 802.15.4 and its enhancements, Wireless PANs device, architecture, physical layer, data link layer, the network layer, applications, IEEE 802.15.3a ultra wideband, Hipper LAN, WLL.	CO5	R1:7.4

Signature of Course Coordinator



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 COURSE DESCRIPTION

Branch	Electronics	Electronics and Communication Engineering				
Course Title	Principles of	of Distributed	d Embedded	Systems		
Course Code	BESB06					
Program	M.Tech-Emb	edded Systems				
Semester	Ι	Ι				
Course Type	Professional 1	Elective-II				
Regulation	R18					
		Theory		Prac	etical	
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits	
	3	0	3	-	-	
Course Coordinator	Ms. G Ajitha	Ms. G Ajitha, Assistant Professor				

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	-	-	EMBEDDED SYSTEMS

II COURSE OVERVIEW:

A distributed embedded system consists of hardware and software parts interacting via an interconnection network. This course deals with the importance of real time communication systems, classification of real time systems, real time operating systems, and the design of real-time protocols. The applications include mobiles, routers, video games consoles, mp3 players, printers, GPS receivers, dishwashers, thermostats, anti-lock banking systems, medical imaging etc.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Principles of Distributed Embedded Systems	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	PowerPoint Presentation	\checkmark	Chalk & Talk	\checkmark	Assignments	x	MOOC
x	Seminars	\checkmark	Others				

V EVALUATION METHODOLOGY:

Each theory course will be evaluated for a total of 100 marks, out of which 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE).Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The

syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

50 %	To test the objectiveness of the concept
30 %	To test the analytical skill of the concept
20 %	To test the application skill of the concept

The emphasis on the questions is broadly based on the following criteria:

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Technical Seminar and Term Paper	10tal Marks
CIA Marks	25	05	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

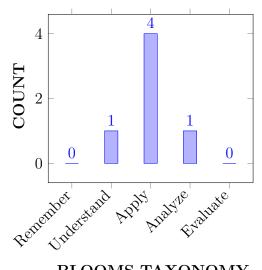
The students will try to learn:

Ι	The concepts of embedded computing, RTOS (Real Time Operating System) and embedded software tools for implementing embedded systems.
II	The design principles of distributed embedded systems.
III	CAN (Control Area Network) based systems to move into different embedded applications.

VII COURSE OUTCOMES: After successful completion of the course, students should be able to:

CO 1	Summarize the concepts of real time systems for real time embedded applications	Understand
CO 2	Build time constrained embedded systems using the concepts of RTOS (Real Time Operating System) for rapid design and programming embedded systems	Apply
CO 3	Construct the time constrained application as a member of a small group to meet design specifications	Apply
CO 4	Identify the working of CAN (Control Area Network) standard protocol to execute real time applications.	Apply
CO 5	Explore the fundamentals of CAN (Control Area Network) standards and its configuration files, service data objectives for preparing different electronic data sheets	Analyze
CO 6	Make use of the CAN (Control Area Network) open standards and design parameters for assuring quality of service and internet working in various internet protocols.	Apply

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes				
PO 1	Independently carry out research / investigation and development work to solve practical problems.				
PO 2	Write and present a substantial technical report / document.				
PO 3	Demonstrate a degree mastery over the area as per the area of specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.				

	Program Outcomes
PO 4	Apply the skills and knowledge needed to serve as a professional engineer
	skilful at designing embedded systems for effective use in communications,
	IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively,
	creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in lifelong learning through continuing
	education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 3	Demonstrate a degree mastery over the area as per the area of specialization of the program.The mastery should be at a level of higher than the requirements in the appropriate bachelor program.	3	SEE / CIE / AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	3	SEE / CIE / AAT

X MAPPING OF EACH CO WITH PO(s):

COURSE	PROGRAM OUTCOMES			ЛES		
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	-	-	\checkmark	\checkmark	-	-
CO 2	-	-	\checkmark	\checkmark	-	-
CO 3	-	-	\checkmark	\checkmark	-	-
CO 4	-	-	\checkmark	\checkmark	-	-
CO 5	-	-	\checkmark	\checkmark	-	-
CO 6	-	-	\checkmark	\checkmark	-	-

XI JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT :

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	Demonstrate and Analyze the complex engineering problems to embedded real time systems for real time embedded applications and their system components of solution development	3
	PO 4	Illustrate the concepts (knowledge) of embedded real time systems for real time embedded applications by using engineering fundamentals to the solution of problem formulation and abstraction to establish innovative solutions	3

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO2	PO 3	Apply the complex engineering problems and their system components to time constrained RTOS (Real Time Operating System) using the concepts of for rapid design and programming embedded systems for solution development	3
	PO 4	Build time constrained embedded systems using the concepts of engineering fundamentals to the solution of problem formulation and abstraction to establish innovative solutions using RTOS (Real Time Operating System) rapid design and its programming	3
CO 3	PO 3	Mange the design process and evaluation outcomes for the time constrained application as a member of a small group to meet design specifications by using engineering sciences to the solution of problem formulation and abstraction to establish innovative solutions	3
	PO 4	Experimental Design the time constrained application as a member of a small group to meet design specifications by using engineering fundamentals to problem formulation and abstraction to establish innovative solutions .	3
CO4	PO 3	Identify the problem formulation and abstraction of CAN (Control Area Network) standard protocol to execute real time applications using engineering problems solution development and implementation in various applications.	3
	PO 4	Apply the principles and methodology of CAN (Control Area Network) standard protocol to execute engineering fundamentals to problem formulation and abstraction to establish innovative solutions in IoT applications.	3
CO5	PO 3	Demonstrate problem formulation and abstraction to CAN (Control Area Network) standards and its configuration files manage the design processfor preparing different electronic data sheets to the solution development of IoT applications.	3
	PO 4	Apply the knowledge of imporatnce of considerations with the principles of CAN (Control Area Network) standards for implementation of the solutions preparing different electronic data sheets.	3

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO 6	PO 3	Demonstrate problem formulation and abstraction to CAN (Control Area Network) standards and its configuration files manage the design processfor preparing different electronic data sheets to the solution development of IoT applications.	3
	PO 4	Illustrate the needs of importance concepts of CAN (Control Area Network) standards and its configuration files manage the design process for preparing different electronic data sheets to the solution development of IoT applications.	3

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – PO MAPPING:

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	6	6	9	10	7	8
CO 1	-	-	3	3	-	-
CO 2	-	-	3	3	-	-
CO 3	-	-	3	3	-	-
CO 4	-	-	3	3	-	-
CO 5	-	-	3	3	-	-
CO 6	-	-	3	3	-	-

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO:

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
	6	6	9	10	7	8	
CO 1	-	-	30	33.3	-	-	
CO 2	-	-	30	33.3	-	-	
CO 3	-	-	30	33.3	-	-	
CO 4	-	-	30	33.3	-	-	
CO 5	-	-	30	33.3	-	-	
CO 6	-	-	30	33.3	-	-	

XIV COURSE ARTICULATION MATRIX (PO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

1 - 0 C 5% – No correlation

2 -5 lt;C 40% – Low/ Slight

2 - 40% lt;C lt; 60% –Moderate

3 - 60% C lt; 100% – Substantial /High

COURSE		PROGRAM OUTCOMES				
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	-	-	2	2	-	-
CO 2	-	-	2	2	-	-
CO 3	-	-	2	2	-	-
CO 4	-	-	2	2	-	-
CO 5	-	-	2	2	-	-
CO 6	-	-	2	2	-	-
TOTAL	-	-	12	12	-	-
AVERAGE	-	-	2	2	-	-

XV ASSESSMENT METHODOLOGY INDIRECT:

✓ End Semester OBE Feed Back

XVI SYLLABUS:

UNIT I	REAL-TIME ENVIRONMENT
	Real-time computer system requirements, classification of real time systems, simplicity, global time, internal and external clock synchronization, real time model. Real time communication, temporal relations, dependability, power and energy awareness, real time communication, event triggered, rate constrained, time triggered.
UNIT II	REAL-TIME OPERATING SYSTEMS
	USB bus, introduction, speed identification on the bus, USB states, USB bus communication: Packets,data flow types, enumeration, descriptors,PIC18 micro controller USB interface, C programs; CAN bus: Introduction, frames, bit stuffing, types of errors, nominal bit timing, PIC micro controller CAN interface, simple application with CAN.
UNIT III	SYSTEM DESIGN
	Scheduling problem, static and dynamic scheduling, system design. Validation, time-triggered architecture.
UNIT IV	INTRODUCTION TO CAN
	Introduction to CAN open CAN open standard, object directory, electronic data sheets and devices.
UNIT V	CAN STANDARDS
	Configuration files, service data objectives, network management CAN open messages, device profile encoder.

TEXTBOOKS

1. Hermann Kopetz, "Real–Time systems-Design Principles for distributed Embedded Applications", Springer, 2nd Edition, 2011.

2. Glaf P. Feiffer, Andrew Ayre and Christian Keyold, "Embedded networking with CAN and CAN open", Copperhill Media Corporation, 1st Edition, 2008.

REFERENCE BOOKS:

- 1. Rajkamal, Embedded system-Architecture-Programming-Design", Tata Mc Graw Hill, 3rd Edition, 2011.
- 2. Frank Vahid, Tony Givargis, "Embedded System Design", JohnWiley and sons, 2nd Edition, 2002.
- 3. Lyla B Das, "Embedded Systems-An Integrated Approach", Pearson,1st Edition,2013.
- 4. David E. Simon, "An Embedded Software Primer", PearsonEducation, 1st Edition, 1999.

WEB REFERENCES:

- 1. https://www.youtube.com/watch?v=Uk9zFrEGguM
- 2. http://freevideolectures.com/blog/2010/11/130-nptel-iit-online-courses/

E-TEXT BOOKS:

- 1. http://dsp-book.narod.ru/ESDUA.pdf
- 2. http://esd.cs.ucr.edu/
- 3. www.intel.com/education/highered/Embedded/Syllabus/Embeddedsyllabus.pdf

XVII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
	OBE DISCUSSION		
1	Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Outcomes (PO) and CO-PO Mapping	-	
	CONTENT DELIVERY (THEORY)		
1	Real-time computer system requirements	CO1	T1:1.1, 1.2
2	Classification of real time systems	CO1	T1:1.1, 1.2
3	Simplicity, global time	CO1	T1:2.1,2.2, T2:2.3,2.4
4	Internal and external clock synchronization	CO1	T2:2.5
5	Real time model and Real time communication	CO1	T2:2.6
6	Temporal relations, dependability	CO1	T2:2.6
7	Power and energy awareness	CO1	T1:3.1
8	Event triggered architecture, rate constrained	CO1	T1:3.2
9	Time triggered architecture	CO2	T2:3.5
10	Inter component communication	CO2	T1:3.4
11	Task management and dual role of time	CO2	T1:3.6
12	Inter task interactions	CO2	T1:4.2
13	Process input/output	CO2	T1:4.3
14	Agreement protocols	CO2	T1:4.4

15	Failure faults and amore	CON	T1.4 4
15	Failure faults and errors	CO2	T1:4.4
16	Error detection	CO2	T1:4.4
17	Fault-Tolerant Units	CO2	T1:4.5
18	System design	CO3	T2:5.2
19	Scheduling problem	CO3	T2: 5.1,
		GOA	5.2
20	Static and dynamic scheduling	CO3	T2:6.1,
21	Validation	CO3	$\begin{array}{c} 6.2, \ 6.4 \\ \hline T2:7.2, \end{array}$
21	vandation	005	12.7.2, 7.3, 7.4
22	Time triggered architecture	CO3	T2:8.1, 8.3
23	Introduction to Time-Triggered Protocols	CO3	T2:8.1, 8.3
			-
24	Overview of the TTP/C Protocol Layers	CO3	T1:5.3
25	The Basic CNI, Internal Operation of TTP/C	CO3	T1:5.5, $5.6, 5.7$
96	TTTD / A for Eight Does Appeliestions	CO2	5.6, 5.7
26	TTTP/A for Field Bus Applications	CO3	$\begin{array}{c} T1:5.5, \\ 5.6, \ 5.7 \end{array}$
27	Wide-Area Real-Time Systems	CO3	1.0, 0.7 T1:5.5,
21	Wide-Area Real-Time Systems	005	5.6, 5.7
28	CAN Overview, An Introduction to CAN	CO4	T1:5.5,
20		001	5.6, 5.7
29	Object Dictionary Organization	CO4	T1:5.5,
-			5.6, 5.7
30	Data Type Definitions, Communication Profile	CO4	T1:5.5,
			5.6, 5.7
31	CAN open Devices, Object Dictionary Access Sequences	CO4	T1:5.5,
			5.6, 5.7
32	Using Identifiers and Objects	CO5	T1:5.5,
			5.6, 5.7
33	The Electronic Data Sheets (EDS)	CO5	T1:5.5,
			5.6, 5.7
34	Device Configuration Files (DCF)	CO5	T1:5.5,
			5.6, 5.7
35	Choosing the Devices and Tools	CO5	T1:5.5,
			5.6, 5.7
36	Accessing the CAN open Object Dictionary (OD) with	CO5	T1:5.5, 5.6 , 5.7
97	Service Data Objects (SDO)	COF	5.6, 5.7
37	Handling Process Data with Process Data Objects (PDO)	CO5	$\begin{array}{c} T1:5.5, \\ 5.6, \ 5.7 \end{array}$
9 0	Network Menagement (NMT)	COE	
38	Network Management (NMT)	CO6	$\begin{array}{c} T1:5.5, \\ 5.6, \ 5.7 \end{array}$
20	CAN open Example Configurations and Exercises	CO6	
39	CAN open Example Configurations and Exercises		$\begin{array}{c} T1:5.5, \\ 5.6, \ 5.7 \end{array}$
			0.0, 0.7

40	Contents of CAN open Messages	CO6	T1:5.5, 5.6, 5.7
41	Masters and Managers (DS302)	CO6	$T1:5.5, \\ 5.6, 5.7$
42	Device Profile for Encoder	CO6	$T1:5.5, \\ 5.6, 5.7$
43	Device Profile for Generic I/O (DS401)	CO6	T1:5.5, 5.6, 5.7
44	Safety-Relevant Communication (DSP304, DSP307)	CO6	T1:5.5, 5.6, 5.7
45	Evaluating the System Requirements	CO6	T1:5.5, 5.6, 5.7
	DISCUSSION OF QUESTION BANK		
1	Unit – I: Real-Time Environment	CO1	T1:1.1-1.6
2	Unit– II: Real-Time Operating Systems	CO2	T2:2.1-2.5
3	Unit – III:System Design	CO3, CO4	T1:4.1-4.5,
4	Unit – IV: Introduction To CAN	CO5	T2:5.1-5.4
5	Unit – V:CAN Standards	CO6	T1:6.1- 6.4,7.1- 7.4,T2:8.1- 8.4

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION

Course Title	EMBED	EMBEDDED PROGRAMMING LABORATORY				
Course Code	BESB09					
Program	M.Tech	EMBDDED SY	STEMS)			
Semester	1					
Course Type	Laborato	Laboratory				
Regulation	R18	R18				
		Theory		Pract	ical	
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits	
	-	-	-	3	2	
Course Coordinator	Mr. S Lak	Mr. S Lakshmanachari, Assistant Professor				

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AECB52	VII	Embedded Systems
B.Tech	AECB58	VII	Real Time Systems

II COURSE OVERVIEW:

This course outlines the design and implementation of embedded systems using suitable hardware and Keil Embedded C software tools. The instruction set, Embedded C programming for I/O and memory interfacing techniques are covered. The hands-on experience acquired by the student's during the course makes them to carry out processor/controller based projects and extend their knowledge on the latest trends and technologies in the field of embedded system.

III MARKS DISTRIBUTION:

	Subject	SEE Examination	CIE Examination	Total Marks
En	nbedded Programming Laboratory	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Demo Video	\checkmark	Lab Worksheets	\checkmark	Viva Questions	\checkmark	Probing further Questions	
--------------	------------	--------------	-------------------	--------------	----------------	--------------	------------------------------	--

V EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks forinternal assessment and 70 marks for semester end lab examination. Out of 30 marks of assessment, continuous lab assessment will be done for 20 marks for the day today performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE):The semester end labexamination for 70 marks shall be conducted by two examiners, one of them beingInternal Examiner and the other being External Examiner, both nominated by thePrincipal from the panel of experts recommended by Chairman, BOS. The emphasis on the experiments is broadly based on the following criteria given in Table: 1

	Experiment Based	Programming based
20 %	Objective	Purpose
20 %	Analysis	Algorithm
20 %	Design	Programme
20 %	Conclusion	Conclusion
20 %	Viva	Viva

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Component	Component Laborato		Total Marks
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

1. Experiment Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

2. Programming Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

VI COURSE OBJECTIVES:

The students will try to learn:

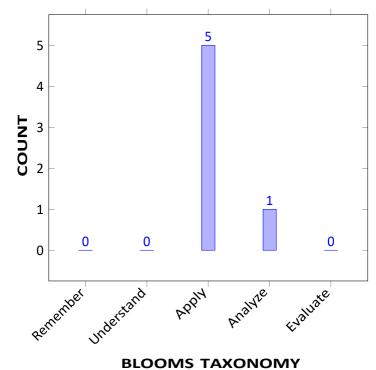
I	Use embedded C for reading data from port pins.
11	Understand the interfacing of data I/O devices with microcontroller.
	Understand serial communication and port RTOS on microcontroller.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Make use of emulators and cross-compilers for writing, compiling and running an embedded C language programs on training boards.	Apply
CO 2	Develop Embedded C language programs for accomplishing code to reading the data from ports, blinking the LED and interfacing of switch and buzzer and temperature sensors to the microcontrollers.	Apply
CO 3	Select suitable RTOS of microcontroller and write Embedded C language program to run 2 to 3 tasks simultaneously.	Apply
CO 4	Choose serial or parallel communication for transmitting the data between microcontroller and peripherals.	Apply
CO 5	Utilize the Analog to Digital and Digital to Analog converters with micro- controller for data conversion.	Apply
CO 6	Build an interface between micro controller and peripherals to provide solutions to the real world problems.	Analyze

COURSE KNOWLEDGE COMPETENCY LEVEL



VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in life long learning through continuing education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	1	Day to Day Evaluation/Cl E/SEE
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.	3	Day to Day Evaluation/Cl E/SEE
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	2	Day to Day Evaluation/Cl E/SEE
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	Day to Day Evaluation/Cl E/SEE
PO 6	Recognize the need to engage in life long learning through continuing education and research.	3	Day to Day Evaluation/Cl E/SEE

3 = High; 2 = Medium; 1 = Low

X JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions to get the solution development and communicate effectively in writing / orally societal problems.	4
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO2	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO3	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO3	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO4	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas. .	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO5	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO5	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO6	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

XI MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES

COURSE	PROGRAM OUTCOMES				
OUTCOMES	PO 1	PO 3	PO 4	PO 5	PO 6
CO 1	6	2	5	3	4
CO 2	6	3	5	7	8
CO 3	6	3	-	4	-
CO 4	6	3	2	7	8
CO 5	6	3	9	7	8
CO 6	6	3	9	7	4

XII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO :

COURSE	PROGRAM OUTCOMES				
OUTCOMES	PO 1	PO 3	PO 4	PO 5	PO 6
CO 1	100	33.3	50	50	50
CO 2	100	50	50	100	100
CO 3	100	50	-	50	-
CO 4	100	50	33.3	100	100
CO 5	100	50	100	100	100
CO 6	100	50	100	100	50

XIII COURSE ARTICULATION MATRIX (CO – PO MAPPING):

COURSE		PROGRAM OUTCOMES			
OUTCOMES	PO 1	PO 3	PO 4	PO 5	PO 6
CO 1	3	1	2	2	2
CO 2	3	2	2	3	3
CO 3	3	2	-	2	-
CO 4	3	2	1	3	3
CO 5	3	2	3	3	3
CO 6	3	2	3	3	2
TOTAL	18	11	11	16	13
AVERAGE	3	1.8	2.2	2.6	2.6

XIV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	1	SEE Exams	1	Seminars	-
Laboratory Practices	1	Student Viva	1	Certification	-

XV ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	\checkmark	End Semester OBE Feedback	
Х	Assessment of Mini Projects by Experts			

XVI SYLLABUS:

WEEK I	LED BLINKING			
	Program to toggle all the bits of port P1 continuously with 250 ms delay.			
WEEK II	INTERFACING OF SWITCH AND BUZZER			
	Program to interface a switch and a buzzer to two different pins of a port such that the buzzer should soundas long as the switch is pressed.			
WEEK III	INTERFACING OF LCD			
	Program to interface LCD data pins to port P1 and display a message on it.			
WEEK IV	INTERFACING SEVEN SEGMENT DISPLAY			

	Program to interface seven segment display.
WEEK V	INTERFACING OF KEYPAD
	Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
WEEK VI	SERIAL COMMUNICATION
	Program to transmit message from microcontroller to PC serially using RS232. Program to receive a message from PC to microcontroller serially using RS232
WEEK VII	INTERFACING OF STEPPER MOTOR
	Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
WEEK VIII	INTERFACING TEMPERATURE SENSOR
	Program to read data from temperature sensor and display the temperature value.
WEEK IX	PORTING OF RTOS
	Port RTOS on to 89V51 Microcontroller and verify. Run 2 to 3 tasks simultaneously on 89V51 SDK. UseLCD interface, LED interface, Serial communication.
WEEK X	INTERFACING OF ADC
	Program to convert analog signal into digital (ADC).
WEEK XI	INTERFACING OF DAC
	Program to convert Digital into Analog (DAC).
WEEK XII	INTERFACING OF ELEVATOR
	Program to interface Elevator.

REFERENCE BOOKS:

1. 1. Michael J. Pont, —Embedded C, Pearson Education, 2 nd Edition, 2008.

2. 2. Nigel Gardner, —The Microchip PIC in CCS C. CCS Inc, 2nd Revision Edition, 2002.

XVII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
1	Program to blinking the LED interfacing with 89V51 microcontroller.	CO1,CO2	R1
2	Program to interfacing of switch and buzzer.	CO1,CO2	R1
3	Program to interfacing of LCD.	CO1,CO2	R1
4	Program to interfacing of Seven segment display.	CO1,CO2	R1
5	Program to interfacing of Keypad.	CO1,CO2	R1
6	Program to perform serial communication using RS232 .	CO1,CO2,CO4	R2
7	Program to interfacing of Stepper mototor	CO1,CO2,CO6	R1
8	Program to interfacing of temperature sensor .	CO1,CO2	R1
9	Program to perform Porting of RTOS.	CO1,CO3	R2
10	Program to interfacing of ADC.	CO1,CO2,CO5	R1
11	Program to interfacing of DAC.	CO1,CO2,CO5	R1
12	Program to interfacing of Elevator.	CO1,CO2,CO6	R2

XVIII EXPERIMENTS FOR ENHANCED LEARNING (EEL):

S.No	Design Oriented Experiments
1	Program to read data from Humidity sensor and display the humidity value.
2	Program to interface a DC Motor to increase and decrease the speed using PWM.
3	Program to interface a IR sensor.

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 COURSE DESCRIPTION

Branch	ELECTRONICS AND COMMUNICATION ENGINEERING						
Course Title	MICRO	MICROCONTROLLERS AND PROGRAMMABLE DSP LAB					
Course Code	BESB10						
Program	M.Tech(H	EMBEDDED S	YSTEMS)				
Semester	Ι	Ι					
Course Type	Core	Core					
Regulation	R18						
		Theory		Pra	actical		
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits		
	-	-	-	3	2		
Course Coordinator	Ms. G Ma	Ms. G Mary Swarna Latha, Assistant Professor					

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	-	-	Digital Signal Processing
B.Tech	-	-	Microprocessors and Microcontrollers

II COURSE OVERVIEW:

This course provides knowledge of basics of DSP processors and embedded C programming language. It covers the concepts like blinking an LED with software delay, system clock real time alteration using the PLL modules and controlling an LED using switch by polling method. Through laboratory experiments, students are provided learning experiences that enable them to provide in depth knowledge about embedded and DSP processors.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
MICROCONTROLLERS	70 Marks	30 Marks	100
AND PROGRAMMABLE DSP LAB			

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Demo Video	\checkmark	Lab	\checkmark	Viva Questions	\checkmark	Probing further
			Worksheets				Questions

V EVALUATION METHODOLOGY:

Each lab will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment. The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being a internal examiner and another is external examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

All the drawing related courses are evaluated in line with lab courses. The distribution shall be 30 marks for internal evaluation (20 marks for day–to–day work, and 10 marks for internal tests) and 70 marks for semester end lab examination. There shall be ONE internal test for 10 marks each in a semester.

The emphasis on the experiments is broadly based on the following criteria given in Table: 1

	Experiment Based	Programming based
20 %	Objective	Purpose
20 %	Analysis	Algorithm
20 %	Design	Programme
20 %	Conclusion	Conclusion
20 %	Viva	Viva

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Component	Labo	Total Marks	
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

1. Experiment Based

Objective	Analysis	Design	Conclusion	Viva	Total
-	-	-	-	-	-

2. Programming Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

VI COURSE OBJECTIVES:

The students will try to learn:

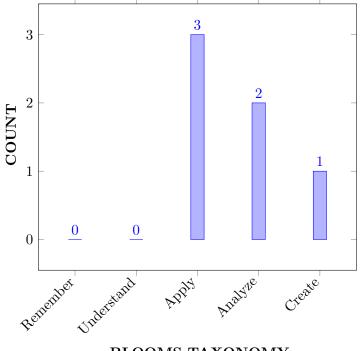
Ι	Demonstrate Keil IDE tool for development of Embedded system.
II	The Program the interfacing of various devices with ARM using Embedded C.
III	Implementation of digital signal processing algorithms in MATLAB and C.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Make use of Cortex-M3 development board write a assembly language	Apply
	program for LED display in various applications	
CO 2	Analyze the various sleep modes by putting core in sleep and deep sleep modes using GNU tool chain	Analyze
CO 3	Develop an embedded C program for Temperature indication on an RGB LED and Verify the output in the Cortex-M3 kit	Apply
CO 4	Build an assembly code and C code to compute Euclidian distance between any two Points	Apply
CO 5	Examine various filters in C to enhance the features of given input sequence or signal	Apply
CO 6	Design an assembly and C code for convolution Operation using code composer studio (CCS).	Create

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes				
PO 1	Independently carry out research / investigation and development work to solve practical				
	problems.				
PO 2	Write and present a substantial technical report / document				
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program.				
	The mastery should be at a level of higher than the requirements in the appropriate				
	bachelor program				
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at				
	designing embedded systems for effective use in communications, IoT, medical				
	electronics and signal processing applications.				
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and				
	responsibly as a member of a team.				
PO 6	Recognize the need to engage in lifelong learning through continuing education and				
	research.				

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	3	CIE/SEE/AAT
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program	3	CIE/SEE/AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	3	CIE/SEE/AAT

X MAPPING OF EACH CO WITH PO(s), PSO(s):

COURSE		PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO1	-	-	\checkmark	\checkmark	-	-	
CO2	-	-	\checkmark	\checkmark	-	-	
CO3	-	-	\checkmark	\checkmark	-	-	
CO4	\checkmark	-	\checkmark	\checkmark	-	-	
CO5	-	-	\checkmark	\checkmark	-	-	
CO6	-	-	\checkmark	\checkmark	-	-	

XI COURSE ARTICULATION MATRIX (PO-PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

 $\boldsymbol{\theta}$ - $0 \leq C \leq 5\%$ – No correlation

- 1 -5 <C \leq 40% Low/ Slight
- $\pmb{2}$ 40 % < C < 60% – Moderate
- $\boldsymbol{3}$ $60\% \leq C < 100\%$ Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	-	-	3	3	-	-
CO 2	-	-	3	3	-	-
CO 3	-	-	3	3	-	-
CO 4	3	-	3	3	-	-
CO 5	-	_	3	3	-	-
CO 6	-	_	3	3	-	-
TOTAL	3	-	18	18	-	-
AVERAGE	3	-	3	3	-	-

XII ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	-	Seminars	-	Student Viva	-
Laboratory Practices	\checkmark	5 Minutes Video /	-	Open Ended	-
		Concept Video		Experiments	
Micro Projects	-	-	-	-	-

XIII ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	\checkmark	End Semester OBE Feedback
-	Assessment of activities / Modeling and Ex	kperin	nental Tools in Engineering by Experts

XIV SYLLABUS:

Part A) Exp	Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain				
WEEK I	Blink an LED with software delay, delay generated using the SysTick timer.				
WEEK II	System clock real time alteration using the PLL modules.				
WEEK III	Control intensity of an LED using PWM implemented in software and hardware				
WEEK IV	Control an LED using switch by polling method, by interrupt method and flash the LED once.				
WEEK V	UART Echo Test.				

WEEK VI	Take analog readings on rotation of rotary potentiometer connected to an ADC channel
WEEK VII	Temperature indication on an RGB LED
WEEK VIII	Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
WEEK IX	Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
WEEK X	System reset using watchdog timer in case something goes wrong.
WEEK XI	Sample sound using a microphone and display sound levels on LEDs.
Part	B) Experiments to be carried out on DSP C6713 evaluation kits and using (CCS)
WEEK XII	To develop an assembly code and C code to compute Euclidian distance between any two points
WEEK XIII	To develop assembly code and study the impact of parallel, serial and mixed execution.
WEEK XIV	To develop assembly and C code for implementation of convolution operation.
WEEK XV	To design and implement filters in C to enhance the features of given input sequence/signal

TEXTBOOKS

- 1. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3", Elsevier, 3rd Edition, 2014.
- 2. Venkatramani B, Bhaskar M, —Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition, 2011.

REFERENCE BOOKS:

- 1. Sloss Andrew N, Symes Dominic, Wright Chris, —"ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publications
- 2. Steve furber, —"ARMSystem-on-ChipArchitecture", Pearson Education.
- 3. Frank Vahid and Tony Givargis, —"Embedded System Design", Wiley Publications

XV COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
1-3	Blink an LED with software delay, delay generated using the SysTick timer.	CO 1	T1: 1.1.5
4-6	System clock real time alteration using the PLL modules.	CO 1	T1: 3.2-3.5
7-9	Control intensity of an LED using PWM implemented in software and hardware	CO 2	T1: 3.5-3.7
10-12	Control an LED using switch by polling method, by interrupt method and flash the LED once.	CO 1	T1: 4.1-4.2
13-15	UART Echo Test.	CO 2	T1: 4.2-4.3

16-18	Take analog readings on rotation of rotary potentiometer	CO 2	T1:
10 10	connected to an ADC channel	002	4.3-4.4
19-21	Temperature indication on an RGB LED	CO 2	T1:5.1-5.2
22-24	Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.	CO 3	T1:5.2,5.5
25-27	Evaluate the various sleep modes by putting core in sleep and deep sleep modes.	CO 3	T1: 6.1-6.2
28-30	System reset using watchdog timer in case something goes wrong.	CO 3	T1: 6.1-6.2
31-33	To develop an assembly code and C code to compute Euclidian distance between any two points	CO 4	T1: 7.1-7.2
34-36	To develop assembly code and study the impact of parallel, serial and mixed execution.	CO 4	T1: 7.1-7.2
37-39	To develop assembly and C code for implementation of convolution operation.	CO 4	T1: 7.4-7.5
40-42	To design and implement filters in C to enhance the features of given input sequence/signal	CO 5	T1: 7.4-7.5
43-45	To develop an assembly code and C code to compute Euclidian distance between any two points	CO 6	T2: 7.6-8.1

Signature of Course Coordinator

HOD,



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 COURSE DESCRIPTION

Branch	ELECTRONICS AND COMMUNICATION ENGINEERING						
Course Title	EMBEL	EMBEDDED SYSTEM ARCHITECTURE					
Course Code	BESB11						
Program	M.Tech(H	M.Tech(EMBEDDED SYSTEMS)					
Semester	II	II					
Course Type	Professional Core						
Regulation	R18						
		Theory		Pra	ctical		
Course Structure Lecture Tutorials Credits Laboratory Credits					Credits		
3 - 3							
Course Coordinator	Dr. V Padmanabha Reddy, Professor						

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
M.Tech	BESB01	Ι	Embedded System Design

II COURSE OVERVIEW:

This course is allows the students to learn the fundamentals of embedded system hardware and firmware design. It focuses on basics of embedded systems, embedded firmware design approaches, development languages and system design. The knowledge acquired from this course will enable the students to implement embedded hardware projects and models for engineering and scientific applications.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Embedded System Architecture	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	PPT		Chalk & Talk	x	Assignments	x	MOOC
x	Open Endeded Experiments	\checkmark	Seminars	x	Mini Project	x	Videos
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with either or choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50 %	To test the objectiveness of the concept
30 %	To test the analytical skill of the concept
20 %	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Theory		Total Marks
Type of Assessment	CIE Exam	Seminar and Term	10tai Marks
		Paper	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

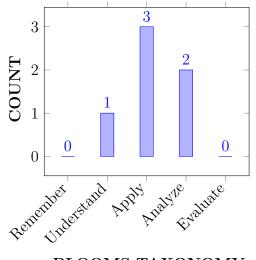
Ι	Understanding of fundamental embedded systems design paradigms, architectures.
II	Interpret possibilities and challenges, both with respect to software and hardware.
III	Analyze a system both as whole and in the included parts, to understand how these parts interact in the functionality and properties of the system.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

-		
CO 1	Summarize the fundamental components that make up an	Understand
	embedded board to implement an Instruction Set Architecture's	
	features in a processor.	
CO 2	Detect the internal processor design operations to achieve better	Analyze
	performance used in embedded systems.	
CO 3	Apply the suitable hardware and memory technology for different	Apply
	applications to meet the ever growing needs of the embedded	
	applications.	
CO 4	Make use an appropriate middleware software for real time	Apply
	embedded system based design .	
CO 5	Categorize the different design stages for designing the embedded	Analyze
	systems.	
CO 6	Identify the hardware software co- design issues pertaining to	Apply
	design of an embedded system using low power microcontrollers.	
L		

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to
	solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of
	the program. The mastery should be at a level of higher than the
	requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer
	skillful at designing embedded systems for effective use in communications,
	IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively,
	creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in life long learning through continuing
	education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 3	Demonstrate the importance of embedded	3	SEE/CIE/AAT
	technologies and design innovative products for		
	solving society relevant problems.		
PO 4	Apply the skills and knowledge needed to serve	2	SEE/CIE/AAT
	as a professional engineer skillful at designing		
	embedded systems for effective use in		
	communications, IoT, medical electronics and		
	signal processing applications.		
PO 6	Recognize the need to engage in life long	1	SEE/CIE/AAT
	learning through continuing education and		
	research.		

3 = High; 2 = Medium; 1 = Low

X MAPPING OF EACH CO WITH PO(s):

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	-	-	\checkmark	\checkmark	-	-
CO2	-	-	\checkmark	\checkmark	-	-
CO3	-	-	\checkmark	\checkmark	-	-
CO4	-	-	\checkmark	\checkmark	-	\checkmark
CO5	-	-	\checkmark	\checkmark	-	\checkmark
CO6	-	-	\checkmark	\checkmark	-	\checkmark

XI JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge , understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions to get the solution development and communicate effectively in writing / orally societal problems .	4
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO2	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO3	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge , understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO4	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas .	1

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO5	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems .	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas.	1
CO6	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO6	PO 6	Recognize the need to engage in lifelong learning through continuing education and research for strengthen in embedded and advanced engineering areas .	1

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – PO/ PSO MAP-PING:

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
	6	6	9	10	7	8	
CO 1	-	-	4	5	-	-	
CO 2	-	-	6	5	-	-	
CO 3		-	5	5	-	-	
CO 4	-	-	5	5	-	1	
CO 5	-	-	6	5	-	1	
CO 6	-	-	6	5	-	1	

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO/ PSO :

COURSE	PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
	6	6	9	10	7	8	
CO 1	-	-	44.4	50	-	-	
CO 2	-	-	66.6	50	-	-	
CO 3		-	55.5	50	-	-	
CO 4	-	-	55.5	50	-	12.5	
CO 5	-	-	66.6	50	-	12.5	
CO 6	-	-	66.6	50	-	12.5	

XIV COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

 $\boldsymbol{\theta}$ - $0 \leq C \leq 5\%$ – No correlation

1 -5 <C \leq 40% - Low/ Slight

 $\pmb{2}$ - 40 % < C < 60% – Moderate

3	- 60%	\leq	C <	100% –	Substantial	/High
---	-------	--------	-----	--------	-------------	-------

COURSE	PROGRAM OUTCOM				IES	
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	-	-	2	2	-	-
CO 2	-	-	3	2	-	-
CO 3	-	-	2	2	-	-
CO 4	-	-	2	2	-	1
CO 5	-	-	3	2	-	1
CO 6	-	-	3	2	-	1
TOTAL	-	-	15	12	-	3
AVERAGE	-	-	2.5	2	-	1

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	\checkmark	Seminars	\checkmark	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XVI ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	End Semester OBE Feed Back
--------------	----------------------------

XVII SYLLABUS:

MODULE I	INTRODUCTION TO EMBEDDED SYSTEMS
	Embedded system model, embedded standards, block diagrams, powering the hardware: Embedded board using von Neuman model; EMBEDDED processors: ISA architecture models, application specific ISA models and general purpose ISA models: Instruction level parallelism.
MODULE II	PROCESSOR HARDWARE
	Internal processor design: ALU, registers, control unit, clock, on chip memory, processor i/o, interrupts, processor buses, processor performance.
MODULE III	SUPPORT HARDWARE
	Board memory: ROM, RAM, cache , auxiliary memory, memory management, memory performance Board buses: Arbitration and timing, PCI bus example, integrating bus with components, bus performance.
MODULE IV	SOFTWARE
	Middleware and applications: PPP, IP middleware UDP, Java. Application layer: FTP client, SMTP, HTTP server and client.
MODULE V	ENGINEERING ISSUES OF SOFTWARE
	Design and development: architectural patterns and reference models: Creating the architectural structures, documenting the architecture, analyzing and evaluating the architecture, debugging testing, and maintaining.

TEXTBOOKS

1. Tammy Noergaard, "Embedded system architecture", Elsevier, 2006.

REFERENCE BOOKS:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", the publisher Paul Temme, 2011.

WEB REFERENCES:

- 1. http://www.nptelvideos.in/2012/11/embedded-systems.html
- 2. http://nptel.iitg.ernet.in/courses/Elec_Engg/IIT %20Delhi/Embedded%20Systems%20(Video).html

COURSE WEB PAGE:

1. https://lms.iare.ac.in/index?route=course/details&course_id=1192

XVIII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference T1: 4.1					
I	OBE DISCUSSION							
1	Course Description on Outcome Based Education(OBE): Course Objectives,Course Outcomes(CO),Program Outcomes(PO) and CO-PO Mapping	-	-					
	CONTENT DELIVERY (THEORY)		1					
lecture No.	Topics to be covered	Course Out- comes	Reference					
1.	Embedded system model	CO1	T1:1.5					
2.	Embedded standards	CO1	T1:2					
3.	Block diagrams	CO1	T1:3.1					
4.	Powering the hardware: Embedded board using von Neuman model	CO1	T1:3.2, 3.3					
5.	EMBEDDED processors: ISA architecture models	CO1	T1:4.1					
6.	Application specific ISA models and general purpose ISA models	CO1	T1:4.1.1					
7.	Instruction level parallelism	CO2	T1:4.1.3					
8.	Internal processor design	$\rm CO2$	T1:4.2					
9.	ALU	$\rm CO2$	T1:4.2.1					
10.	Registers	$\rm CO2$	T1:4.2.1					
11.	Control unit, clock	$\rm CO2$	T1:4.2.1					
12.	On chip memory	$\rm CO2$	T1:4.2.2					
13.	Processor I/O	$\rm CO2$	T1:4.2.3					
14.	Interrupts	$\rm CO2$	T1:4.2.3					
15.	Processor buses	$\rm CO2$	T1:4.2.4					
16.	Processor performance	$\rm CO2$	T1:4.3					
17.	Board memory	$\rm CO2$	T1:5					
18.	ROM, RAM,Cache	CO3	T1:5.1					
19.	Auxiliary memory	CO3	T1:5.3					
20.	Memory management, memory performance Board buses	CO3	T1:5.4					
21.	Arbitration and timing	CO3	T1:7.1					
22.	PCI bus example	CO4	T1:7.1					
23.	Integrating bus with components	CO4	T1:7.2					
24.	Bus performance	CO5	T1:7.3					
25.	Middleware and applications	CO5	T1:10.1					
26.	PPP	CO5	T1:10.3					
27.	IP middleware UDP	CO5	T1:10.3					

28.	Java	CO5	T1:10.3
29.	Application layer: FTP client	CO5	T1:10.4
30.	SMTP	CO5	T1:10.4.2
31.	HTTP server and client	CO5	T1:10.4.3
32.	Design and development	CO6	T1:11
33.	Creating the architectural structures	CO6	T1:11.1
34.	Documenting the architecture	CO6	T1:11.1
35.	Architectural patterns and reference models	CO6	T1:11.1
36.	Analyzing and evaluating the architecture	CO6	T1:11.1
36.	Debugging	CO6	T1:12.1.4
37.	Testing	CO6	T1:12.2
38.	Maintaining	CO6	T1:12.3
	DISCUSSION OF QUESTION BANK		
1	Introduction to Embedded Systems	CO1	R2:1.1
2	Processor Hardware	CO2	R2:2.1
3	Support Hardware	CO3,4	R2:2.6,9.1
4	Software	CO 5	R2:10.1
5	Engineering Issues of Software	CO6	R2: 10.7

Signature of Course Coordinator

HOD,ECE

ANNEXURE - I

KEY ATTRIBUTES FOR ASSESSING PROGRAM OUTCOMES

PO Number	NBA Statement / Key Competencies Features (KCF)	No. of KCF's
PO 1	 Independently carry out research / investigation and development work to solve practical problems. 1. Independence 2. Self driven 3. Quality of work 4. Problem identification and implementation 5. Demonstrate the solutions 6. Budget 	6
PO 2	 Write and present a substantial technical report / document. 1. Demonstrate and communicate effectively in writing report and document/ present orally. 2. Clarity (writing/ presentation) 3. Grammar/ punctuation (writing) 4. References 5. Speaking/ Presenting 6. Subject knowledge while preparing report 	6
PO 3	 Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program. 1. Knowledge, understanding and demonstrations of embedded applications in real time scenario. 2. Ability to demonstrate and communicate effectively in writing / orally societal problems. 3. Analyze and design innovative products 4. Problem formulation and abstraction 5. Use creativity to establish innovative solutions 6. Experimental design 7. Manage the design process and evaluate outcomes using modern tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 	9

PO 4	 Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications. 1. Understand the need of users with the importance of considerations such as IoT and Robotics 2. Scientific principles and methodology 3. Problem formulation and abstraction 4. Use creativity to establish innovative solutions 5. Experimental design 6. Manage the design process and evaluate outcomes 7. Computer software / simulation packages / diagnostic equipment / technical library resources / literature search tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 10. Under take research and development projects in the field of Embedded Systems 	10
PO 5	 Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team. Maturity – requiring only the achievement of goals to drive their performance Self-direction (take a vaguely defined problem and systematically work to resolution) Individual performance is used during the classroom periods, in the hands-on labs, and in the design projects. Knowledge of management techniques which may be used achieve engineering objectives Meeting deadlines and producing solutions Work with all level of people in the team. Demonstrate ability to work well with a team 	7
PO 6	 Recognize the need to engage in lifelong learning through continuing education and research. Project management and research orientation/ Ph.D Strengthen in embedded and advanced engineering areas Continuing education efforts through literature and courses Personal development Plan tasks and resources, manage risk and produce deliverables Meeting deadlines and producing solutions Work with all levels of people in team Demonstrated ability to work well with a team 	8



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043

COURSE DESCRIPTION

Department	Electron	Electronics and Communication Engineering			
Course Title	Interne	Internet of Things			
Course Code	BESB12				
Program	M.Tech				
Semester	II				
Course Type	Core				
Regulation	R18				
		Theory		Pract	ical
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits
	3	1	4	-	-
Course Coordinator	Mr. N Paparao, Assistant Professor				

I COURSE OVERVIEW:

The Internet of things allows every device to connect the world for exchange of information among the associated devices. It focuses on the concepts of data communication, network protocols, cloud computing and network security fundamental techniques, customs and terms including the basic components of hardware and software. The applications of IoT include home automation, smart parking, smart lighting, and smart phone detection.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech		-	Microprocessors and Microcontrollers

III MARKS DISTRIBUTION:

Subject SEE Examination		CIE Examination	Total Marks
Internet of Things 70 Marks		30 Marks	100

IV CONTENT DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Power Point Presentations	\checkmark	Chalk & Talk	x	Assignments	x	MOOC
\checkmark	Open Ended Experiments	x	Seminars	x	Mini Project	x	Videos
	Tech Talks	x	Concept	x	others		
			Videos				

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into five modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The expected percentage of cognitive level of the questions is broadly based on the criteria given in below Table.

45%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
25%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

Continuous Internal Assessment (CIA): For each theory course the CIA shall be conducted by the faculty / teacher handling the course. CIA is conducted for a total of 30 marks, with 20 marks for Continuous Internal Examination (CIE), 05 marks for Assignment and 05 marks for Alternative Assessment Tool (AAT). Two CIE Tests are Compulsory and sum of the two tests, along with the scores obtained in the assignment / AAT shall be considered for computing the final CIA of a student in a given course.

The CIE Tests/Assignment /AAT shall be conducted by the course faculty with due approval from the HOD. Advance notification for the conduction of Assignment/AAT is mandatory and the responsibility lies with the concerned course faculty. CIA is conducted for a total of 30 marks (Table 1), with 25 marks for Continuous Internal Examination (CIE), 05 marks for Technical Seminar and Term Paper

Component		Theory		
Type of	CIE Exam	Assignment	AAT	Total Marks
Assessment				
CIA Marks	20	5	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 8^{th} and 16^{th} week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Assignment:

To improve the writing skills in the course an assignment will be evaluated for 05 marks. One assignment has to submit at the end of the CIE2 for the questions provided by the each course coordinator in that semester. Assignments to be handed in as loose paper collection stapled together at the top left corner. The assignment should be presented as a professional report. It must consist of a cover sheet, content page, and should have an introduction, a body, a conclusion or recommendation, and a reference page

Alternative Assessment Tool (AAT)

In order to encourage innovative methods while delivering a course, the faculty members are encouraged to use the Alternative Assessment Tool (AAT). This AAT enables faculty to design own assessment patterns during the CIA. The AAT enhances the autonomy (freedom and flexibility) of individual faculty and enables them to create innovative pedagogical practices. If properly applied, the AAT converts the classroom into an effective learning center. **The AAT may includes, concept videos, course related term paper, technical seminar, term paper, paper presentations conducted by reputed organizations relevant to the course etc.**

VI COURSE OBJECTIVES:

The students will try to learn:

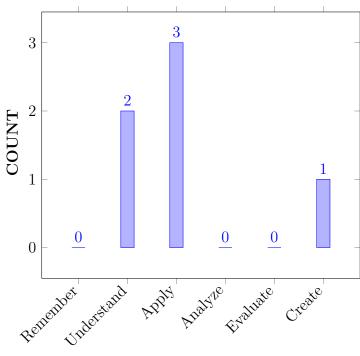
Ι	The principle and operation of software defined networking and network function virtualization.
II	The knowledge of IoT enabled technologies, security protocols and architectures.
III	Python programming skills to move into specific areas – deep learning (DL), data science, machine learning (ML),artificial intelligence (AI) etc.

VII COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1	Understand the programming of microcontroller for the functional	Understand
	stack of IoT ecosystem.	
CO 2	Understand the concepts of data synchronization for agility and	Understand
	autonomy in protocols.	
CO 3	Apply IEEE 802.11 protocol for topology and security in physical	Apply
	and MAC layer.	
CO 4	Identify the applications of IoT including home automation, smart	Apply
	cities, and smart environment to implement the real time applica-	
	tions.	
CO 5	Develop the cloud environment using web enabling constrained	Create
	devices in Internet of things.	
CO 6	Make use of appropriate communication protocolsto acquire the	Apply
	knowledge of programming with Raspberry PI.	

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in lifelong learning through continuing education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	$\mathbf{Strength}$	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	3	SEE/CIE/AAT
PO 2	Write and present a substantial technical report / document.	2	SEE/CIE/AAT

PO 3Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program2		PROGRAM OUTCOMES	Strength	Proficiency Assessed by
	PO 3	as per the specialization of the program. The mastery should be at a level of higher than the	2	SEE/CIE/AAT

3 =High; 2 =Medium; 1 =Low

X MAPPING OF EACH CO WITH PO(s), PSO(s):

COURSE		PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO1	\checkmark	-	\checkmark	-	-	-	
CO2	\checkmark	\checkmark	✓	-	-	-	
CO3	-	\checkmark	✓	-	-	-	
CO4	 ✓ 	-	 ✓ 	-	-	-	
CO5	\checkmark	\checkmark	\checkmark	-	-	-	
CO6	 ✓ 	-	 ✓ 	-	-	-	

XI JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO 1	PO 1	Understand the basic characteristics of IoT along with their enabling technologies by applying the principles of science to engineering problems.	3
	PO 3	Apply the knowledge of physical design and Logical design to appropriate consideration for the public health, safety, cultural, societal and environmental Considerations.	5
CO 2	PO 1	Understand the concept of the IoT levels by applying the principles of science to engineering problem .	2
	PO 2	Understand the knowledge of the IoT levels and deployment models to apply on wireless communication applications.	1
	PO 3	Apply the knowledge of software defined networking to understand the research, analysis and presentation using software aids.	1
CO 3	PO 2	Understand the basic structure of Management system and can collect operational data from IoT devices to applying mathematics , science and engineering fundamentals.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
	PO 3	Apply the knowledge of software defined networking to understand the research, analysis and presentation using software aids.	1
CO 4	PO 1	Understand the performance of different types of Components by applying mathematics, science and engineering fundamentals.	3
	PO 3	Identify the different types of Components to design system components or processes that meet the specified needs with appropriate consideration for the public health, and environmental Considerations	1
CO 5	PO 1	Discuss (Understand) different types of modules in python to write the programming by applying mathematics, science and engineering fundamentals.	3
	PO 2	Apply the programming knowledge to Design solutions for complex engineering problems and design system components.	1
	PO 3	Apply the knowledge of cloud storage models and application programming interfaces to to interface automation tools and program for operation and control of smart antennas for wireless communication applications	2
CO 6	PO 1	Discuss (Understand) different types of modules in python to write the programming by applying mathematics , science and engineering fundamentals.	3
	PO 3	Apply the programming knowledge to Design solutions for complex engineering problems and design system components.	1

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAP-PING:

. COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	10	7	9	6	6	8
CO 1	3	-	2	-	-	-
CO 2	3	1	3	-	-	-
CO 3	-	1	3	-	-	-
CO 4	2	-	2	-	-	-
CO 5	3	1	1	-	-	-
CO 6	3	-	1	-	-	-

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO/ PSO

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	10	7	9	6	6	8
CO 1	100	-	66	-	-	-
CO 2	100	33.3	100	-	-	-
CO 3	0	33.3	100	-	-	-
CO 4	66.6	-	66	-	-	-
CO 5	100	-	66	-	-	-
CO 6	100	-	66	-	-	-

XIV COURSE ARTICULATION MATRIX (PO / PSO MAPPING): CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

- $\boldsymbol{\theta}$ 0 < C< 5% No correlation
- **1** $-5 < C \le 40\% Low / Slight$
- $\pmb{2}$ 40 % <C < 60% Moderate
- $3 60\% \leq C < 100\%$ Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	-	2	-	-	-
CO 2	3	1	3	-	-	-
CO 3	-	1	3	-	-	-
CO 4	2	-	2	-	-	-
CO 5	3	1	1	-	-	-
CO 6	3	-	1	-	-	-
TOTAL	14	3	12	-	-	-
AVERAGE	2.8	1	2	-	-	-

XV ASSESSMENT METHODOLOGY-DIRECT:

CIE Exams	~	SEE Exams	~	Laboratory Practices	-
Assignments	-	Student Viva	-	Certification	-
5 Minutes Video	\checkmark	Seminar and	~	Open Ended	-
/ Concept Video		term paper		Experiments	

XVI ASSESSMENT METHODOLOGY-INDIRECT:

\checkmark	Early Semester	\checkmark	End Semester	\checkmark	Assessment of activities / model-
	OBE Feedback	E Feedback OBE Feedback			ing and experimental tools in en-
					gineering by experts

XVII SYLLABUS:

MODULE I	Fundamentals of IoT
	Evolution of Internet of Things - Enabling Technologies – IoT Architectures: oneM2M, IoT World Forum (IoTWF) and Alternative IoT models – Simplified IoT Architecture and Core IoT Functional Stack – Fog, Edge and Cloud in IoT – Functional blocks of an IoT ecosystem – Sensors, Actuators, Smart Objects and Connecting Smart Objects.
MODULE II	IoT Protocols IoT access technologies
	Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a,802.11ah and LoRaWAN – Network Layer: IP versions, Constrained Nodes and Constrained Networks – Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks – Application Transport Methods: Supervisory Control and Data Acquisition – Application Layer Protocols: CoAP and MQTT.
MODULE III	Design and development design methodology
	Embedded computing logic - Microcontroller, System on Chips - IoT system building blocks - Arduino - Board details. IDE programming -Raspberry Pi - Interfaces and Raspberry Pi with Python Programming
MODULE IV	Data analytics and supporting services
	Structured Vs Unstructured Data and Data in Motion Vs Data in Rest – Role of Machine Learning – No SQL Databases – Hadoop Ecosystem – Apache Kafka, Apache Spark – Edge Streaming Analytics and Network Analytics – Xively Cloud for IoT, Python Web Application Framework – Django – AWS for IoT – System Management with NETCONF-YANG Developing.
MODULE V	IoT Physical Servers and Cloud Offerings
	Introduction to cloud storage models and communication APIs; WAMP: AutoBahn for IoT, Xively cloud for IoT; Case studies illustrating IoT design: Home automation, smart cities, smart environment.

TEXTBOOKS

- 1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, Cisco Press, 2017.
- 2. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-on-Approach", VPT, 1st Edition, 2014.
- 3. Matt Richardson, Shawn Wallace, "Getting Started with Raspberry Pi", O Reilly (SPD), 3rd Edition, 2014.

REFERENCE BOOKS:

- 1. Adrian McEwen, Hakim Cassimally, "Designing the Internet of Things", John Wiley and Sons, 1st Edition, 2014.
- 2. Francis Da Costa, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", Apress Publications, 1st Edition, 2013.

WEB REFERENCES:

1. https://www.upf.edu/pra/en/3376/22580.

- 2. https://www.coursera.org/learn/iot.
- 3. https://bcourses.berkeley.edu.
- 4. www.innovianstechnologies.com.
- 5. https://mitpress.mit.edu/books/internet-things
- 6. http://www.apress.com

XVIII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
	OBE DISCUSSIO	N	
1	Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Outcomes (PO) and CO-PO Mapping	-	https://lms.iare.ac.in/index ?route=course/details& course id_127
	CONTENT DELIVERY (THEOR	.Y)
2	Pre requisites	CO1	T1-3.1-3.2
3	Introduction to Internet of Things	CO 1	T1-3.3-3.4
4	Evolution of Internet of Things	CO 1	T1-3.3-3.4
5	Enabling Technologies – IoT Architectures	CO 1	T1-3.5
6	OneM2M	CO 1	T1-3.5
7	IoT World Forum (IoTWF)	CO 1	T1-3.5
8	Alternative IoT models	CO 1	T1-3.6
9	Simplified IoT Architecture and Core IoT Functional Stack	CO 1	T1-3.7
10	Fog, Edge and Cloud in IoT	CO 1	T1-4.2
11	Fog, Edge and Cloud in IoT	CO 1	T1-4.6
12	IoT Protocols IoT access technologies - Introduction	CO 1	T1-4.7
13	Physical and MAC layers	CO 2	T1-4.10.6
14	topology and Security of IEEE 802.15.4	CO 2	T1-4.11
15	topology and Security of IEEE 802.15.4g	CO 2	T1-5.1.1
16	topology and Security of IEEE 802.15.4e	CO 3	T1-5.1.1
17	topology and Security of IEEE 1901.2a,802.11ah and LoRaWAN	CO 3	T1-5.1.1
18	Network Layer: IP versions	CO 4	T11.1,5.1.2
19	Constrained Nodes and Constrained Networks	CO 4	T1-5.2
20	Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks	CO 4	T1-5.3
21	Application Transport Methods: Supervisory Control and Data Acquisition	CO 4	T1-5.3.2
22	Application Layer Protocols: CoAP and MQTT.	CO 4	T1-5.3.3,5.4
23	Design and development design methodology	CO 4	T1-5.4.2

24	Embedded computing logic - Microcontroller	CO 4	T1-5.5
25	System on Chips - IoT system building blocks - Arduino - Board details	CO 4	TT1-5.11
26	IDE programming -Raspberry Pi	CO 4	T1-5.111
27	Interfaces and Raspberry Pi with Python Programming	CO 5	T1-7.1,7.2
28	Data analytics and supporting service	CO 4	T1-7.3,7.4
29	Structured Vs Unstructured Data and Data in Motion Vs Data in Rest	CO 5	T1-7.7.2
30	Role of Machine Learning –No SQL Databases	CO 5	T1-7.8
31	Hadoop Ecosystem – Apache Kafka	CO 5	T1-7.8.1,8.2
32	Apache Spark –	CO 6	T1-7.10,11
33	Edge Streaming Analytics and Network Analytics	CO 5	T1-7.10.2-3
34	Xively Cloud for IoT, Python Web Application Framework	CO 6	T1 7.10.3.3
35	Django, AWS for IoT – System Management with NETCONF-YANG Developing.	CO 5	T1-7.10.
36	Introduction to cloud storage models and communication APIs	CO 6	R3-P184
37	WAMP: AutoBahn for IoT	CO 6	R3-P185
38	Xively cloud for IoT	CO 6	R3-P191
39	Case studies illustrating IoT design	CO 6	R3-P190
40	Home automation, smart cities, smart environment	CO 6	R3-P1911
	PROBLEM SOLVING/ CAS	SE STUD	DIES
41	SNMP Netopeer	CO 1	T1:5.1.1
42	Serial peripheral interface bus	CO 1	T1:7.3,7.4
43	Inter integrated circuit	CO 2	T1:7.4
44	Raspberry PI - Interfaces (serial, SPI,I2C)	CO 4	T1:7.2
45	Cloud Offerings	CO 2	T1:1-7.8
46	Diversity techniques	CO 1	T1:5.1.1
47	Wireless networks, advantages of wireless local area network	CO 6	R1:184
48	IoT Architecture and challengee	CO 1	T1:4.2
49	Raspberry PI and external interfacing	CO 4	T17-7.2
50	Reference model and architecture	CO 5	T1:5.3.2
51	Logical design using Python	CO 4	T1:4.2
52	Python data types and data structures	CO 5	T1:5.3
53	WLAN standards	CO 6	R3:P185
54	Medium access control,	CO 6	R3-P191
55	High Performance Radio LAN	CO 6	R3-P1911
	DISCUSSION OF DEFINITION AN	ID TERN	AINOLOGY
56	Interoperable characteristics of IoT	CO 1	T1:4.2

57	Software defined networking	CO 2	T1:4.6		
58	Various Types of loops in Python	CO 4	T1:5.11		
59	Class variables Vs instance variables	CO 5	T1:7.1		
61	Infrastructure-as-a-Service	CO 6	T1:7.10		
	DISCUSSION OF QUESTION BANK				
62	Web-based communication models	CO 6	T1:4.2		
63	Network configuration yang module	CO 2	T1:4.6		
64	IoT reference model with diagram	CO 3	T1:5.11		
65	IoT Physical Devices and Endpoints	CO 4	T1:7.1		
66	Case studies in IoT design	CO 6	T1: 7.10		

Course Coordinator:

HOD,ECE

ANNEXURE - I

KEY ATTRIBUTES FOR ASSESSING PROGRAM OUTCOMES

PO Number	NBA Statement / Key Competencies Features (KCF)	No. of KCF's
PO 1	 Independently carry out research / investigation and development work to solve practical problems. 1. Independence 2. Self driven 3. Quality of work 4. Problem identification and implementation 5. Demonstrate the solutions 6. Budget 	6
PO 2	 Write and present a substantial technical report / document. 1. Demonstrate and communicate effectively in writing report and document/ present orally. 2. Clarity (writing/ presentation) 3. Grammar/ punctuation (writing) 4. References 5. Speaking/ Presenting 6. Subject knowledge while preparing report 	6
PO 3	 Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program. 1. Knowledge, understanding and demonstrations of embedded applications in real time scenario. 2. Ability to demonstrate and communicate effectively in writing / orally societal problems. 3. Analyze and design innovative products 4. Problem formulation and abstraction 5. Use creativity to establish innovative solutions 6. Experimental design 7. Manage the design process and evaluate outcomes using modern tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 	9

PO 4	 Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications. 1. Understand the need of users with the importance of considerations such as IoT and Robotics 2. Scientific principles and methodology 3. Problem formulation and abstraction 4. Use creativity to establish innovative solutions 5. Experimental design 6. Manage the design process and evaluate outcomes 7. Computer software / simulation packages / diagnostic equipment / technical library resources / literature search tools 8. Solution development or experimentation / Implementation 9. Interpretation of results and Validation 10. Under take research and development projects in the field of Embedded Systems 	10
PO 5	 Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team. Maturity – requiring only the achievement of goals to drive their performance Self-direction (take a vaguely defined problem and systematically work to resolution) Individual performance is used during the classroom periods, in the hands-on labs, and in the design projects. Knowledge of management techniques which may be used achieve engineering objectives Meeting deadlines and producing solutions Work with all level of people in the team. Demonstrate ability to work well with a team 	7
PO 6	 Recognize the need to engage in lifelong learning through continuing education and research. 1. Project management and research orientation/ Ph.D 2. Strengthen in embedded and advanced engineering areas 3. Continuing education efforts through literature and courses 4. Personal development 5. Plan tasks and resources, manage risk and produce deliverables 6. Meeting deadlines and producing solutions 7. Work with all levels of people in team 8. Demonstrated ability to work well with a team 	8



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043 COURSE DESCRIPTION

Branch	Electronics	Electronics and Communication Engineering(ES)			
Course Title	Embedded	Embedded wireless sensor networks			
Course Code	BESB14	BESB14			
Program	M.Tech	M.Tech			
Semester	11	11			
Course Type	Professional	Professional Elective			
Regulation	IARE- R18	IARE- R18			
		Theory		Prac	tical
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits
	3	0	3	-	-
Course Coordinator	Ms. G Mary SwarnaLatha, Assistant Professor				

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
M.TECH	BESC01	I	EMBEDDED SYSTEM DESIGN
			AND ARCHITECTURE

II COURSE OVERVIEW:

This course introducing basic ideas of wireless, embedded, internetworked sensor/actuator systems, an emerging technology that can provide visibility into and control over complex physical processes. This course covers the overview of WSN, Architecture of wireless networks, sensor programming techniques, programming models and wireless sensor networks for different applications. Wireless sensor networks are a becoming an important application of embedded systems, giving scope for unique designs and applications.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Embedded Wireless sensor	70 Marks	30 Marks	100
Networks			

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

	Power Point	Chalk & Talk	х	Assignments	х	MOOC
	Presentations					
x	Open Ended Experiments	Seminars	x	Mini Project	x	Videos
x	Others					

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

50%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
20%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component		Theory		Total Marks
Type of Assessme	nt	CIE Exam Technical Seminar and Term Paper		
CIA Marks		25	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

Ι	The characteristic requirements and sensor network scenarios to design the embedded wireless sensor networks.
II	The fundamentals of programming sensors and models are used to implement the wireless sensor networks.

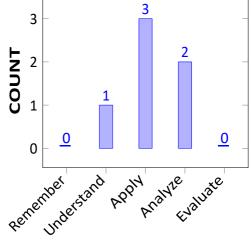
111	Develop program wireless sensor networks using embedded C for real time
	applications.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Relate the concept of wireless sensor networks with characteristic requirements involved in demonstrating of sensor nodes.	Understand
CO 2	Make use of energy consumption of sensor nodes to improve he life span of wireless sensor networks.	Apply
CO 3	Contrast sensor network scenarios for designing of large scale wireless sensor networks.	Analyze
CO 4	Identify the optimisation and figure of merit to measure the performance characteristics of sensor networks.	Apply
CO 5	Categorize tiny os programming for providing interfaces among sensor nodes.	Analyze
CO 6	Utilize inter vehicle communication networks to enhance the safety of moving vehicles.	Apply

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree mastery over the area as per the area of specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.

	Program Outcomes
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in lifelong learning through continuing education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work tosolve practical problems.	2	SEE / CIE / AAT
PO 2	Write and present a substantial technical report / document.	2	SEE / CIE / AAT
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.	2	SEE / CIE / AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	2	SEE / CIE / AAT
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.	2	SEE / CIE / AAT

X MAPPING OF EACH CO WITH PO(s):

COURSE		PRO	DGRAM	OUTCON	/IES	
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	-	1	1	1	-
CO 2	1	1	-	1	1	-
CO 3	1	-	1	1	-	-
CO 4	1	1	-	1	-	-
CO 5	1	-	-	1	-	-
CO 6	1	-	_	1	-	_

XI JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT :

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	understand the concept of wireless sensor networks in real time systems with characteristic requirements involved in demonstrating of sensor nodes in real time scenario.Analyze and design innovative products by Using of creativity to establish innovative solutions	5
	PO 4	 understand the concepts of embedded real time systems for real time embedded applications by Managing the design process and evaluate outcomes and interpreting of results and Validation 	4
	PO 5	Illustrate the concepts knowledge of embedded real time systems for real time embedded applications by using strengthen in embedded and advanced engineering areas by Working with all levels of people in team	2
CO2	PO 3	Demonstrate energy consumption of sensor nodes byunderstanding embedded applications in real time scenario byAnalyzing and design innovative products Appl,y the complex engineering problems and their system components by design and programming of sensor nodes in embedded systems for solution development	5
	PO 4	Make use of time constrained embedded systems using the concepts of engineering fundamentals to the solution of problem formulation and abstraction to establish innovative solutions for Interpretation of results and Validation	4
	PO 5	Improve the life span of wireless sensor networks by Strengthen in embedded and advanced engineering area and time constrained embedded systems using the concepts of engineering fundamentals to the solution of problem formulation and abstraction to establish innovative solutions.	4
CO 3	PO 3	Contrast the design process and evaluation outcomes for Knowledge, understanding and demonstrations of embedded applications in real time scenario for designing of large scale wireless sensor networks for Solution development or experimentation / Implementation in Interpretation of results and Validation	4
	PO 4	Experimental Design for large scale wireless sensor networks by under take research and development projects in the field of Embedded Systemstime constrained application as a member of a small group to meet design specifications.	3

	PO 5	Build time constrained embedded systems using the concepts of engineering fundamentals to the solution of problem formulation and abstraction to establish innovative solutions using RTOS (Real Time Operating System) rapid design and its programming	5
CO4	PO 3	Problem formulation and abstraction by Identifying engineering problems solution development and implementation in various applications of embedded wireless sensor networks.	4
	PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems by Interpreting algorithms of wireless sensor networks for target area coverage to improve the performance of wireless sensor networks.	3
	PO 5	Recognize the need to engage in lifelong learning through continuing education and research to improve the performance of wireless sensor networks.	3
CO5	PO 3	Knowledge understanding and demonstrations of embedded applications in real time scenario by Examine the architecture of multicore embedded systems in Analyze and design innovative products like wireless videosystems.	4
	PO 4	Applythe skills and knowledge needed to serve as a professional engineer skilful by learning the architecture of multicore embedded systems in signal processing applications by Under take research and development projects in the field of Embedded Systems.	4
	PO 5	Using creativity to establish innovative solutions by Apply the principles and architecture of multicore embedded systems to establish Solution development or experimentation / Implementation	4
CO 6	PO 3	Demonstrate problem formulation and abstraction in sensor networks for inter vehicle communication system in Embedded systems.	3
	PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in inter vehicle communication networks to Enchance the safety of moving vehicles.	3
	PO 5	Knowledge, understanding and demonstrations of embedded applications in real time scenario for inter vehicle communication networks by applying the principles and methodology of inter vehicle communication system by Experimental design of communication networks.	5

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – PO MAPPING: COURSE **PROGRAM OUTCOMES** PO 2 OUTCOMES PO 1 PO 3 PO 4 PO 5 PO 6 9 7 8 6 6 10 CO 1 2 6 3 5 _ _ CO 2 2 2 3 3 -_ CO 3 3 4 10 --_ CO 4 3 3 -5 --CO 5 3 5 ----CO 6 2 5 ---

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – PO:

COURSE		PROGRAM OUTCOMES				
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	6	6	9	10	7	8
CO 1	100	-	33.3	50	33.3	-
CO 2	50	50	-	33.3	33.3	-
CO 3	50	-	50	100	-	-
CO 4	50	50	-	50	-	-
CO 5	50	-	-	50	-	-
CO 6	33.3	-	-	50	-	

XIV COURSE ARTICULATION MATRIX (PO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

COURSE		PROGRAM OUTCOMES				
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	-	1	2	1	-
CO 2	2	2	-	1	1	-
CO 3	2	-	2	3	-	-
CO 4	2	2	-	2	-	-
CO 5	2	-	-	2	-	-
CO 6	1	-	-	2	-	
TOTAL	12	4	3	12	2	-
AVERAGE	2	2	1.5	2	1	-

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	1	SEE Exams	1	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	1	Seminars	1	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-

|--|

XVI SYLLABUS:

UNIT I	INTRODUCTION TO WSN:
	Introduction to WSN, challenges for WSNs, characteristic requirements, required mechanisms, C, hardware components, energy consumption of sensor nodes, operating systems and execution environments, some examples of sensor nodes.
UNIT II	NETWORK ARCHITECTURE:
	Sensor network scenarios, optimization goals and figures of merit, design principles for WSNs, service interfaces of WSNs, gateway concepts.
UNIT III	SENSOR NETWORK IMPLEMENTATION:
	Sensor programming, introduction to tiny OS programming and fundamentals of programming sensors using nes C. Algorithms for WSN: Techniques for protocol programming.
UNIT IV	PROGRAMMING MODELS:
	An introduction to the concept of cooperating objects and sensor networks, system architectures and programming models.
UNIT V	CASE STUDIES
	Wireless sensor networks for environmental monitoring, wireless sensor networks with mobile nodes, autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.

TEXTBOOKS

- 1. Holger karl, Andreas Willig, "Protocols and architectures for wireless sensor networks", John Wiley, 1st Edition, 2005.
- 2. Liljana Gavrilovska, Srdjan Krco, Veljko Milutinovic, Ivan Stojmenovic, Roman Trobec, "Application and Multidisciplinary Aspects of Wireless Sensor Networks", Springer, London Limited, 1st Edition, 2011.

REFERENCE BOOKS:

- Michel Banatre, Pedro Jose Marron, Anibal Ollero, A. Dam Wolisz, "Cooperating Embedded Systems and Wireless Sensor Networks", John Wiley and Sons, 1st Edition, 2008.
- 2. Seetharaman Iyengar, Nandhan, "Fundamentals of Sensor Network Programming Applications and Technology", John Wiley and Sons, 1st Edition, 2008. Page

WEB REFERENCES:

1. https://www.youtube.com/watch?v=Uk9zFrEGguM

2. http://freevideolectures.com/blog/2010/11/130-nptel-iit-online-courses/

E-TEXT BOOKS:

- 1. http://dsp-book.narod.ru/ESDUA.pdf
- 2. http://esd.cs.ucr.edu/
- 3. www.intel.com/education/highered/Embedded/Syllabus/Embeddedsyllabus.pdf

XVII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

C 1 Ir 2 C 3 C 4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D	OBE DISCUSSION Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Dutcomes (PO) and CO-PO Mapping CONTENT DELIVERY (THEORY)	-					
C 1 Ir 2 C 3 C 4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D	Course Objectives, Course Outcomes (CO), Program Dutcomes (PO) and CO-PO Mapping CONTENT DELIVERY (THEORY)	-					
2 C 3 C 4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D							
2 C 3 C 4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D		CONTENT DELIVERY (THEORY)					
3 C 4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D	ntroduction to WSN	CO1	T1:1.1				
4 R 5 C 6 Si 7 h 8 E 9 Si 10 Si 11 O 12 fi 13 D Ir D	Challenges for WSNs	CO1	T1:1.2				
5 C 6 Si 7 h 8 E 9 Si 10 Si 11 O 12 fi 13 D Ir D	Characteristic requirements	CO1	T1:1.3				
6 Si 7 h 8 E 9 Si 10 Si 11 C 12 fi 13 D Ir D	Required mechanisms	CO1	T1:1.4				
7 h 8 E 9 So 10 So 11 O 12 fi 13 D Ir D	Cross-Layer Design in Wireless Sensor Networks	CO1	T1:1.5				
8 E 9 So 10 So 11 O 12 fi 13 D Ir D	Single node architecture,	CO1	T1:1.6				
9 Sr 10 Sr 11 C 12 fi 13 D Ir D	nardware components	CO1	T1:2.1				
10 Second	Energy consumption of sensor nodes.	CO1	T1:2.2				
11 C 12 fi 13 D Ir D	Some examples of sensor nodes	CO2	T1:2.3				
12 fi 13 D Ir D	Sensor network scenarios	CO2	T1:2.4				
13 D Ir D	Optimization goals	CO2	T1:2.5				
lr D	igures of merit	CO2	T1:2.6				
14 0	Design principles for WSNs -Distributed organization, n-network processing, Adaptive fidelity and accuracy, Data centricity	CO2	T1:2.7				
E C	Design principles for WSNs -Exploit location information, Exploit activity patterns, Exploit heterogeneity, Component-based protocol stacks and crosslayer Optimization	CO2	T1:2.8				
	Service interfaces of WSNs- Structuring application/protocol stack interfaces	CO2	T1:2.9				
	Service interfaces of WSNs- Expressibility requirements for WSN service interfaces	CO2	T1:2.10				
	Gateway concepts- The need for gateways, WSN to nternet communication	CO2	T1:3.1				
	Gateway concepts- Internet to WSN communication, WSN tunneling	CO3	T1:4.5				
19 F	Fundamentals of programming sensors using nes C	CO3	T1: 4.6				

20	Introduction to TinyOS Programming	CO2	T1:4.7
21	fundamentals of Programming sensors using nesC -continue.	CO3	T1:4.8
22	Algorithms for WSN- Structural Characteristics of Sensor Nodes, Distinctive Properties of Wireless Sensor Networks	CO3	T1:4.9
23	Algorithms for WSN- Sensor Network Stack, Synchronization in Wireless Sensor Networks	CO3	T1:5.1
24	Algorithms for WSN- Collision Avoidance: Token-Based Approach, Carrier Sensing Versus Decoding	CO3	T1:5.2
25	Techniques for Protocol Programming- The Mediation Device Protocol, Contention-Based Protocols, Programming with Link-Layer Protocols, Automatic Repeat Request (ARQ) Protocol, Transmitter Role	CO3	T1:5.3,
26	Techniques for Protocol Programming- Alternating-Bit-Based ARQ Protocols, Selective Repeat/Selective Reject, Naming and Addressing, Distributed Assignment of Networkwide Addresses, Improved Algorithms	CO3	T1:5.5,
27	Techniques for Protocol Programming- Content-Based Addressing, Flooding, Rumor Routing, Tracking, Querying in Rumor Routing	CO3	, 5.6
28	An Introduction to the Concept of Cooperating Objects and Sensor Networks- Cooperating objects and wireless sensor networks	CO4	T1: 5.7.1
29	An Introduction to the Concept of Cooperating Objects and Sensor Networks- Embedded WiSeNts	CO4	T1:5.7.2
30	Programming models- Requirements	CO4	T1:5.7.3,
31	Programming models- State of the art	CO4	T1:5.7.4,
32	System architectures: node internals- Data-centric and service-centric approach, Operating systems, Virtual machines	CO5	T1:5.5.1
33	System architectures: node internals- Data management middleware, Adaptive system software, Summary and evaluation	CO5	T1:5.5.2
34	System architecture: interaction of nodes- Introduction, Communication models	CO5	T1:5.6
35	System architecture: interaction of nodes- Network dynamics, Architectures and functionalities summary	CO5	T1:5.7
36	future work- Programming models,Node internals	CO5	T1:5.8
37	Wireless sensor networks for environmental monitoring	CO6	T1:5.9,
38	Wireless sensor networks for environmental monitoring- continue	CO6	T1:5.10,

39	Wireless sensor networks with mobile nodes	CO6	T1:5.11,
40	Wireless sensor networks with mobile nodes- continue	CO6	T1:5.12
41	Autonomous robotic teams for surveillance	CO6	T1:5.13,
42	Autonomous robotic teams for surveillance- continue	CO6	T1:5.14,
43	Autonomous robotic teams for monitoring	CO6	T1:3.1, 5.6, 5.7
44	Autonomous robotic teams for monitoring	CO6	T1:3.2, 5.6, 5.7
45	Intervehicle communication networks	CO6	T1:3.3,
	DISCUSSION OF QUESTION BANK		
1	Unit – I: Real-Time Environment	CO1	T1:1.1-1.6
2	Unit– II: Network architecture	CO2	T1:2.1-2.5
3	Unit – III:Sensor network implementation	CO3, CO4	T1:4.1-4.5,
4	Unit – IV: Programming codes:	CO5	T1:5.7-5.4
5	Unit – V:Case studies	CO6	T1:5.1- 5.14

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043

COURSE DESCRIPTION

Department	Electronics and Communication Engineering					
Course Title	Microcontro	Microcontrollers for Embedded System Design				
Course Code	BESB16	BESB16				
Program	M.Tech-Emb	M.Tech- Embedded Systems				
Semester	II					
Course Type	Core	Core				
Regulation	R18					
		Theory		Pract	tical	
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits	
	3	-	3	-	-	
Course Coordinator	r Dr. S China Venkateswarlu, Professor					

I COURSE OVERVIEW:

This course outlines the design and implementation of embedded systems using suitable hardware and software tools .It covers 8051 microcontroller architecture, PIC controller, Embedded RISC processor architecture, Interrupts and device drivers and network protocals. The knowledge acquired from this course will enable the students to develop embedded hardware projects and prototype models for engineering and scientific applications.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AECB23	VI	Digital Signal Processing
M.Tech	BESB02	VI	Microcontrollers And Programmable DSP

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Microcontrollers for Embedded System Design	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✓	Power Point	\checkmark	Chalk & Talk	x	Assignments	x	MOOC
	Presentations						
x	Open Ended	1	Seminars	х	Mini Project	х	Videos
	Experiments						
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The expected percentage of cognitive level of the questions is broadly based on the criteria given in below Table.

50%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
20%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Theory CIE Exam Technical Seminar		Total Marks
Type of Assessment			10tai Maiks
		and Term Paper	
CIA Marks	25 5		30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

Ι	The design and implementation of embedded systems using suitable hardware and software tools.
II	The 8051micro controller, ARM and PIC microcontroller for embedded system design and development.

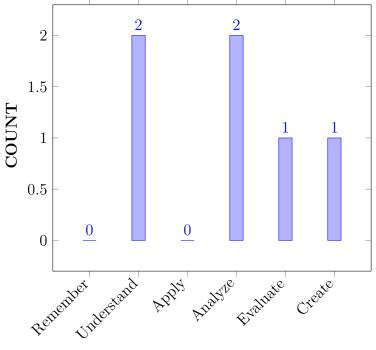
III	The Embedded C- language programming and interfacing various peripherals for
	designing of embedded systems in the field of Communications, Electronic
	measurement, Control systems, Consumer electronics industry and other
	real-time systems.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Summarize the concepts of Embedded Systems for system	Understand
	design with examples.	
CO 2	Compare the architecture and operation of RISC and ARM for	Analyze
	designing embedded system	
CO 3	Demonstrate 8051 microcontroller functionality using registers	Understand
	,memory and Hardware/Software interfacing	
CO 4	Construct programmable system on chip architecture using	Create
	configurable analog and digital blocks	
CO 5	Analyze interrupt latency, context switching time for	Analyze
	development of device drivers	
CO 6	Determine network protocols such as serial, ethernet, SDMA,	Evaluate
	IDMA for high-performance network communication	

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to
	solve practical problems.
PO 2	Write and present a substantial technical report / document
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in
	the appropriate bachelor program
PO 4	Apply the skills and knowledge needed to serve as a professional engineer
	skilful at designing embedded systems for effective use in communications,
	IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively,
	creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in lifelong learning through continuing
	education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	2	CIE/SEE/AAT
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program	2	CIE/SEE/AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	3	CIE/SEE/AAT

X MAPPING OF EACH CO WITH PO(s), PSO(s):

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	\checkmark	-	\checkmark	✓	-	-
CO2	-	-	-	1	-	-
CO3	\checkmark	-	\checkmark	\checkmark	-	-
CO4	-	-	-	\checkmark	-	-
CO5	\checkmark	-	-	\checkmark	-	-
CO6	\checkmark	-	\checkmark	\checkmark	_	-

XI JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING -DIRECT:

Course Out- comes	PO'S	Justification for mapping (Students will be able to)	No. of Key com- petencies matched.
CO1	PO 1	Understand the concepts of Embedded Systems by applying Scientific principles and methodology , Use creativity to establish architecture , identify Problem formulation for interfacing problems , Implement different applications by using arm processor.	6
	PO 3	Analyze the given problem statement and formulate the kernel, and other components in embedded systems and use creativity to establish innovative solutions for embedded system , Interpret the result on various applications	4
	PO 4	Develop embedded hardware units and devices for various Problems in pre processors to implement complex systems	3
CO2	PO 4	Illustrate the architecture of RISC processor task scheduling types for Soft real-time operating system and Hard Real-Time operating systems by using mathematics, science, engineering fundamentals to the solution of complex engineering problems	6
CO3	PO 1	Illustrate components of real time operating systems (knowledge) to integrate the software and hardware components (mathematical model) the design of reliable embedded system by applying the principles of mathematical model and science	5
	PO 3	Construct the high level of integration in embedded applications using 8051 Microcontroller	4
	PO 5	Independently carry out research / investigation and development work to solve practical problems.	3
CO4	PO 4	Analyze (problem statement) finite state machine by applying solutions for complex engineering problems and design system components.	6
CO5	PO 1	Create (Engineering knowledge) semaphore token for the execution of one or more threads in mutual exclusion by applying the principles of mathematics, science.	5
	PO 4	Identify the given problem statement and solve it using synchronization or mutual exclusion by applying mathematical properties.	3
CO6	PO 1	Understand (knowledge) asynchronous communications protocol in operating systems by applying its mathematical properties.	6

РО	 Analyze the given problem statement and formulate the kernel, and other components in embedded systems and use creativity to establish innovative solutions for embedded system , Interpret the result on various applications 	4
РО	Understand (knowledge) asynchronous communications protocol in operating systems by applying its mathematical properties.	3

Note: For Key Attributes refer Annexure - I

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAP-PING:

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	10	7	9	6	6	8
CO 1	3	-	4	6	-	-
CO 2	-	-	-	6	-	-
CO 3	3	-	4	5	-	-
CO 4	-	-	-	6	-	-
CO 5	3	-	-	5	-	-
CO 6	3	-	4	5	-	-

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO, PSO):

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	10	7	9	6	6	8
CO 1	50	-	44.4	60	-	-
CO 2	-	-	-	60	-	-
CO 3	50	-	44.4	50	-	-
CO 4	-	-	-	60	-	-
CO 5	50	-	-	50	-	-
CO 6	50	-	44.4	50	-	-

XIV COURSE ARTICULATION MATRIX (PO-PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

- $\boldsymbol{0}$ $0 \leq C \leq 5\%$ No correlation
- ${\it 1}$ -5 <C ≤ 40% – Low/ Slight
- $\pmb{\mathcal{2}}$ 40 % < C < 60% – Moderate
- $\boldsymbol{3}$ $60\% \leq C < 100\%$ Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	2	-	2	3	-	-
CO 2	-	-	-	3	-	-
CO 3	2	-	2	2	-	-
CO 4	-	-	-	3	-	-
CO 5	2	-	-	2	-	-
CO 6	2	-	2	2	-	-
TOTAL	8	-	6	15	-	-
AVERAGE	2	-	2	2.5	-	-

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	\checkmark	Seminars	\checkmark	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XVI ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	\checkmark	End Semester OBE Feedback
-	Assessment of activities / Modeling a	and E	xperimental Tools in Engineering by Experts

XVII SYLLABUS:

MODULE I	INTRODUCTION TO EMBEDDED SYSTEMS
	Overview of embedded systems, processor embedded into a system, embedded hardware units and devices in system, embedded software, complex system design, design process in embedded system, formalization of system design, classification of embedded systems.
MODULE II	MICROCONTROLLERS
	8051 architecture, input/output ports and circuits, external memory, counters and timers, PIC controllers; Interfacing processor 8051, PIC, memory interfacing, I/O devices, memory controller and memory arbitration schemes.
MODULE III	EMBEDDED RISC PROCESSORS
	Programmable system on chip architectures, continuous timer blocks, switched capacitor blocks, I/O blocks, digital blocks, programming of PSOC. Embedded RISC processor architecture, ARM processor architecture, registers set, modes of operation and overview of Instructions.
MODULE IV	INTERRUPTS AND DEVICE DRIVERS

	Exceptions and Interrupt handling Schemes, Context and periods for context switching, deadline and interrupt latency; Device driver using interrupt service routine, serial port device driver and device drivers for internal programmable timing devices.
MODULE V	NETWORK PROTOCOLS
	Serial communication protocols, Ethernet protocol, SDMA, Channel and IDMA, external bus interface.

TEXTBOOKS

- 1. 1. Raj Kamal, "Embedded systems, Architecture programming and design", Tata Mc Graw Hill,2nd Edition, 2008
- 2. 2. Muhammad Ali Mazidi, Rolin D. Mckinaly, Danny Causy,"PIC Microcontroller and Embedded systems", Pearson Education, 1st Edition, 2008.

REFERENCE BOOKS:

- 1. 1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
- 2. 2. Steve furber, "ARM System-on-Chip Architecture", Pearson Educations.
- 3. Frank Vahid and Tony Givargis, —"Embedded System Design", Wiley Publications

COURSE WEB PAGE:

1. https://www.iare.ac.in/?q=courses/electronics-and-communication-engineeringautonomous/Microcontrollers for Embedded System Design

XVIII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference		
OBE DISCUSSION					
1	Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Outcomes (PO) and CO - PO Mapping	-	https://lms. iare.ac.in/ index?route= course/ details& course_id= 354		
CONTENT DELIVERY (THEORY)					
2	Overview of embedded systems	CO 1	T1: 1.1-1.5		
3	Classification of Embedded Systems	CO 1	T1: 3.2-3.5		
4	Embedded System Design Process	CO 1	T1: 3.5-3.7		
5	Embedded Hardware Units and Devices	CO 1	T1: 4.1-4.2		
6	Embedded software	CO 1	T1: 4.2-4.3		
7	Complex system design	CO 1	T1: 4.3-4.4		

8	Formalization of system design,	CO 1	T1:5.1-5.2
9	Various embedded system units	CO 1	T1:5.2,5.5
10	Embedded system applications	CO 1	T1: 6.1-6.2
11	Problems discursion	CO 1	T1: 6.1-6.2
12	8051 architecture	CO 1	T1: 6.1-6.2
13	input/output ports	CO 2	T1: 7.1-7.2
14	input/output ports	CO 2	T1: 7.1-7.2
15	External memory units	CO 2	T1: 7.4-7.5
16	Counters and timers circuits	CO 2	T1: 7.4-7.5
17	PIC controllers	CO 2	T2: 7.6-8.1
18	PIC controllers Architecture	CO 2	T2: 7.6-8.1
19	Interfacing processor 8051, PIC	CO 2	T1: 8.2-8.5
20	Memory controller and memory arbitration schemes.	CO 2	T1:9.1-9.2
21	Problems discursion	CO 2	T1:9.1-9.
22	Introduction to RISC processors	CO 2	T1: 9.1-9.2
23	Programmable system on chip architectures	CO 3	R2:8.4,8.10
24	I/O blocks of RISC processors	CO 3	R2:8.4-10
25	Digital blocks programming of PSOC.	CO 3	R2:8.4
26	Embedded RISC processor architecture	CO 3	R2: 8.14-8.16
27	ARM processor architecture	CO 3	R2: 8.14-8.16
28	registers set, modes of operation	CO 3	R2: 8.16,8.17
29	Problems discursion	CO 3	R2: 8.16,8.17
30	Exceptions and Interrupt handling Schemes	CO 3	R2:8.22
31	Exceptions and Interrupt handling Schemes with examples	CO 3	R2:8. 27
32	Context and periods for context switching	CO 3	R2:8. 28
33	Deadline and interrupt latency	CO 4	T2: 2.1-2.2
34	Device driver using interrupt service routine	CO 4	T2:2.2-2.4
35	Serial port device driver	CO 4	T2: 2.1-2.4
36	Device drivers for internal programmable timing devices.	CO 4	T2:3.1-2.1
37	Introduction to Network protocols	CO 4	T2: 2.5
38	Serial communication protocols	CO 4	T2: 2.5
39	Serial communication protocols	CO 4	T2: 2.5,13.4
40	Ethernet protocol	CO 4	T2: 2.5,13.4
41	SDMA- spatial division multiple access	CO 5	T2: 2.5-2.6
42	SDMA Channel	CO 5	T2: 13.3
43	Interleave Division Multiple Access	CO 5	T2:13.6-13.5
44	External bus interface.	CO 5	T2: 13.3-13.4
45	Applications of various communication protocals	CO 5	T2: 13.3

46	Problems discursion	CO 6	T2: 13.5
	PROBLEM SOLVING/ CASE ST	UDIES	
47	Problems on embedded systems overview	CO 1	T1: 1.1-1.5
48	Problems on 8051 microcontroller architecture	CO 2	T1: 7.1-7.2
49	Problems on Embedded RISC Processors	CO 3	R2:8.4-10
50	Problems Interrupts and device drivers	CO 4	T2: 2.1-2.4
51	Problems Network protocols	CO 5	T2: 2.5-2.6
	DISCUSSION ON DEFINITION AND TE	RMINOLO	OGY
52	embedded systems overview	CO 1	T1: 1.1-1.5
53	8051 microcontroller architecture	CO 2	T1: 7.1-7.2
54	Embedded RISC Processors	CO 3	R2:8.4-10
55	Interrupts and device drivers	CO 4	T2: 2.1-2.4
56	Network protocols	CO 5	T2: 2.5-2.6
	DISCUSSION ON QUESTION B	ANK	
61	Discursion on embedded systems overview	CO 1	T1: 1.1-1.5
57	Discursion on 8051 microcontroller architecture	CO 2	T1: 7.1-7.2
58	Discursion on Embedded RISC Processors	CO 3	R2:8.4-10
59	Discursion on Interrupts and device drivers	CO 4	T2: 2.1-2.4
60	Discursion on Network protocols	CO 5	T2: 2.5-2.6

Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 AERONAUTICAL ENGINEERING COURSE DESCRIPTION

Course Title	EMBED	EMBEDDED SYSTEM LABORATORY					
Course Code	BESB19	BESB19					
Program	M.Tech(I	EMBEDDED S	YSTEMS)				
Semester	II	II					
Course Type	Laboratory						
Regulation	R18	R18					
		Theory		Pract	ical		
Course Structure	Lecture Tutorials Credits Laboratory Credits						
	3 2						
Course Coordinator	Ms. G Mary SwarnaLatha, Assistant Professor						

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
M.Tech	BESB01	Ι	Embedded System Design
M.Tech	BESB09	Ι	Embedded Programming Laboratory

II COURSE OVERVIEW:

This course outlines the design and implementation of embedded systems using suitable hardware(ARM and PSOC) and Keil Embedded C software tools. The instruction set, Embedded C programming for I/O and memory interfacing techniques are covered. The hands-on experience acquired by the student's during the course makes them to carry out processor/controller based projects and extend their knowledge on the latest trends and technologies in the field of embedded system.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Embedded System Laboratory	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

	Demo Video		Lab		Viva Questions		Probing further
\checkmark		\checkmark	Worksheets	\checkmark		 ✓ 	Questions

V EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day today performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end laberamination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS. The emphasis on the experiments is broadly based on the following criteria given in Table: 1

	Experiment Based	Programming based
20 %	Objective	Purpose
20 %	Analysis	Algorithm
20 %	Design	Programme
20 %	Conclusion	Conclusion
20 %	Viva	Viva

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Component	Labo	Total Marks		
Type of Assessment	Day to day performance	Final internal lab assessment		
CIA Marks	20	10	30	

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

1. Experiment Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

2. Programming Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

VI COURSE OBJECTIVES:

The stude	nts v	will	\mathbf{trv}	to	learn:	

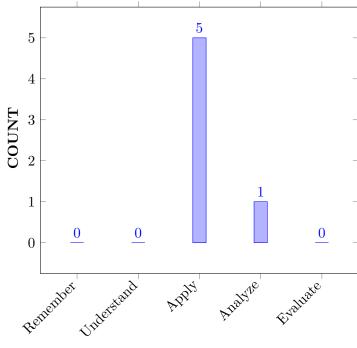
I	Use embedded C for reading data from port pins.
II	Understand the interfacing of data I/O devices with microcontroller.
III	Understand serial communication, port RTOS on microcontroller.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Make use of emulators and cross-compilers for writing, compiling and	Apply
	running an embedded C language programs on ARM and PSoC training	
	boards.	
CO 2	Develop Embedded C language programs for accomplishing code to reading	Apply
	the data from ports, blinking the LED and interfacing of switch and buzzer ,	
	temperature sensors and other display units to the ARM processors.	
CO 3	Select suitable RTOS of ARM and PSoC and write Embedded C language	Apply
	program to run 2 to 3 tasks simultaneously.	
CO 4	Identify different filters and timers in PSoC for transmitting the data	Apply
	between PSOC and peripherals.	
CO 5	Utilize Analog to Digital and Digital to Analog converters with PSoC for	Apply
	data conversion.	
CO 6	Build an interface between PSoC and peripherals to provide solutions to	Analyze
	the real world problems.	

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in life long learning through continuing education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	1	Day to Day Evalua- tion/CIE/SEE
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.	3	Day to Day Evalua- tion/CIE/SEE
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team	2	Day to Day Evalua- tion/CIE/SEE

3 = High; 2 = Medium; 1 = Low

X JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO1	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions to get the solution development and communicate effectively in writing / orally societal problems.	4
	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO2	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO2	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO3	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO4	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO5	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO6	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 5	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

XI COURSE ARTICULATION MATRIX (PO-CO) MAPPING):

COURSE	PROGRAM OUTCO	MES	
OUTCOMES	PO 1	PO 3	PO 5
CO 1	-	2	2
CO 2	-	2	2
CO 3	-	2	2
CO 4	-	2	2
CO 5	2	2	2
CO 6	-	2	2

XII ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Seminars	-
Laboratory Practices	\checkmark	Student Viva	\checkmark	Certification	-

XIII ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	✓	End Semester OBE Feedback
X	Assessment of Mini Projects by Expe	erts	

XIV SYLLABUS:

WEEK I	LED BLINKING
	Program to toggle all the led to port and with some time delay using ARM .
WEEK II	INTERFACING OF LCD
	Interface LCD to ARM7 and display message on screen.
WEEK III	INTERFACING OF KEYPAD
	Interface keypad with ARM7.
WEEK IV	INTERFACING OF LED
	Interface LED with ARM7.
WEEK V	INTERFACING OF STEPPER MOTOR
	Stepper motor interfacing.
WEEK VI	INTERFACING OF DC MOTOR
	DC motor interfacing.
WEEK VII	PROGRAMMABLE GAIN AMPLIFIER
	Study and characterization of the Programmable Gain Amplifier (PGA): Gain Bandwidth Product.
WEEK VIII	FILTERS
	Realization of Low pass, High pass and Band pass filters and their characterization.

WEEK IX	ADC AND DAC
	Experiments with on-chip ADC and DACs.
WEEK X	DIGITAL FUNCTION IMPLEMENTATION
	Digital Function Implementation using Digital Blocks.
	a. Timer experiment
	b. Counter for blinking LED
	c. PWM experiment
	d. Digital buffer and digital inverter
WEEK XI	ALU OPERATIONS
	Logical/Arithmetic function implementation using Microcontroller.
WEEK XII	TIMER
	Timer operation in different Modes.

TEXTBOOKS

- 1. 1.Andrew Sloss, Dominic systems and Chris wright, ARM System Developers guide designing and optimizing system, Elsevier India private limited, New Delhi, 2009.
- 2. Andrew N. Sloss, Dominic Symes, Chris Wright, ARM Systems Developer's Guides Designing and Optimizing System Software, 2008, Elsevier.

REFERENCE BOOKS:

- 1. Michael J. Pont, Embedded C, Pearson Education, 2 nd Edition, 2008
- 2. Nigel Gardner, The Microchip PIC in CCS C. Inc, 2nd Revision Edition, 2002

XV COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
1	Program to toggle all the led to port and with some time delay using ARM .	CO1,CO2,CO3	T1
2	Interface LCD to ARM7 and display message on screen.	CO1,CO2,CO3	T1
3	Interface keypad with ARM7.	CO1,CO2,CO3	T1
4	Interface LED with ARM7.	CO1,CO2,CO3	T1
5	Stepper motor interfacing with ARM7.	CO1,CO2,CO3	T1
6	DC motor interfacing with ARM7 .	CO1,CO2,CO3	T1
7	Study and characterization of the Programmable Gain Amplifier (PGA): Gain Bandwidth Product.	CO1,CO3,CO4	R2
8	Realization of Low pass, High pass and Band pass filters and their characterization.	CO1,CO3,CO4	R2
9	Experiments with on-chip ADC's and DAC's.	CO1,CO3,CO5	R2
10	Digital Function Implementation using Digital Blocks.	CO1,CO3,CO6	R2
11	Logical/Arithmetic function implementation using Microcontroller.	CO1,CO3,CO6	R2
12	Timer operation in different Modes.	CO1,CO3,CO6	R2

XVI EXPERIMENTS FOR ENHANCED LEARNING (EEL):

S.No	Design Oriented Experiments
1	Temperature sensorinterfacing with ARM7.
2	PIR sensor interfacing with ARM7.
3	UART Communication using ARM7

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 ELECTRONICS AND COMMUNICATION ENGINEERING COURSE DESCRIPTION

Course Title	INTERN	INTERNET OF THINGS LABORATORY				
Course Code	BESB20					
Program	M.Tech(H	EMBEDDED S	YSTEMS)			
Semester	II					
Course Type	Laborato	Laboratory				
Regulation	R18	R18				
		Theory		Pract	ical	
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits	
	-	-	-	4	2	
Course Coordinator	Mr. N Papa Rao, Assistant Professor					

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
M.Tech	BESB02	I	Microcontrollers and
			Programmable Digital Signal
			Processing

II COURSE OVERVIEW:

This course outlines the design and implementation of embedded systems using suitable hardware(ARM and PSOC) and Keil Embedded C software tools. The instruction set, Embedded C programming for I/O and memory interfacing techniques are covered. The hands-on experience acquired by the student's during the course makes them to carry out processor/controller based projects and extend their knowledge on the latest trends and technologies in the field of embedded system.

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
Advanced Microprocessors and Interfacing Laboratory	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

	Demo Video		Lab		Viva Questions		Probing further
√		\checkmark	Worksheets	\checkmark		\checkmark	Questions

V EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day today performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end laberamination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS. The emphasis on the experiments is broadly based on the following criteria given in Table: 1

	Experiment Based	Programming based
20 %	Objective	Purpose
20 %	Analysis	Algorithm
20 %	Design	Programme
20 %	Conclusion	Conclusion
20 %	Viva	Viva

Continuous Internal Assessment (CIA):

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Component	Labo	Total Marks	
Type of Assessment	Day to day performanceFinal internal lab assessment		
CIA Marks	20	10	30

Continuous Internal Examination (CIE):

One CIE exams shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

1. Experiment Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

2. Programming Based

Objective	Analysis	Design	Conclusion	Viva	Total
2	2	2	2	2	10

VI COURSE OBJECTIVES:

The stud	ents will	try to	learn:
----------	-----------	--------	--------

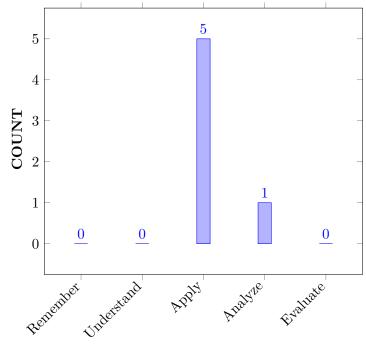
Ι	The IoT using Arduino programming.
II	The interfacing of data I/O devices with Arduino.
III	The design steps using Rasberry Pi.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Make use of Arduino programming for Internet of Things (IoT) on Controlling RGB LED and Wi-Fi Module .	Apply
CO 2	Develop Programming for Internet of things with Android and Arduino to control a remote LED and interface HC-05 Bluetooth Module.	Apply
CO 3	Choose suitable temperature sensor to Interface Tempaetaure sensor and Monitoring the values using IoT with Arduino Uno and display digital value on LCD.	Apply
CO 4	Identify different IR sensors to Interface IR sensors and Bluetooth for detecting obstacle using Arduino with android application.	Apply
CO 5	Utilize GPS module to track location with GPS module and send data from Arduino to Webpage using Wi-Fi module	Apply
CO 6	Analyze the interface sensors on a motion sensor by using GPIO pins with a Raspberry Pi. and Gas sensor for detection and monitoring the values.	Analyze

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes
PO 1	Independently carry out research / investigation and development work to solve practical problems.
PO 2	Write and present a substantial technical report / document.
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.
PO 5	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.
PO 6	Recognize the need to engage in life long learning through continuing education and research.

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency
			Assessed by
PO1	Independently carry out research / investigation and development work to solve practical problems.	1	Day to Day Evalua- tion/CIE/SEE
PO3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program.	3	Day to Day Evalua- tion/CIE/SEE
PO4	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	2	Day to Day Evalua- tion/CIE/SEE

3 = High; 2 = Medium; 1 = Low

X JUSTIFICATIONS FOR CO – PO/ PSO MAPPING -DIRECT:

Course Outcomes			No. of Key competencies matched.
CO1	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions to get the solution development and communicate effectively in writing / orally societal problems.	4
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO2	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO3	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5

Course Outcomes	PO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO3	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
CO4	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems. science and engineering fundamentals.	5
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5
$\rm CO5$	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
CO5	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

Course Outcomes	PO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO6	PO 1	Independently carry out research / investigation and development work strengthen in embedded and advanced engineering areas.	1
	PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems for applying knowledge, understanding and demonstrations of embedded applications in real time scenario and use creativity to establish innovative solutions and make the experimental design with manage the design process and evaluate outcomes using modern tools to get the solution development and communicate effectively in writing / orally societal problems.	6
	PO 4	Apply the concepts (knowledge) of embedded systems using their architectures by using Scientific principles and methodology and problem formulation and abstraction for understand the need of users with the importance of considerations such as IoT and Robotics and use creativity to establish the solutions and make the experimental design.	5

XI COURSE ARTICULATION MATRIX (PO-CO) MAPPING):

COURSE	PROGRAM OUTCOMES		
OUTCOMES	PO 1	PO 3	PO 4
CO 1	2	3	-
CO 2	2	-	2
CO 3	2	3	-
CO 4	2	-	2
CO 5	2	2	3
CO 6	2	3	-

XII ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Seminars	-
Laboratory Practices	\checkmark	Student Viva	\checkmark	Certification	-

XIII ASSESSMENT METHODOLOGY INDIRECT:

\checkmark	Early Semester Feedback	✓	End Semester OBE Feedback
\mathbf{X}	Assessment of Mini Projects by Experts		

XIV SYLLABUS:

WEEK I	IOT WITH ARDUINO PROGRAMMING
	Introduction to Internet of Things (IoT) using Arduino programming.
WEEK II	CONROLLING RGB LED
	Programming for Controlling RGB LED using Arduino and Wi-Fi Module
WEEK III	IOT TO CONTROL REMOTE LED
	Programming for Internet of things with Android and Arduino. Build an Arduino IoT to control a remote LED
WEEK IV	INTERFACING BLUETOOTH MODULE
	Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application.
WEEK V	INTERFACING TO TEMPERATURE SENSOR
	Programming to Interface Tempaetaure sensor and Monitoring using IoT with Arduino Uno and display digital value on LCD.
WEEK VI	INTERFCAING IR SENSOR
	Programming to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android Application.
WEEK VII	TRACK LOCATION
	Programming for Node MCU for track location without using GPS module
WEEK VIII	SEND DATA FROM ARDUINO TO WEB PAGE
	Programming for how to send data from Arduino to Webpage using Wi-Fi module.
WEEK IX	IOT WITH RASBERRY PI
	Introduction to Internet of things (IoT) by using a Raspberry Pi to connect devices.
WEEK X	SETUP WI-FI ON RASBERRY PI USING USB
	Programming for how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle
WEEK XI	INTERFACE TO MOTION SENSOR
	Programming to interface a motion sensor to use GPIO pins with a Raspberry Pi.
WEEK XII	INTERFACE TO GAS SENSOR
	Programming to interface Gas sensor for detection and monitoring using Arduino and IoT.

REFERENCE BOOKS:

- 1. 1. Mark torvalds, —Arduino Programming: Step-by-step guide to mastering arduino hardware and software(Arduino, Arduino projects, Arduino uno, Arduino starter kit, Arduino ide, Arduino yun, Arduino mega, Arduino nano) Kindle Edition, 2 nd Edition, 2009.
- 2. 2. Michael J. Pont, —Embedded C||, Pearson Education, 2 nd Edition, 2008.

XV COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference
1	Introduction to Internet of Things (IoT) using Arduino programming.	CO1,CO2,CO3	T1
2	Programming for Controlling RGB LED using Arduino and Wi-Fi Module	CO1,CO2,CO3	T1
3	Programming for Internet of things with Android and Arduino. Build an Arduino IoT to control a remote LED	CO1,CO2,CO3	T1
4	Programming for how to interface HC-05 Bluetooth Module with Arduino UNO for various application	CO1,CO2,CO3	T1
5	SProgramming to Interface Tempaetaure sensor and Monitoring using IoT with Arduino Uno and display digital value on LCD.	CO1,CO2,CO3	T1
6	Programming to Interface IR sensors and Blue tooth for detecting obstacle using Arduino with android Application.	CO1,CO2,CO3	T1
7	Programming for Node MCU for track location without using GPS module.	CO1,CO3,CO4	R2
8	Programming for how to send data from Arduino to Webpage using Wi-Fi module.	CO1,CO3,CO4	R2
9	Introduction to Internet of things (IoT) by using a Raspberry Pi to connect devices.	CO1,CO3,CO5	R2
10	Programming for how to Setup Wi-Fi on Raspberry Pi 2 using USB Dongle.	CO1,CO3,CO6	R2
11	Programming to interface a motion sensor to use GPIO pins with a Raspberry Pi.	CO1,CO3,CO6	R2
12	Programming to interface Gas sensor for detection and monitoring using Arduino and IoT	CO1,CO3,CO6	R2

XVI EXPERIMENTS FOR ENHANCED LEARNING (EEL):

S.No	Design Oriented Experiments		
1	Program to read data from temperature sensor interfacing with Raspberry Pi		
2	Program to interface a PIR sensor with Arduino.		
3	Program to perform Wi-Fi Communication using Arduino		

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous)

Dundigal, Hyderabad - 500 043

COURSE DESCRIPTION

Branch	Electronics a	Electronics and Communication Engineering			
Course Title	Research Me	ethodology an	d IPR		
Course Code	BCSB31				
Program	M.Tech-Embe	edded Systems			
Semester	III	III			
Course Type	Core	Core			
Regulation	R18	R18			
		Theory Practical			
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits
	2	-	2	-	-
Course Coordinator	Mr. B Santhosh Kumar, Assistant Professor				

I COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
M.Tech	-	-	-

II COURSE OVERVIEW:

This course provides the basic concepts on research methodology and intellectual property rights. This course emphasis on sampling techniques, data collection, writing Reports, Projects, Dissertations, thesis and articles for publication in academic journals, avail the intellectual property rights of the inventors or owners for their assets like patents on innovative design, copy rights on literary and artistic works, trademark on goods & services and geographical indications on products famous for specific geographical areas. This course makes use of the potential future economic benefits to the intellectual property owner or authorized user.

III MARKS DISTRIBUTION:

Subject SEE Examination		CIE Examination	Total Marks	
Research Methodology	70 Marks	30 Marks	100	
and IPR				

IV CONTENT DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Power Point Presentations	\checkmark	Chalk & Talk	x	Assignments	x	MOOC
x	Open Ended Experiments	\checkmark	Seminars	x	Mini Project	x	Videos
\checkmark	Others						

V EVALUATION METHODOLOGY:

Each theory course will be evaluated for a total of 100 marks, out of which 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE).Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE modules and each module carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could

be a maximum of two sub divisions in a question.

The expected percentage of cognitive level of the questions is broadly based on the criteria given in below Table.

50%	To test the objectiveness of the concept		
30 %	To test the analytical skill of the concept		
20 %	To test the application skill of the concept		

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in below table. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	r	Total Marks	
Type of Assessment	CIE Exam Technical Seminar		10tai Marks
		and Term Paper	
CIA Marks	25	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9^{th} and 17^{th} week of the semester respectively. The CIE exam is conducted for 25 marks of 2 hours duration consisting consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

Ι	The knowledge on sources of research problem, data collection, analysis, and interpretation.
II	The importance of effective technical writing and analysis plagiarism.
III	The new developments in the law of intellectual property rights in order to bring progressive changes towards a free market society.

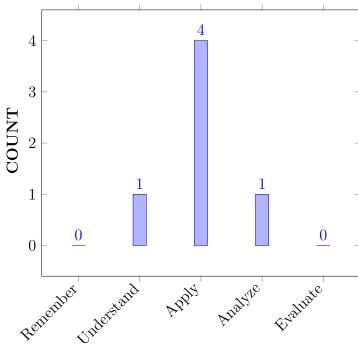
VII COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1	Interpret the technique of determining a research problem for a	Understand
	crucial part of the research study	
CO 2	Examine the way of methods for avoiding plagiarism in research	Analyze
CO 3	Apply the feasibility and practicality of research methodology	Apply
	for a proposed project	
CO 4	Make use of the legal procedure and document for claiming	Apply
	patent of invention.	

CO 5	Identify different types of intellectual properties, the right of ownership, scope of protection to create and extract value from IP	Apply
CO 6	Defend Defend the intellectual property rights throughout the world with the involvement of World Intellectual Property Organization	Apply

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII PROGRAM OUTCOMES:

	Program Outcomes				
PO 1	Independently carry out research / investigation and development work to				
	solve practical problems				
PO 2	Write and present a substantial technical report / document.				
PO 3	Demonstrate a degree of mastery over the area as per the specialization of				
	the program. The mastery should be at a level of higher than the				
	requirements in the appropriate bachelor program.				
PO 4	Apply the skills and knowledge needed to serve as a professional engineer				
	skilful at designing embedded systems for effective use in communications,				
	IoT, medical electronics and signal processing applications.				
PO 5	Function on multidisciplinary environments by working cooperatively,				
	creatively and responsibly as a member of a team.				
PO 6	Recognize the need to engage in lifelong learning through continuing				
	education and research.				

IX MAPPING OF EACH CO WITH PO(s):

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	\checkmark	\checkmark	-	-	-	\checkmark

COURSE		PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	
CO 2	\checkmark	-	-	-	-	\checkmark	
CO 3	\checkmark	\checkmark	-		-	-	
CO 4	\checkmark	\checkmark	-		-	-	
CO 5	\checkmark	-	-	-		\checkmark	
CO 6	-	\checkmark	-	-	-	-	

X JUSTIFICATIONS FOR CO – PO MAPPING -DIRECT:

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
CO 1	PO 1	Describe the steps involved in problem identification for the research process with quality of work and demonstrate the solutions	4
	PO 2	Demonstrate and communicate effectively in writing the research problem with clarity and subject the knowledge while preparing report	4
	PO 6	Describe the importance of continuing education efforts through literature, personal development, meeting deadlines and producing solutions in research study	4
CO 2	PO 1	Explain the methods for avoiding plagiarism in research work for improving the quality of work , self driven and Independence in research process	3
	PO 6	Describe the methods for avoiding plagiarism in research work by continuing education efforts through literature, manage risk, meeting deadlines and producing solutions	3
CO 3	PO 1	Describe the steps of problem identification and implementation in development of independence , quality of work by using research methodology	3
	PO 2	Demonstrate and communicate effectively in writing a proposed project with clarity and avoid the mistakes in terms of grammar (writing) to subject knowledge while preparing report	4
CO 4	PO 1	Demonstrate the solutions and self driven, independence in work for copyright and quality of work in document	4
	PO 2	Demonstrate and communicate effectively in Process of applying presenting Patent with clarity and subject knowledge of intellectual property management for claiming patent of invention	3
CO 5	PO 1	Demonstrate the solutions to attain the right of ownership and independence and self driven for scope of protection	3

Course Outcomes	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key competencies matched.
	PO 6	Continuing education efforts through literature, demonstrated ability to work well with a team, meeting deadlines and producing solutions for licensing and transfer of technology in patent rights	4
CO 6	PO 2	Demonstrate and communicate effectively of the new Developments in IPR with considering references and clarity in presentation	4

XI TOTAL COUNT OF KEY COMPETENCIES FOR CO – PO MAPPING:

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	6	6	9	10	7	8
CO 1	4	4	-	-	-	4
CO 2	3	-	-	-	-	3
CO 3	3	4	-	-	-	-
CO 4	4	3	-	-	-	-
CO 5	3	-	-	-	-	4
CO 6	-	4	-	-	-	-

XII PERCENTAGE OF KEY COMPETENCIES FOR CO - PO

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
	6	6	9	10	7	8
CO 1	66.6	66.6	-	-	-	50
CO 2	50	-	-	-	-	37.5
CO 3	50	66.6	-	-	-	-
CO 4	66.6	50	-	-	-	-
CO 5	50	-	-	-	-	50
CO 6	-	66.6	-	-	-	-

XIII COURSE ARTICULATION MATRIX (PO MAPPING): CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

 $\boldsymbol{\theta}$ - 0 \leq C \leq 5% – No correlation

- 1 -5 <C \leq 40% Low/ Slight
- $\pmb{2}$ 40 % < C < 60% Moderate
- $\boldsymbol{3}$ $60\% \leq C < 100\%$ Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	3	-	-	-	2
CO 2	2	-	-	-	-	1
CO 3	2	3	-	-	-	-
CO 4	3	2	-	-	-	-
CO 5	2	-	-	-	-	2
CO 6	-	3	-	-	-	-
Total	12	11	-	-	-	5
Average	2.4	2.75	-	-	-	1.7

XIV ASSESSMENT METHODOLOGY-DIRECT:

CIE Exams	\checkmark	SEE Exams	\checkmark	Seminars	 ✓
Laboratory Practices	-	Student Viva	-	Certification	-
Term Paper	~	5 Minutes Video	-	Open Ended Experiments	-
Assignments	-				

XV ASSESSMENT METHODOLOGY-INDIRECT:

\checkmark	Early Semester Feedback	\checkmark	End Semester OBE Feedback
\checkmark	Assessment of mini projects by experts		

XVI SYLLABUS:

MODULE I	INTRODUCTION
	Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research
	problem, Scope and objectives of research problem. Approaches of
	investigation of solutions for research problem, data collection, analysis,
	interpretation, Necessary instrumentations
MODULE II	RESEARCH ETHICS
	Effective literature studies approaches, analysis Plagiarism, Research ethics.
MODULE III	RESEARCH PROPOSAL
	Effective technical writing, how to write report, Paper Developing a Research Proposal. Format of research proposal, a presentation and assessment by a review committee
MODULE IV	PATENTING
	Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT
MODULE V	PATENT RIGHTS

Patent Rights: Scope of Patent Rights. Licensing and transfer of
technology. Patent information and databases. Geographical Indications.
New Developments in IPR: Administration of Patent System. New
developments in IPR; IPR of Biological Systems, Computer Software etc.
Traditional knowledge Case Studies, IPR and IITs

TEXTBOOKS

- 1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science and engineering students".
- 2. C R Kothari, "Research Methodology: Methods and techniques", New age international limited publishers, 1990 .
- 3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"

REFERENCE BOOKS:

- 1. Halbert, "Resisting Intellectual Property", Taylor and Francis Ltd , 2007.
- 2. Mayall, "Industrial Design", McGraw Hill, 1992.
- 3. Niebel , "Product Design", McGraw Hill, 1974.

WEB REFERENCES:

- 1. Robert P. Merges, Peter S. Menell, Mark A. Lemley Age", 2016 , "Intellectual Property in New Technological Age", 2016
- 2. T. Ramappa, "Intellectual Property Rights Under WTO" S. Chand 2008
- 3. Peter-Tobias stoll, Jan busche, Katrianarend- WTO- Trade –related aspects of IPR-Library of Congress

COURSE WEB PAGE: https://lms.iare.ac.in/index?route=course/details&course_id=367

XVII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference					
	OBE DISCUSSION							
0	0 Course Description on Outcome Based Education (OBE): Course Objectives, Course Outcomes (CO), Program Outcomes (PO) and CO-PO Mapping							
	CONTENT DELIVERY (THEORY)							
1	Introduction, Definition, types of research	CO 1	T1:2.1					
2	Meaning of research problem	CO 1	T1:2.1					
3	Sources of research problem	CO 1	T1:2.3					
4	Criteria characteristics of good research problem	CO 1	T1:2.3.1					
5	Research process	CO 1	T1:7.2					
6	Research design	CO 1	T1:7.3					

7	Errors in selecting a research problem	CO 1	T1:7.4
8	Scope and objectives of research problem	CO 1	T1:2.3
9	Approaches of investigation of solutions for research problem	CO 1	T1:2.3
10	Data collection	CO 1	T1:7.4
10	Analysis and interpretation of data	CO 1	T1:8.1.1
11	Necessary instrumentation's	CO 1	T1:8.1.1
12	Effective literature studies approaches	$\frac{\text{CO I}}{\text{CO 2}}$	T1:8.2
13	Literature	$\frac{\text{CO 2}}{\text{CO 2}}$	T1:8.2
14	Literature Literature review	$\frac{\text{CO 2}}{\text{CO 2}}$	T1:8.2
10 16	Literature review techniques	$\frac{\text{CO 2}}{\text{CO 2}}$	T1:8.2
10	Literature studies	$\frac{\text{CO 2}}{\text{CO 2}}$	T1:8.2
		$\frac{\text{CO 2}}{\text{CO 2}}$	
18	Introduction to ethics, Importance of ethics		T1:8.2
19	Ethical issues in conducting research	$\frac{\text{CO } 2}{\text{CO } 2}$	T1:8.3
20	Principles of research ethics	CO 2	T1:8.4
21	Analysis	CO 2	T1:8.5
22	Plagiarism- types of plagiarism	CO 2	T1:8.6
23	Tips to avoid plagiarism	CO 2	T1:9.1
24	Other ethical issues	CO 2	T1:9.2, 9.3
25	Interpretation, Interpretation Techniques and precautions	CO 2	T2:9.3.4
26	Writing of report and steps involved	CO 3	T2:7.1
27	Layout of research report	CO 3	T2:7.2
28	Types of reports	CO 3	T2:7.3
29	Paper developing a research proposal	CO 3	T2:7.4
30	Format of research proposal	CO 4	T2:8.3
31	Presentation of report	CO 4	T2:8.4
32	Summary of findings	CO 4	T3:8.5
33	Assessment by review committee	CO 4	T3:8.6
34	Technical appendixes	CO 4	T3:8.6
35	Logical analysis of the subject matter	CO 4	T3:8.6
36	Statement of findings and recommendations	CO 4	T3:8.6
37	Introduction, Nature of Intellectual Property	CO 5	T3:10.1- 10.6
38	Types of intellectual Property rights	CO 5	T3:10.1- 10.6
39	Patents	CO 5	T3:11.10
40	Designs	CO 5	T3:11.10
41	Trademarks and copyrights: Definition, classification of trademarks	CO 5	T3:11.10
42	Process of Patenting and Development	CO 5	T3:11.14
43	Technical research, innovation, patenting	CO 5	T3:11.15
44	Developments in patenting	CO 5	T3:11.17
	Patent Trademark Organization	CO 5	T3:11.17
45			

47	International scenario, international cooperation on Intellectual property	CO 5	T3:11.19
48	Procedure for grant of patents	CO 5	T3:11.21
49	procedure of copyright	CO 5	T1:8.1- 8.3; R2: 7.4-7.5
50	Patenting under PCT, Provisional patent application	CO 5	T1-8.1- 8.1.7
51	Patent protection for the invention	CO 5	T1-8.1- 8.1.7
52	Patent Rights	CO 6	T3:12.1
53	Scope of Patent Rights	CO 6	T3:12.1
54	Licensing and transfer of technology	CO 6	T3:12.1
55	Patent information and databases	CO 6	T3:12.4
56	Geographical Indications	CO 6	T3:12.4
57	New Developments in IPR: Administration of Patent System	CO 6	T3:12.7
58	New developments in IPR, IPR of Biological Systems and Computer Software etc	CO 6	T3:12.10
59	Traditional knowledge Case Studies	CO 6	T3:12.13
60	IPR and IITs.	CO 6	T3:12.15
	DISCUSSION OF QUESTION BANK		1
61	Module – I: Research problem	CO 1	T1:2.1- 2.3
62	Module – II: Research ethics	CO 2	T1:8.2
63	Module – III: Research proposal	CO 3, CO 4	T3:8.3; R2: 7.4-7.5
64	Module – IV: Patenting	CO 5	T3:10.1- 10.6
65	Module – V: Patent rights	CO 6	T3:12.1- 12.15

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION

Course Title	EMBEDD	EMBEDDED REAL TIME OPERATING SYSTEMS			
Course Code	BESB22				
Program	M.Tech	M.Tech			
Semester	111	III ES			
Course Type	Professional	Professional Elective			
Regulation	IARE - R18	IARE - R18			
		Theory		Prac	tical
Course Structure	Lecture	Lecture Tutorials Credits Labor			Credits
	3 - 3			-	
Course Coordinator	Ms. G Bhava	Ms. G Bhavana, Assistant Professor			

I COURSE OVERVIEW:

This course is to introduce students with the basic concepts and approaches in the design and analysis of real-time operating systems. It covers design considerations of real time operating systems, task scheduling, threads, multitasking, task communication and synchronization. Applications of the course include real time operating systems in image processing, fault tolerant applications and control systems.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AECB58	VII	Embedded Systems

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
EMBEDDED REAL TIME OPERATING SYSTEMS	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

\checkmark	Power Point	\checkmark	Chalk & Talk	х	Assignments	х	MOOC
	Presentations						
×	Open Ended	\checkmark	Seminars	х	Mini Project	х	Videos
	Experiments						
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carriesequal weightage in terms of marks distribution. The question paper pattern shall be as defined below. Two full questions with 'either' 'or' choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question. The emphasis on the questions is broadly based on the following criteria:

50%	To test the objectiveness of the concept
30%	To test the analytical skill of the concept
20%	To test the application skill of the concept

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Th	Total Marks
Type of Assessment	CIE Exam	
CIA Marks	25	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

Technical Seminar and Term Paper:

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

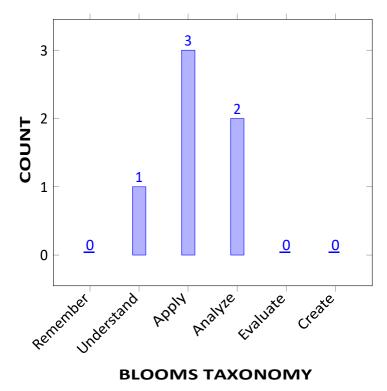
I	The concepts of operating systems and principles of real time operating system, implementation aspects of real time concepts in embedded systems.
11	The design of real time operating system by using the concepts of Timers, I/O subsystem and Memory management units.
111	Software development process and tools like Vxworks and muCOS for real time operating system applications.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

	ssiul completion of the course, students should be able t	0.						
CO 1	CO 1 Outline the components of real time operating systems for the design of reliable embedded system.							
CO 2	Interpret real time operating system to provide resource management and synchronization for communication systems.	Apply						
CO 3	Identify Real-Time Clocks and System Clocks to keep tracks of current time and clock speeds.	Apply						
CO 4	Construct memory management system for fragmentation and compaction.	Apply						
CO 5	Examine hierarchical Timing Wheels to reduce timer overflow in single timing wheel and multiple timing wheels.	Analyze						
CO 6	Analyze finite state machine for the task scheduling and execution in kernel models.	Analyze						

COURSE KNOWLEDGE COMPETENCY LEVEL



VIII PROGRAM OUTCOMES:

	Program Outcomes					
PO 1	Apply the skills and knowledge needed to serve as a professional engineer skillful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.					
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.					
PO 3	Demonstrate the importance of embedded technologies and design new innovative products for solving society relevant problems					
PO 4	Write and present a substantial technical report / document.					
PO 5	Independently carry out research / investigation and development work to solve practical problems.					
PO 6	Recognize the need to engage in lifelong learning through continuing education and research.					

3 = High; 2 = Medium; 1 = Low

IX HOW PROGRAM OUTCOMES ARE ASSESSED:

	PROGRAM OUTCOMES	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	2	CIE/SEE/AAT
PO 2	Function on multidisciplinary environments by working cooperatively, creatively and responsibly as a member of a team.		
PO 3	Demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level of higher than the requirements in the appropriate bachelor program	2	CIE/SEE/AAT
PO 4	Apply the skills and knowledge needed to serve as a professional engineer skilful at designing embedded systems for effective use in communications, IoT, medical electronics and signal processing applications.	3	CIE/SEE/AAT
PO 5	Independently carry out research / investigation and development work tosolve practical problems.	2	CIE/SEE/AAT
PO 6	Recognize the need to engage in lifelong learning through continuingeducation and research.	2	CIE/SEE/AAT

COURSE		PROGRAM OUTCOMES							
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6			
CO1	✓	-	-	✓	✓	✓			
CO2	✓	✓	-	✓	-	-			
CO3	✓	✓	-	✓	✓	~			
CO4	-	✓	✓	 ✓ 	✓	-			
CO5	✓	✓	-	✓	✓	~			
CO6	✓	-	-	✓	-	✓			

X MAPPING OF EACH CO WITH PO(s), PSO(s):

XI JUSTIFICATIONS FOR CO – (PO, PSO) MAPPING -DIRECT:

COURSE OUTCOMES	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key Competencies
CO1	PO 2	Understand the importance of network types, suitable transmission medium, devices and the Internet in supporting business communications and everyday activities by understanding fundamentals of Computer engineering specialization and scientific principles.	1
CO2	PO 2	Understand the significance of data communication models, packet switching, circuit switching for internal and external operations, in data communications and networking using mathematical principles, fundamental of Computer engineering specialization and scientific principles.	2
CO3	PO 1	Explain the concept of Hamming distance, and the significance of the minimum Hamming Distance and its relationship to errors by understanding mathematical principles and scientific principles.	3
CO4	PO 4	Describe the relationship between data and signals, their types, behavior, properties, characterization and transmission through the physical layer by understanding mathematical principles and scientific principles.	2
	PO 3	Explain the role of Protocol in data transmission and types of their versions by understanding mathematical principles and scientific principles	3
CO5	PO 1	Analyze the correct transport layer protocol, such as TCP, UDP, SCTP to transfer data segments in the networks using mathematical principles and scientific principles	3
	PO 2	Apply standardised protocols in applications for secure data transmission in the network by applying the knowledge of computer engineering fundamentals, mathematical principles, and scientific principles.	2
CO6	PO 4	Describe importance of email system by apply the the knowledge of computer engineering fundamentals, and scientific principles.	2

XII TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAPPING:

COURSE	PROGRAM OUTCOMES							
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6		
CO 1	6	-	-	5	2	2		
CO 2	3	3	-	2	-	-		
CO 3	6	3	-	5	4	8		
CO 4	-	3	9	10	7	-		
CO 5	6	3	-	10	4	4		
CO 6	6	-	-	2	-	4		

XIII PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO, PSO):

COURSE	PROGRAM OUTCOMES							
OUTCOMES	PO 1	PO 5	PO 6					
CO 1	100	-	-	50	33.3	33.3		
CO 2	50	50	-	33.3	-	-		
CO 3	100	50	-	50	50	100		
CO 4	-	50	100	100	100	-		
CO 5	100	50	-	100	50	50		
CO 6	100	-	-	33.3	-	50		

XIV COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being **no correlation**, 1 being the **low correlation**, 2 being **medium correlation** and 3 being **high correlation**.

- **0** $0 \le C \le 5\%$ No correlation
- 1 -5 < C \leq 40% Low/ Slight
- **2** 40 % <C < 60% –Moderate
- **3** 60% \leq C < 100% Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	-	-	2	1	1
CO 2	2	2	-	1	-	-
CO 3	3	2	-	2	2	3
CO 4	-	2	3	3	3	-
CO 5	3	2	-	3	2	2
CO 6	3	-	-	1	-	2
TOTAL	14	8	3	12	8	8
AVERAGE	2.8	2	3	2	2	2

XV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	1	SEE Exams	1	Assignments	1
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	-	Seminars	-	Student Viva	-
Laboratory	-	5 Minutes Video /	1	Open Ended	-
Practices		Concept Video		Experiments	
Micro Projects	_	-	-	-	-

XVI SYLLABUS:

MODULEI	INTRODUCTION
	Introduction to UNIX/LINUX, overview of commands, file I/O (open, create, close, lseek, read, write), process control (fork, vfork, exit, wait, waitpid, exec).
MODULE II	REAL TIME OPERATING SYSTEM
	Brief history of OS, defining RTOS, Scheduler, objects, services, characteristics of RTOS, defining a task, task states and scheduling, task operations, structure, synchronization, communication and concurrency, defining semaphores, operations and use, defining message queue, states, content, storage, operations and use.
MODULE III	OBJECTS, SERVICES AND INPUT OUTPUTS
	Pipes, event registers, signals, other building blocks, component configuration. Basic I/O concepts, I/O subsystem.
MODULE IV	EXCEPTIONS , INTERUPTS AND TIMERS
	Exceptions, interrupts, applications, processing of exceptions and spurious interrupts, real time clocks, programmable timers, timer interrupt service routines, soft timers, operations.
MODULE V	CASE STUDIES OF RTOS
	RT Linux, Micro C/OS-II, Vx works, embedded linux, tiny OS and basic concepts of android OS.

TEXTBOOKS

1. Quing Li, "Real Time Concepts for Embedded Systems", Elsevier, 1st Edition, 2011

REFERENCE BOOKS:

- 1. Rajkamal,"Embedded system Architecture programming and Design" Tata Mc Graw Hill,2nd Edition 2003.
- 2. Richard steven,"Advanced UNIX Programming", Addision Wesely professional,3rd Edition 2013.
- 3. Dr.Craig Hollabaugh ,"Embedded Linux :Hardwar0e,software and Interfacing",Addision Wesely,1st Edition,2002

XVII COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference T1: 4.1
1-2	Understand the basic concepts of operating system.	CO 1	T1:1.1- 1.8, 2.2
3-4	Defining RTOS, classification of real-time systems	CO 1	T1:1.10
5-6	Overview of Unix/Linux Commands.	CO 2	T1:2.7
7-8	Acquire the knowledge about the Process Control	CO 2	T1:2.8
9-10	Defining RTOS, classification of real-time systems	CO 2	T1:2.8
11-12	The scheduler, objects, services and key characteristics of RTOS.	CO 3	T1:3.1- 3.2
13-14	Tasks: Defining a task, task states and scheduling, typical task, typical task structure.	CO 3	T1:3.3- 3.7
15-16	Semaphores: Defining semaphores, typical semaphore operations	CO 3	T1:4.2,7.1- 7.4
17-18	Typical semaphore use; Message Queues: Defining message queues, message queue states	CO 3	T1: 7.6 7.7
19-20	Discuss the message queues, message queue states, message queue storage, typical message queue operations	CO 4	T1:1.1 R3:1.1- 1.4
21-22	Typical message queue use other kernel objects	CO 4	T1:1.1- 1.2
23-24	Discuss the Concepts of Pipes, event registers	CO 4	T1:1.3 R3:1.7,7.4
25-26	Acquire the knowledge of signals, condition variables.	CO 4	T1:3.1- 3.4 R3:2.1- 2.4
27-28	Discuss about the exceptions and interrupts	CO 5	T1:3.3- 3.5
29-30	Discuss the applications of exceptions and interrupts	CO 5	R3:2.8,3.7- 3.8
31-32	Discuss about the programmable interrupt controller	CO 5	T1:5.1 5.10 R3:3.6
33-34	Illustrate the Timers and timer services.	CO 6	T1:4.4- 4.6
35-36	Model for implementing the soft-timer handling facility, timing wheels.	CO 6	T1:6.1,6.4 R3:4.1- 4.5
37-38	Discuss programmable interval timers	CO 6	T1:6.3,6.10 R3:4.9- 4.10
39-40	Discuss timer interrupt service routines	CO 6	T1:6.9,5.12

41	RTOS application domains, Comparison and study of RTOS	CO 6	T1:7.1 R3:5.2- 5.3
42	Vxworks and its Case studies: RTOS for image processing	CO 6	T1:7.2- 7.6 R3:5.4- 5.5
43	Discuss about muCOS,	CO 6	T1:8.1- 8.3
44	Explain the embedded Linux and its real time applications .	CO 6	T1:7.2- 7.6 R3:5.4- 5.5
45	Explain the Tiny OS and Android OS	CO 6	T1:7.2- 7.6 R3:5.4- 5.5

Signature of Course Coordinator

HOD,ECE



INSTITUTE OF AERONAUTICAL ENGINEERING (Autonomous) Dundigal, Hyderabad - 500 043 ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTION

Course Title	WASTE TO	WASTE TO ENERGY				
Course Code	BCSB30	BCSB30				
Program	M.Tech	M.Tech				
Semester	111	ES,CSE				
Course Type	Open Elective	Open Elective				
Regulation	IARE - R 18	IARE - R 18				
	Г	heory		Practio	cal	
Course Structure	Lecture	Tutorials	Credits	Laboratory	Credits	
	3	-	3	-	-	
Course Coordinator	Mrs.C.Radhika	Mrs.C.Radhika, Assistant Professor				

I COURSE OVERVIEW:

The course is designed to create environmental awareness and consciousness among the present generation to become environmental responsible citizens. The course will discuss on the municipal solid waste composition, characteristics and to improve the methods to minimize municipal solid waste generation. This course deals with methods of disposal of solid waste by thermal biochemical processes and production of energy from different types of waste sand to know the environmental impacts of all types of municipal waste. This course will discuss the overall scenario of E-Waste managementin India in comparison with other countries around the globe. This course will deals with E-waste legislation and government regulations on E-waste management.

II COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites
B.Tech	AHS009	П	Environmental Studies

III MARKS DISTRIBUTION:

Subject	SEE Examination	CIE Examination	Total Marks
WASTE TO ENERGY	70 Marks	30 Marks	100

IV DELIVERY / INSTRUCTIONAL METHODOLOGIES:

1	Power Point	1	Chalk & Talk	х	Assignments	х	MOOC
	Presentations						
x	Open Ended Experiments	~	Seminars	x	Mini Project	X	Videos
x	Others						

V EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

Semester End Examination (SEE): The SEE shall be conducted for 70 marks of 3 hours duration. The syllabus for the theory courses shall be divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern shall be as defined below.Two full questions with either or choice will be drawn from each unit. Each question carries 14 marks. There could be a maximum of three sub divisions in a question.

	_
50%	amp; To test the objectiveness of the concept
30%	amp; To test the analytical skill of the concept
20%	amp; To test the application skill of the
	concept

The emphasis on the questions is broadly based on the following criteria:

Continuous Internal Assessment (CIA):

For each theory course the CIA shall be conducted by the faculty/teacher handling the course as given in Table 4. CIA is conducted for a total of 30 marks, with 25 marks for Continuous Internal Examination (CIE) and 05 marks for Technical Seminar and Term Paper.

Component	Theory		Total Marks
Type of Assessment	CIE Exam Technical Seminar and Term Paper		
CIA Marks	25	5	30

Continuous Internal Examination (CIE):

Two CIE exams shall be conducted at the end of the 9th and 17th week of the semesterrespectively. The CIE exam is conducted for 25 marks of 2 hours duration, consisting of 5 one mark compulsory questions in part-A and 4 questions in part-B. The student has to answer any 4 questions out of five questions, each carrying 5 marks. Marks are awarded by taking average of marks scored in two CIE exams. **Technical Seminar and Term Paper:**

Two seminar presentations are conducted during I year I semester and II semester. For seminar, a student under the supervision of a concerned faculty member, shall identify a topic in each course and prepare the term paper with overview of topic. The evaluation of Technical seminar and term paper is for maximum of 5 marks. Marks are awarded by taking average of marks scored in two Seminar Evaluations.

VI COURSE OBJECTIVES:

The students will try to learn:

1	The principles of solid waste management in reducing and eliminating dangerous impacts of waste materials on human health and the environment to contribute economic development and superior quality of life.
II	The insight of the design and operations of a municipal solid waste landfill by collection, transfer and transportation of municipal solid waste for the final disposal.

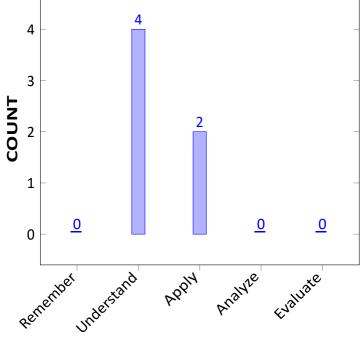
	The main operational challenges in operating thermal and biochemical energy from waste facilities and device processes involved in recovering energy from wastes.
IV	The scenario of E-Waste management in India and other countries around the globe and assess the impact of electronic waste on human, environment and society by informal recycling and management. The sustainable solution of E-Waste Management can be achieved by adopting modern techniques and Life-Cycle Analysis approach.

VII COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	Identify the different sources and types of solid waste by the properties of municipal solid waste for segregation and collection of waste.	Apply
CO 2	Explain the energy generation technologies from waste treatment plants and disposal of solid waste by aerobic composting and incineration process.	Understand
CO 3	Explain the classification, preliminary design considerations of landfill and methods of landfill disposal of solid to control greenhouse gases.	Understand
CO 4	Understand the Composition, characteristics of leachate to control the emission of gases by monitoring the movement of landfill leachate.	Understand
CO 5	Outline the Biochemical conversion of biomass for energy generation by anaerobic digestion of solid waste.	Understand
CO 6	Apply the knowledge in planning and operations of waste to Energy plants by following legal legislation related to solid waste management.	Apply

COURSE KNOWLEDGE COMPETENCY LEVEL



BLOOMS TAXONOMY

VIII HOW PROGRAM OUTCOMES ARE ASSESSED:

	Program	Strength	Proficiency Assessed by
PO 1	Independently carry out research / investigation and development work to solve practical problems.	2	CIE/SEE/AAT
PO 2	Write and present a substantial technical report / document.	1	CIE/SEE/AAT
PO 3	Demonstrate the importance of embedded technologies and design newinnovative products for solving society relevant problems	2	CIE/SEE/AAT
PO 5	Independently carry out research / investigation and development work tosolve practical problems.	2	CIE/SEE/AAT
PO 6	Recognize the need to engage in lifelong learning through continuing education and research.	2	CIE/SEE/AAT

3 = High; 2 = Medium; 1 = Low

IX MAPPING OF EACH CO WITH PO(s):

COURSE		PROGRAM OUTCOMES						
OUTCOMES	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6		
CO 1	1	1	-	-	1	✓		
CO 2	-	1	-	-	-	-		
CO 3	-	1	-	-	-	✓		
CO 4	-	1	-	-	-	1		
CO 5	1	-	-	-	-	-		
CO 6	-	-	1	-	-	-		

X JUSTIFICATIONS FOR CO – (PO) MAPPING -DIRECT:

COURSE OUTCOMES	PO'S PSO'S	Justification for mapping (Students will be able to)	No. of Key Competencies
CO 1	PO 2	List out the different sources, types of municipal solid waste by considering environmental limitations, health, safety and risk assessment issues for waste segregation, operation and maintenance	2
	PO 6	Apply the knowledge of management techniques by understanding the requirement for engineering activities of municipal solid waste for the sustainable development .	3
CO 2	PO 1	Apply the Scientific principles for energy generation by applying different technologies from waste management plants.	1
	PO 2	Identify the constraints including environmental health and safety and risk assessment issues of different methods of disposal of municipal solid waste by aerobic composting to promote sustainable development.	2
CO 3	PO 2	Understand customer and user needs considerations such as aesthetics by disposal of solid waste in land fill sites and identify constraints including environmental and sustainability suitability.	2
	PO 6	Understand the commercial and economic context of landfill layout and preliminary design as per environmental laws to safeguard the personnel, health, safety, and risk (including environmental risk) issues	2
CO 4	PO 2	Identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues for environmental monitoring system of land fill gases and composition of leachate and Understanding commercial and economic context of managing the land fill site	2
	PO 6	Understand the characteristics, generation and movement of leachate in landfills by the management techniques which uses for controlling the emission of gases in landfills to promote sustainable development	2
CO 5	PO 1	Explain the Scientific principles for Energy generation from waste bio-chemical conversion and to integrate / support the engineering disciplines	2

CO 6	PO 6	Apply the knowledge in planning and operations of waste to Energy plants for sustainable	3
		development by following legal legislation related to solid waste management for high level of professional and ethical values.	

XI TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO) MAPPING:

COURSE			Program Ou	utcomes/		
OUTCOMES		No. d	of Key Compe	tencies Ma	tched	
OUTCOMES	1	2	3	4	5	6
CO 1	2	3	-	-	4	4
CO 2	-	3	-	-	-	-
CO 3	-	3	-	-	-	4
CO 4	-	3	-	-	-	8
CO 5	3	-	-	-	-	-
CO 6	-	-	5	-	-	-

XII PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO):

COURSE	PROGRAM OUTCOMES						
OUTCOMES	1	2	3	4	5	6	
CO 1	33.3	50	-	-	50	50	
CO 2	-	50	-	-	-	-	
CO 3	-	50	-	-	-	50	
CO 4	-	50	-	-	-	100	
CO 5	50	-	_	-	-	-	
CO 6	-	-	50	-	-	-	

XIII COURSE ARTICULATION MATRIX (PO mapping):

CO'S and PO'S and CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

- **0** $0 \le C \le 5\%$ No correlation
- **2** 40 % <C < 60% –Moderate
- **1-5** <C≤ 40% Low/ Slight
- **3** 60% \leq C < 100% Substantial /High

COURSE	PROGRAM OUTCOMES					
OUTCOMES	1	2	3	4	5	6
CO 1	1	2	-	-	2	2
CO 2	-	2	-	-	-	-
CO 3	-	2	-	-	-	2
CO 4	-	2	-	-	-	3
CO 5	2	-	-	-	-	-
CO 6	-	-	2	-	-	-
TOTAL	3	8	-	-	2	7
AVERAGE	1.5	2	2	-	2	2.3

XIV ASSESSMENT METHODOLOGY DIRECT:

CIE Exams	1	SEE Exams	1	Assignments	-
Quiz	-	Tech - Talk	-	Certification	-
Term Paper	1	Seminars	1	Student Viva	-
Laboratory Practices	-	5 Minutes Video / Concept Video	-	Open Ended Experiments	-
Micro Projects	-	-	-	-	-

XV SYLLABUS:

MODULE I	INTRODUCTION TO ENERGY FROM WASTE
	Introduction to Energy from Waste: Classification of waste as fuel, Agro based, Forest residue, Industrial waste. MSW, Conversion devices. Incinerators, gasifiers, digestors
MODULE II	BIOMASS PYROLYSIS
	Biomass Pyrolysis: Pyrolysis, Types, slow fast , Manufacture of charcoal, Methods, Yields and application, Manufacture of pyrolytic oils and gases, yields and applications.
MODULE III	BIOMASS GASIFICATION
	Gasifiers, Fixed bed system, Downdraft and updraft gasifiers, Fluidized bed gasifiers, Design, construction and operation. Gasifier burner arrangement for thermal heating. Gasifier engine arrangement and electrical power, Equilibrium and kinetic consideration in gasifier operation.
MODULE IV	BIOMASS COMBUSTION
	Biomass stoves, Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.
MODULE V	BIOGAS
	Properties of biogas (Calorific value and composition), Biogas plant technology and status, Bio energy system. Design and constructional features, Biomass resources and their classification, Biomass conversion processes, Thermo chemical conversion, Direct combustion, biomass gasification, pyrolysis and liquefaction, biochemical conversion, anaerobic digestion. Types of biogas Plants, Applications. Alcohol production from biomass, Bio diesel production. Urban waste to energy conversion, Biomass energy programme in India.

TEXTBOOKS

- 1. Nicholas P Cheremisinoff, —Handbook of Solid Waste Management and Waste Minimization Technologies , An Imprint of Elsevier, New Delhi, 2003.
- 2. P AarneVesilind, William A Worrell and Debra R Reinhart, —Solid Waste Engineering, 2 nd edition 2002.
- 3. M Dutta , B P Parida, B K Guha and T R Surkrishnan, —Industrial Solid Waste Management and Landfilling practice , Reprint Edition New Delhi, 1999.
- 4. RajyaSabha Secretariat, —E-waste in India: Research unit, Reprint Edition, June, 2011.

REFERENCE BOOKS:

- 1. C Parker and T Roberts (Ed), —Energy from Waste, An Evaluation of Conversion Technologies, Elsevier Applied Science, London, 1985.
- 2. KL Shah,"Basics of Solid and Hazardous Waste Management Technology", Prentice Hall, Reprint Edition, 2000.
- 3. M Datta, —"Waste Disposal in Engineered Landfill", Narosa Publishing House, 1997.

XVI COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

S.No	Topics to be covered	CO's	Reference T1: 4.1
1	Summarize about solid waste sources and its importance.	CO 1	T1:3.3, T2:1.2, R2: 2.2
2	Discuss solid waste properties and its composition.	CO 1	T1:3.4, T2:1.4
3	Provides the information regarding collection and transfer of solid waste.	CO 1	T1:3.5 <i>,</i> R2:1.5
4	Discuss the need of waste minimization and recycling	CO 1	T1:3.7, R2:1.8
5	Discuss the need of segregating waste and managing solid waste.	CO 2	T1: 3.9, R3: 1.10
6	Acquire the knowledge about the technologies for generation of energy from solid waste.	CO 2	T1:5.5, T2:6.2, R3:4.8
7	Acquire the knowledge about the technologies for generation of energy from biomedical waste.	CO 2	T1:5.6, T2:6.3, R3:7.5
8	Discuss the environmental impacts of incineration process.	CO 2	T1:4.3, T2:5.2, R2: 5.7
9	Illustrate the importance of landfill method of disposal.	CO 3	T1: 4.4, R1:3.3
10	Discuss the types of land fill disposal and classification of land fill sites.	CO 3	T1:4.5, T2: 5.4, R3: 7.3
11	Analyze the layout and preliminary design of landfills.	CO 3	T1:4.6 <i>,</i> T2:5.5
12	Summarize the properties and characteristics of landfills.	CO 4	T1: 4.5.2., T2: 5.6
13	Acquire the knowledge of generating energy from landfills.	CO 4	T1:4.6 <i>,</i> T2:5.5
14	Discuss the emission of gasses and leach ate from landfills.	CO 4	T1:4.6.2, T2:5.5.2

	T		
15	Discuss the environmental monitoring system for land fill gases.	CO 4	T1:4.7, T2:5.6
16	Discuss about the biochemical conversion and their advantages.	CO 5	T1:4.7 <i>,</i> T2:5.8
17	Illustrate the sources of biochemical conversion process.	CO 5	T1:4.7.2, T2:5.8.2
18	Analyze anaerobic digestion of sewage and municipal waste.	CO 5	T1:4.8 <i>,</i> T2:5.9
19	Analyze direct combustion of Municipal solid waste.	CO 6	T1:4.9 <i>,</i> T2:5.7
20	Discuss about refuse derived solid fuel and their importance in energy generation.	CO 6	T1:6.2 <i>,</i> T2:5.6
21	Discuss about industrial waste and agro residues.	CO 6	T1:6.3, T2:5.7
22	Understand the concept of Thermo-chemical Conversion.	CO 7	T1:6.4, T2:5.8
23	Discuss about Biogas production and generation of energy by Biogas.	CO 7	T1:6.5 <i>,</i> T2:5.3
24	Explain the land fill gas generation and utilization of landfill gas for various purposes.	CO 7	T1:66, T2:5.2
25	Illustrate sources of thermo chemical energy generation	CO 8	T1:6.7, T2:5.3
26	Explain gasification of waste using gasifies briquetting process.	CO 8	T1:6.5 <i>,</i> T2:7.5
27	Discuss utilization of various municipal solid wastes by recycling, refuse and reuse techniques.	CO 8	T1: 6.2, 6.3, R2: 7.9
28	Discuss advantages and disadvantages of briquetting process.	CO 8	T1: 6.2
29	Summarize environmental benefits of bio-chemical conversion	CO 8	T1:6.2, T2:7.2
30	Summarize environmental benefits of thermo- chemical conversion	CO 8	T1:6.3, T2:7.3
31	Outline the Growth of electrical and electronics industry in India.	CO 9	T1:6.4, T2:7.5
32	Summarize the E-waste generation in India and in the global context.	CO 9	T1: 6.2, T2: 5.6
33	Understand the Growth of E waste generated from electrical and electronics industry in India	CO 9	T1:6.3, T2: 5.7
34	Identify environmental concerns and health hazards	CO 9	T1:6.4, T2:5.8
35	Determine recycling concept of E-Waste and advantages of E-waste.	CO 9	T1:2.1, T2:9.1
36	Discuss A thriving economy of the unorganized sector of E-waste	CO 9	T1:2.2, T2:9.2
37	Discuss the global trade in hazardous waste and their impact on the environment	CO 9	T1: 2.1, R2: 9.1

38	Discuss impact of hazardous E-waste in India and effects on human health	CO 9	T1:2.6, R1:5.1
39	Understand the management processes of E-waste and the importance of formal recycling of E-waste	CO 10	T1:2.7, R1:5.2
40	Outline E-waste legislation for the recycling and disposal	CO 10	T1:2.8, R1:5.5
41	Summarize government regulations on E-waste management	CO 10	T1:2.1 <i>,</i> R1:5.6
42	Outline international E-waste management and the guidelines imposed for formal disposal	CO 10	T1:2.2 <i>,</i> R1:5.4
43	Explain the need for stringent health safeguards of human health and their effects	CO 10	T1:2.4,R1:5
44	Discuss the need for environmental protection laws and	CO 10	T1:2.4 <i>,</i> R1:5.5
45	Outline environmental protection laws of India with respect to E-waste management.	CO 10	T1:2.4 <i>,</i> R1:5.5

Signature of Course Coordinator

HOD,ECE