INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

INFORMATION TECHNOLOGY

ATTAINMENT OF COURSE OUTCOME – ACTION TAKEN REPORT

Name of the faculty:	**Ms. G. Bhavana**	Department:	**IT**
Regulation:	**IARE - R16**	Batch:	**2016-2020**
Course Name:	**Digital Logic Design**	Course Code:	**AEC020**
Semester:	**III**	Target Value:	**50% (1.8)**

Attainment of COs:

Course Outcome		Direct attainment	Indirect attainment	Overall attainment	Observation
CO1	Understand the different forms of number representations and binary codes in digital logic circuits.	0.9	2.4	1.2	Attainment target is not yet reached.
CO2	Make use of Boolean postulates, theorems and k-map for obtaining minimized Boolean expressions.	0.9	2.4	1.2	Attainment target is not yet reached.
CO3	Implement the combinational logic circuits using the logic gates.	0.9	2.4	1.2	Attainment target is not yet reached.
CO4	Utilize the functionality and characteristics of flip-flops and latches for designing sequential circuits.	1.6	2.4	1.8	Attainment target reached.
CO5	Construct the synchronous and asynchronous modules using flip-flops used for memory storing applications.	1.6	2.4	1.8	Attainment target is not yet reached.
CO6	Extend the knowledge of memories and programmable logic devices for understanding the architectural blocks of FPGA	0.9	2.4	1.2	Attainment target is not yet reached.

Action taken report: (To be filled by the concerned faculty / course coordinator)

CO 1: Need to provide more related topic Examples.

CO 2: Extend the topics clear and give the Examples.

CO 3: Need to provide more Concepts and assignments.

CO 6: Need to provide more problems and also additional digital resources which enables the students to gain more problem-solving skills.

G. Bhavana

Course Coordinator

Mentor

HOD