INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

INFORMATION TECHNOLOGY

ATTAINMENT OF COURSE OUTCOME – ACTION TAKEN REPORT

Name of the faculty:	**Ms. G. Bhavana**	Department:	**IT**
Regulation:	**IARE - R16**	Batch:	**2017-2021**
Course Name:	**Digital Logic Design LAB**	Course Code:	**AEC116**
Semester:	**III**	Target Value:	**81% (1.8)**

Attainment of COs:

Course Outcome		Overall attainment	Observation
CO1	Identify the functionality of Booean expression using logic gates such as and, or, not, nand, nor, xor and xnor gates.	2.4	Attainment target reached.
CO2	Build combinational circuits such as adder,subtractor,multiplexers and comparators realization using low level elementary blocks.	2.4	Attainment target reached.
CO3	Analyze the operation of medium complexity standard combinational circuits like the code converters used to minimize the boolean expressions.	2.4	Attainment target reached.
CO4	Analyze the operation of a flip-flop and examine relevant timing diagrams	2.4	Attainment target reached.
CO5	Design complex digital system such as ALU to perform arithmetic and bitwise opeartors.	2.4	Attainment target reached.
CO6	Build the universal shift registers, counters using the flip flops..	2.4	Attainment target reached.

Action taken report: (To be filled by the concerned faculty / course coordinator)
All CO's are attained

Course Coordinator **Mentor** **HOD**