SYSTEM ON CHIP ARCHITECTURE

II Semester: ECE(ES)								
Course Code	**Category**	**Hours / Week**			**Credits**	**Maximum Marks**		
BESC21	**ELECTIVE**	**L**	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
		3	0	0	3	30	70	100
Contact Classes: 45	**Tutorial Classes: Nil**	**Practical Classes: Nil**				**Total Classes: 45**		

I. COURSE OVERVIEW:

This course provides the basic knowledge on design, programming of system and processor architecture. It includes memory designing, interconnect customization and configuration, SOC Design approach, AES algorithms, image compression. It provides skills for embedded systems and mobile computing applications, on-chip memories and communication networks, I/O interfacing, RTL design of accelerators.

II. COURSE OBJECTIVES:

The students will try to learn:

I. The system on chip fundamentals and their applications.
II. The various computation models of SOCs and basic concepts of processor architecture and instructions.
III. The SOC customization and reconfiguration technologies and external, internal memory of SOC.
IV. The SOC Design approach for design and evaluation of Image compression.

III. COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO1	Recall the knowledge of all the components required for SOC Design and System Architecture.	Remember
CO2	Interpret the basic elements and architectures required for different types of processors.	Understand
CO 3	Design SOC internal and external memory for interpreting different memory architectures.	Apply
CO 4	Develop the analytical skill for deciding the type of processor required to design the desired application SoC.	Apply
CO 5	Classify the types and applications of different memory devices using SOC design concept.	Understand
CO 6	Analyze different types of interconnect buses required for different applications.	Analyze

IV. SYLLABUS:

MODULE – I:INTRODUCTION TO THE SYSTEM APPROACH (9)

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

MODULE – II:PROCESSORS(9)

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

MODULE – III: MEMORY DESIGN FOR SOC(9)

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache

Organization, Cache data, Write Policies, Strategies for line replacement at miss time.

Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

MODULE – IV: INTERCONNECT CUSTOMIZATION AND CONFIGURATION(9)

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance Specific design, Customizable Soft Processor, Reconfiguration – overhead analysis and trade-off analysis on reconfigurable Parallelism.

MODULE – V: APPLICATION STUDIES / CASE STUDIES(9)

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

V. TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiley India Pvt. Ltd.
2. Steve Furber, "ARM System on Chip Architecture ", 2nd Edition, 2000, Addison Wesley Professional

VI. REFERENCE BOOKS:

1. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st Edition, 2004, Springer
2. Jason Andrews, "Co-Verification of Hardware and Software for ARM System on Chip Design Embedded Technology)", Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2001, Kluwer Academic Publishers.

VII. WEB REFERENCES:

1. www.edufind.com

VIII. E-TEXT BOOKS:

1. https://www.ele.uva.es/~jesman/BigSeti/ftp/Microcontroladores/ARM/Arm%20System-OnChip%20Architecture. pdf
2. https://www.intechopen.com/chapters/53952.