Hall Ticket No | | | | | | | | | | |

Question Paper Code: AECB07

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER - I

B.Tech III Semester End Examinations, November - 2019

Regulation: IARE-R18

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max Marks: 70**

Answer any ONE question from each Unit
All questions carry equal marks
All parts of the question must be answered in one place only

UNIT – I

1	a)	Convert the following Hexadecimal numbers to their Decimal equivalent numbers. i) 785.56 ii) EAF1 iii) 550	[7M]
	b)	Perform the following Subtraction using 2's complement. i) 15-17 ii) 25-13 iii) 55-10	[7M]
2	a)	Given the 8-bit data word 01011011, generate the 12-bit composite word for the hamming code that corrects and detects single errors.	[7M]
	b)	Perform the following addition using excess-3 code. i) 386+756 ii) 1010 + 444 iii) 0110 + 324	[7M]

UNIT – II

3	a)	State and prove the following Boolean laws. i) Associative law ii) Distributive law	[7M]
	b)	Define K-map and minimize the following function using 4 variables K-map. F (A, B, C, D) = Σm (1,3,5,7,9,10,11,12,15)	[7M]
4	a)	Design a 3 bit gray code to binary code converter using logic gates and universal gates?	[7M]
	b)	Implement full adder using two half adders and one OR gate and also construct full adder using decoder and OR gates?	[7M]

UNIT – III

5	a)	Define JK – Flip-flop with the help of a logic diagram and characteristic table?	[7M]
	b)	Draw the logic diagram of a SR latch using NOR gates. Explain its operation using excitation table.	[7M]

6	a)	Design a 3-bit synchronous down counter using T flip-flops and state the flow of sequence using excitation table?	[7M]
	b)	Design a 3bit up/down counter which counts up when the control signal M=1 and counts down when control signal M=0?	[7M]

UNIT – IV

7	a)	Explain about p-channel and n-channel MOS transistor operation.	[7M]
	b)	Explain why the number of CMOS inputs connected to the output of a CMOS gate generally is not limited by DC fanout considerations with example.	[7M]
8	a)	Write about CMOS circuits steady state electrical behavior.	[7M]
	b)	Realize the CMOS NAND gate in transistor level using NOR gate circuit.	[7M]

UNIT – V

9	a)	Write about libraries and packages in VHDL programming.	[7M]
	b)	Write about primary differences between the various programming styles of VHDL language.	[7M]
10	a)	Explain the following giving requisite statements of VHDL: i) Transport delay ii) Inertial delay.	[7M]
	b)	Write a VHDL code for a full subtractor using logic equation.	[7M]

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COURSE OBJECTIVES

I	Understand common forms of number representation in logic circuits.
II	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
III	Understand the concepts of combinational logic circuits and sequential circuits.
IV	Understand the Realization of Logic Gates Using Diodes & Transistors.

COURSE OUTCOMES (COs):

CO 1	Understand the logic simplification and combinational logic design.
CO 2	Explore the MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU
CO 3	Understand the building blocks like FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts
CO 4	Understand the Logic Families And Semiconductor Memories
CO 5	Explore the VHDL Design entry and Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits

COURSE LEARNING OUTCOMES

AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.
AECB07.02	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
AECB07.03	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder
AECB07.05	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.
AECB07.06	Analyze Barrel shifter and ALU
AECB07.07	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
AECB07.08	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
AECB07.09	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
AECB07.10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB07.11	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB07.12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.
AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,
AECB07.14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.
AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL

AECB07.16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,
AECB07.17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNING OUTCOMES:

SEE Question No.		Course Learning Outcomes		Blooms Taxonomy Level
1	a	AECB07.02	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	Understand
	b	AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	Remember
2	a	AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	Understand
	b	AECB07.03	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	Remember
3	a	AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder	Remember
	b	AECB07.05	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.	Apply
4	a	AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	Remember
	b	AECB07.06	Analyze Barrel shifter and ALU.	Apply
5	a	AECB07.07	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.	Remember
	b	AECB07.08	Analyze and apply the design procedures of small sequential circuits to build the gated latches.	Apply
6	a	AECB07.09	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	Understand
	b	AECB07.10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	Apply
7	a	AECB07.12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.	Understand
	b	AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements.	Apply
8	a	AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements.	Remember
	b	AECB07.14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.	Apply
9	a	AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL.	Understand
	b	AECB07.16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling.	Understand
10	a	AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL.	Apply
	b	AECB07.17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	Apply

Signature of Course Coordinator **HOD, ECE**