LECTURE NOTES

ON

ELECTRONIC CIRCUITS

II B. Tech II semester (JNTUH-R15)

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ELECTRONICS AND COMMUNICATION ENGINEERING

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UNIT-I(a):
Single Stage Amplifiers Design And Analysis

Contents:

Introduction

What is Amplifier?

What is the need of an amplifier?

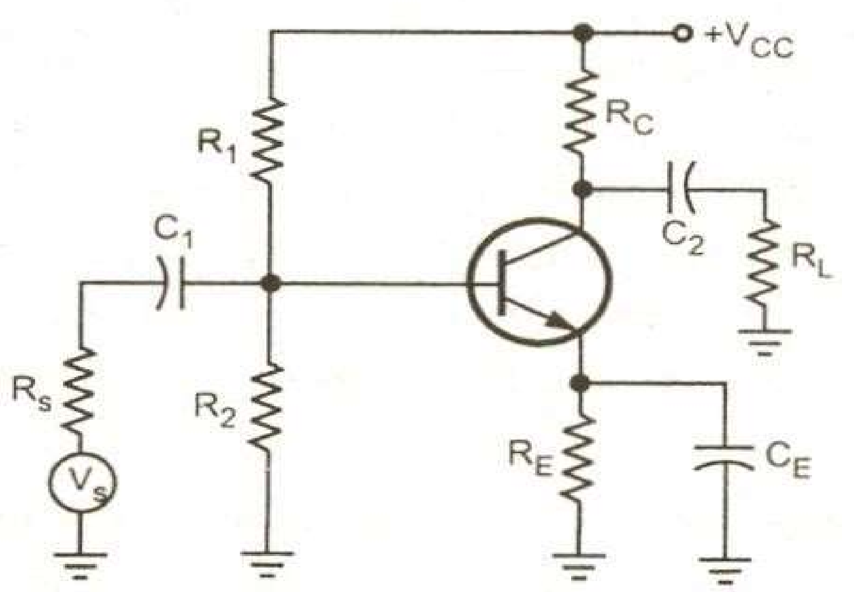
What are the applications of amplifier?

Transistor as an amplifier

- To make the transistor work as an amplifier, it is to be biased to operate in the active region.

- When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as "Single Stage Transistor Amplifier".

Components of an amplifier



CE Amplifier

Classification of amplifiers

Based on the active device.

- BJT Amplifier
- FET Amplifier

Based on the transistor configuration.

- Common Emitter amplifier
- Common Collector amplifier
- Common Base amplifier

Based on input.

- Small signal amplifiers
- Large signal amplifiers

Based on the output.

- Voltage amplifier
- Power amplifier

Based on the number of stages.

- Single stage amplifier
- Multistage amplifier

Based on the Q-point (Operating conduction)

- Class A Amplifier
- Class B Amplifier
- Class AB Amplifier
- Class C Amplifier

Based on the frequency response.

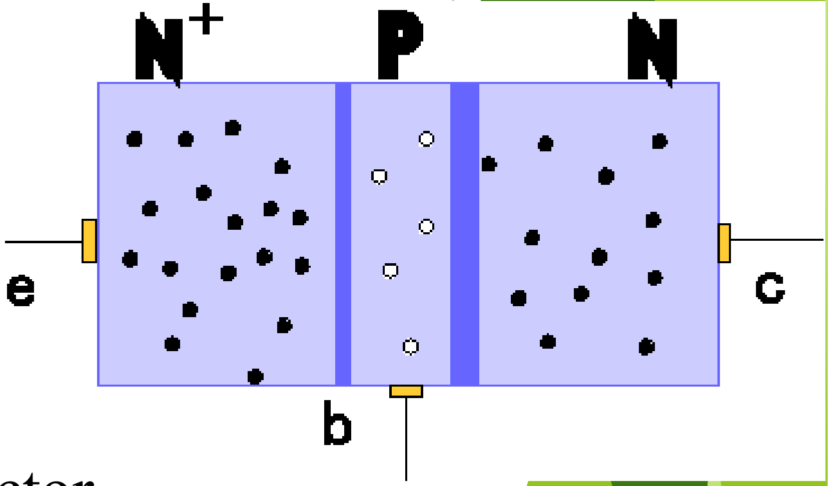
- Audio frequency amplifier
- Intermediate frequency amplifier
- Radio frequency amplifier

Based on the bandwidth.

- Narrow band amplifier
- Wide band amplifier

Bipolar junction transistors (BJTs)

Construction of Bipolar junction transistors

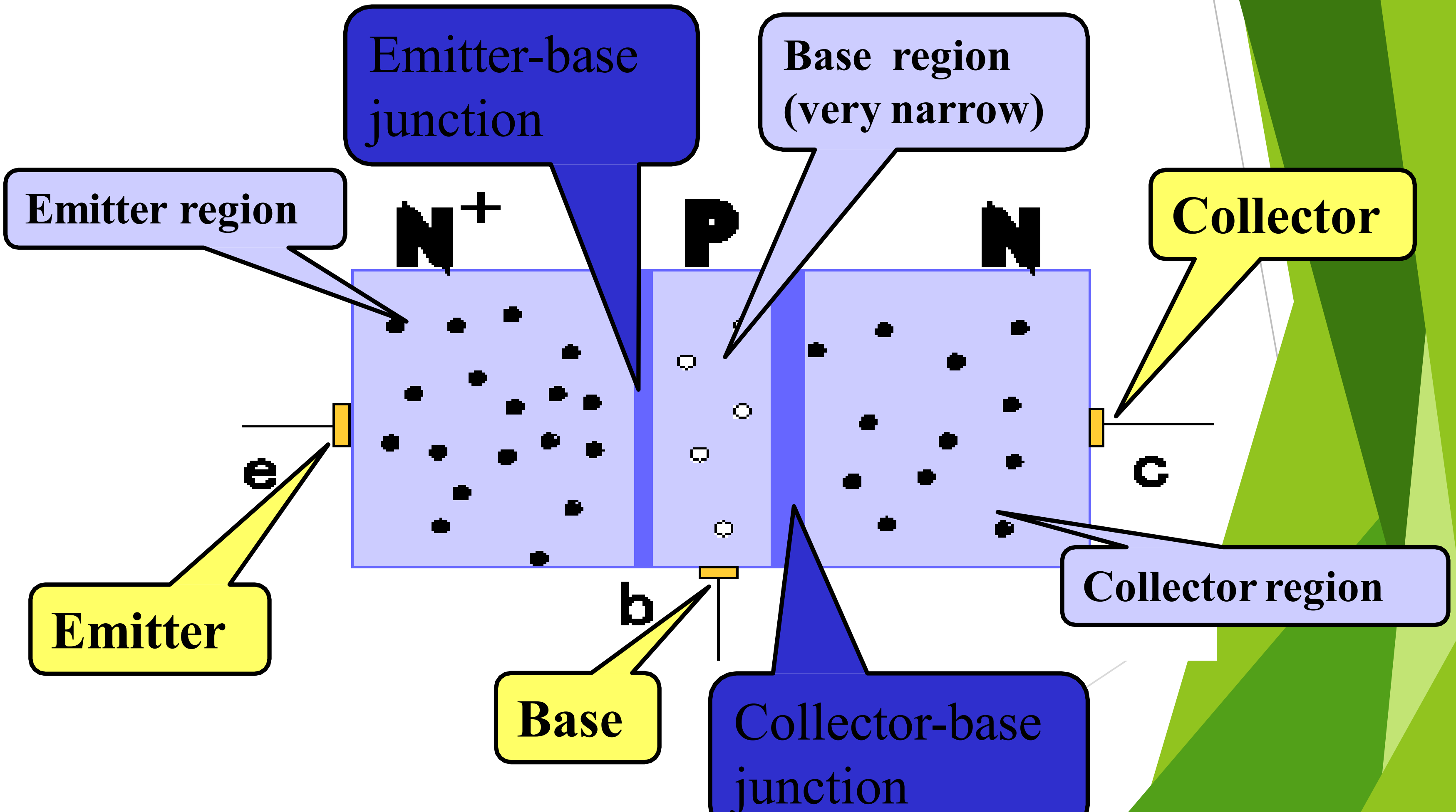


NPN BJT shown

- 3 terminals: emitter, base, and collector
- 2 junctions: emitter-base junction (EBJ) and collector-base junction (CBJ)
  - These junctions have capacitance (high-frequency model)
- BJTs are not symmetric devices
  - doping and physical dimensions are different for emitter and collector

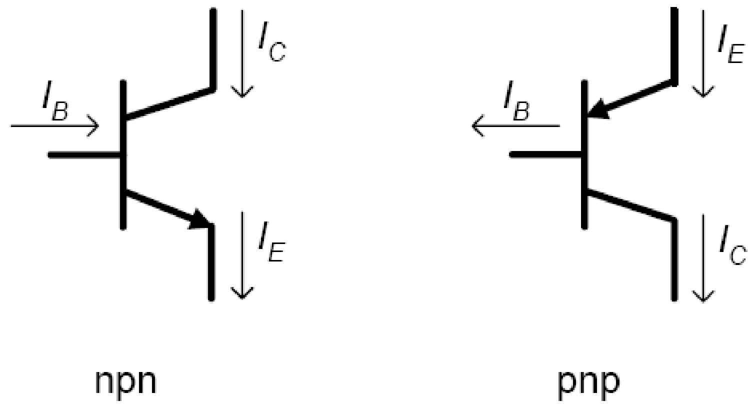
Bipolar junction transistors (BJTs)

Construction of Bipolar junction transistors



6.1 Bipolar junction transistors (BJTs)

Standard bipolar junction transistor symbols

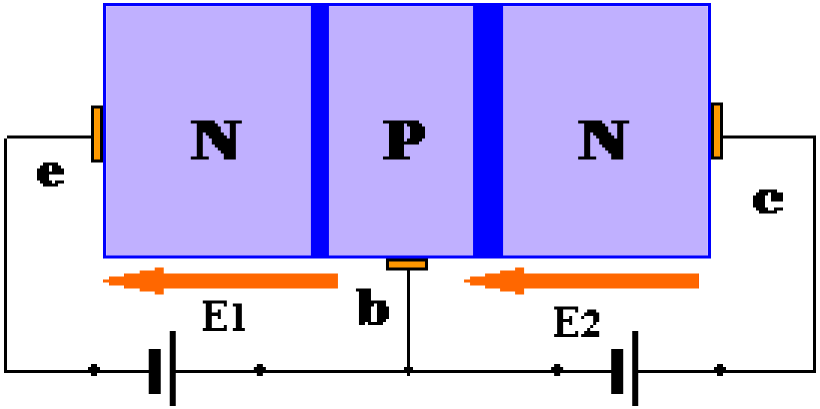


Depending on the biasing across each of the junctions, different modes of operation are obtained – cutoff, active and saturation

MODE	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

Bipolar junction transistors (BJTs)

BJT in Active Mode



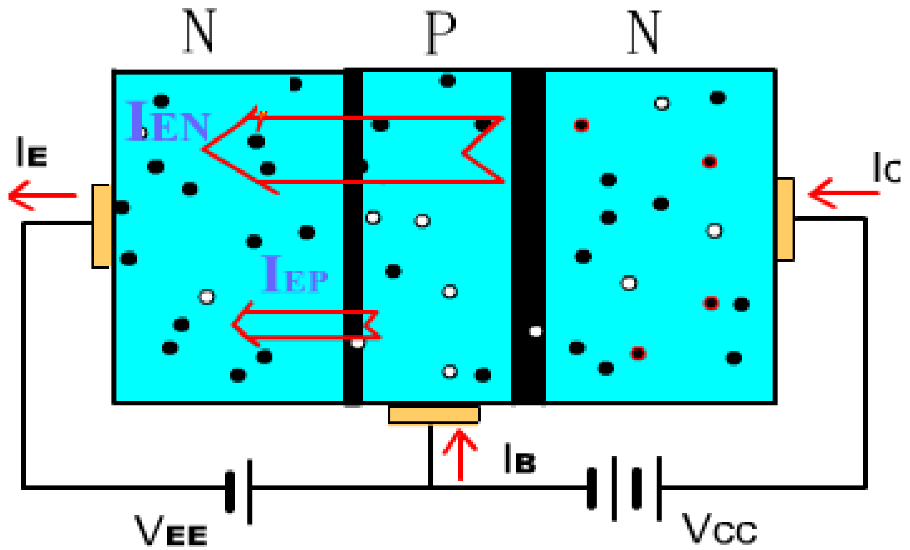
Two external voltage sources set the bias conditions for active mode

– EBJ is **forward biased** and CBJ is **reverse biased**

Bipolar junction transistors (BJTs)

BJT in Active Mode

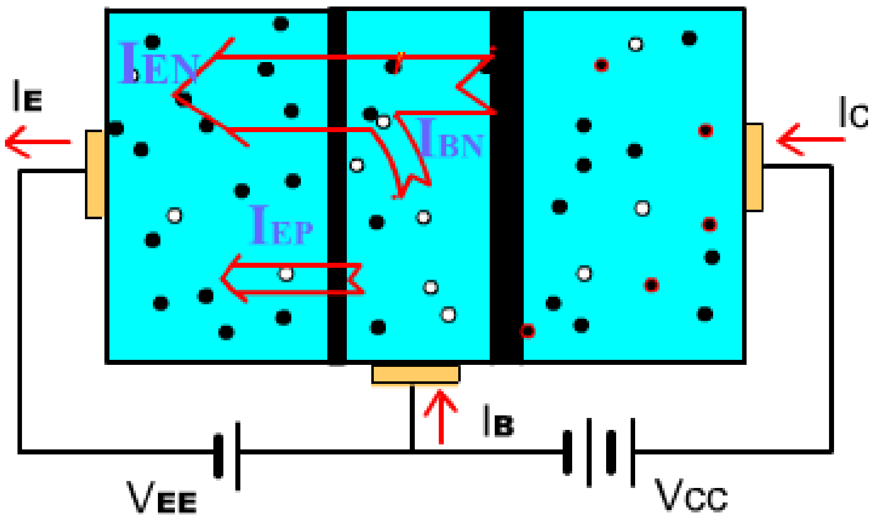
$$I_E = I_{EN} + I_{EP} \approx I_{EN}$$



Forward bias of EBJ injects electrons from emitter into base (small number of holes injected from base into emitter)

Bipolar junction transistors (BJTs)

BJT in Active Mode

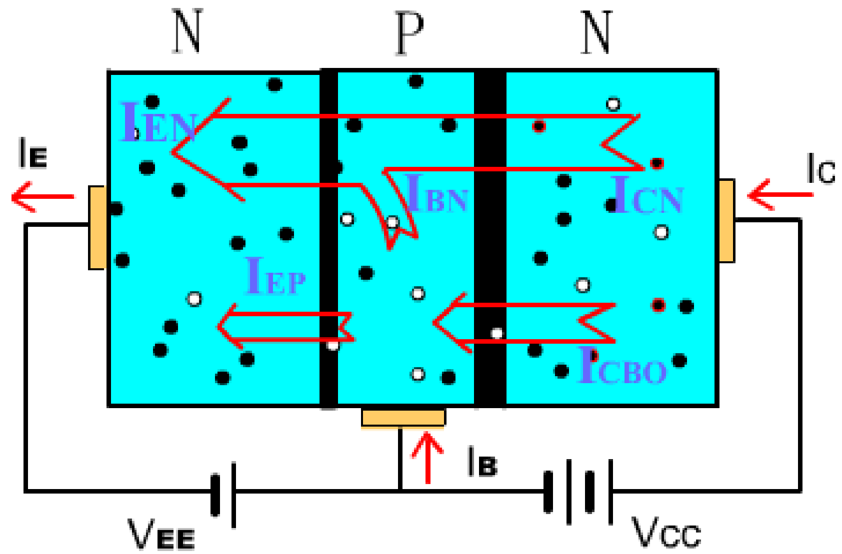


$$I_B = I_{BN} + I_{EP}$$

- Most electrons shoot through the base into the collector across the reverse bias junction
- Some electrons recombine with majority carrier in (P-type) base region

Bipolar junction transistors (BJTs)

BJT in Active Mode



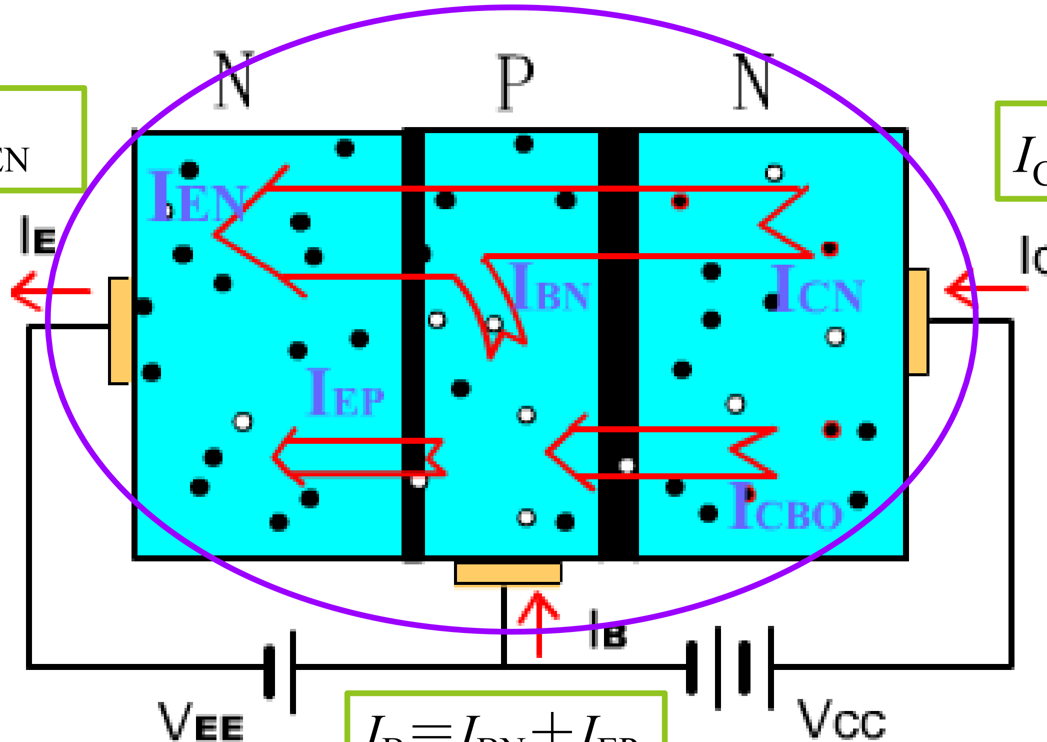
$$I_C = I_{CN} + I_{CBO}$$

Electrons that diffuse across the base to the CBJ junction are swept across the CBJ depletion region to the collector.

6.1 Bipolar junction transistors (BJTs)

BJT in Active Mode

$I_E = I_{EN} + I_{EP} \approx I_{EN}$



$I_C = I_{CN} + I_{CBO}$

$I_B = I_{BN} + I_{EP}$

$I_E = I_B + I_C$

Let $I_{CN} = \alpha I_E$

$I_C(1-\alpha) = \alpha I_B + I_{CBO}$

$\longrightarrow \alpha \approx \frac{I_C}{I_E}$ ---common-base current gain

Bipolar junction transistors (BJTs)

BJT in Active Mode

$\boxed{I_E = I_{EN} + I_{EP} \approx I_{EN}}$ $\boxed{I_B = I_{BN} + I_{EP}}$ $\boxed{I_C = I_{CN} + I_{CBO}}$ $\boxed{I_E = I_B + I_C}$

$$\alpha \approx \frac{I_C}{I_E} \longrightarrow I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\text{Let} \quad \beta = \frac{\alpha}{1-\alpha} \longrightarrow I_C = \beta I_B + (1+\beta) I_{CBO}$$

Beta: $\beta \approx \dfrac{I_C}{I_B}$ ---common-emitter current gain

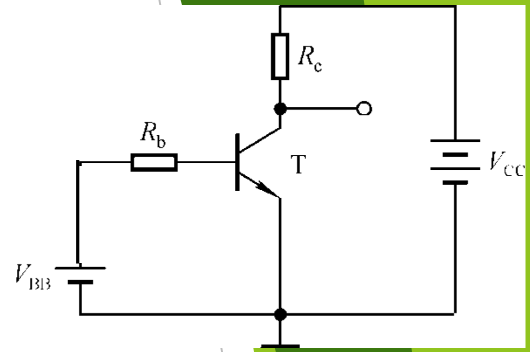
$$\begin{cases} I_E = I_C + I_B \approx (1+\beta) I_B \\ I_C = \beta I_B + I_{CEO} = \beta I_B \\ I_C = \alpha I_E \end{cases}$$

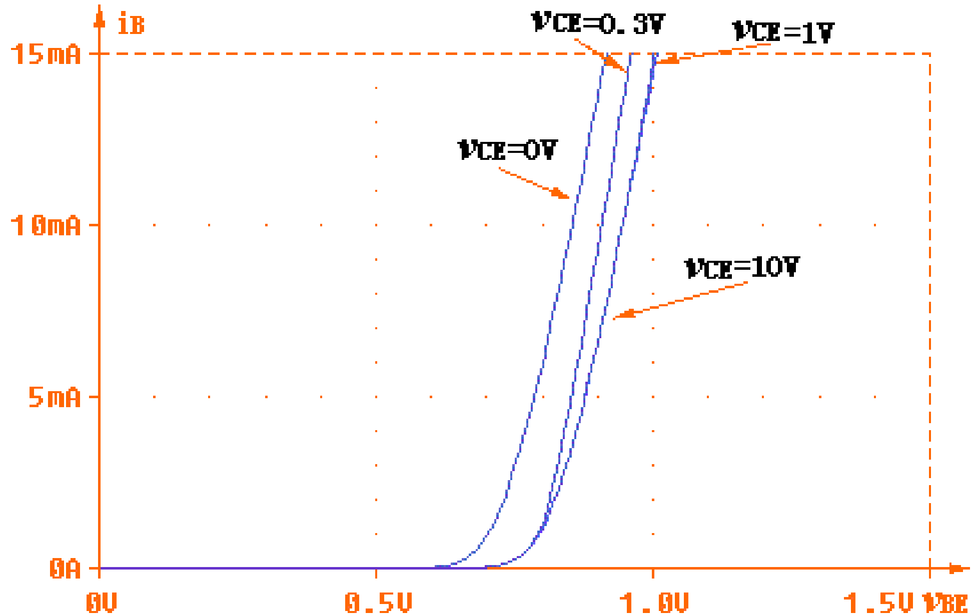
Bipolar junction transistors (BJTs)

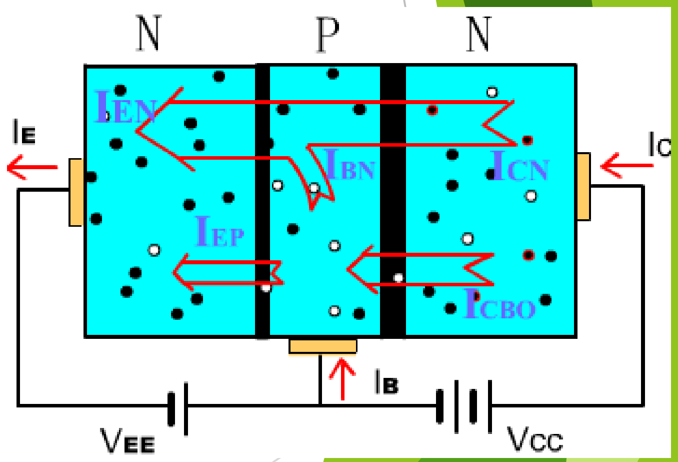
C-E Circuits I-V Characteristics

Base-emitter Characteristic(Input characteristic)

$$i_B = f(v_{BE})\ \Big|_{v_{CE=C}}$$



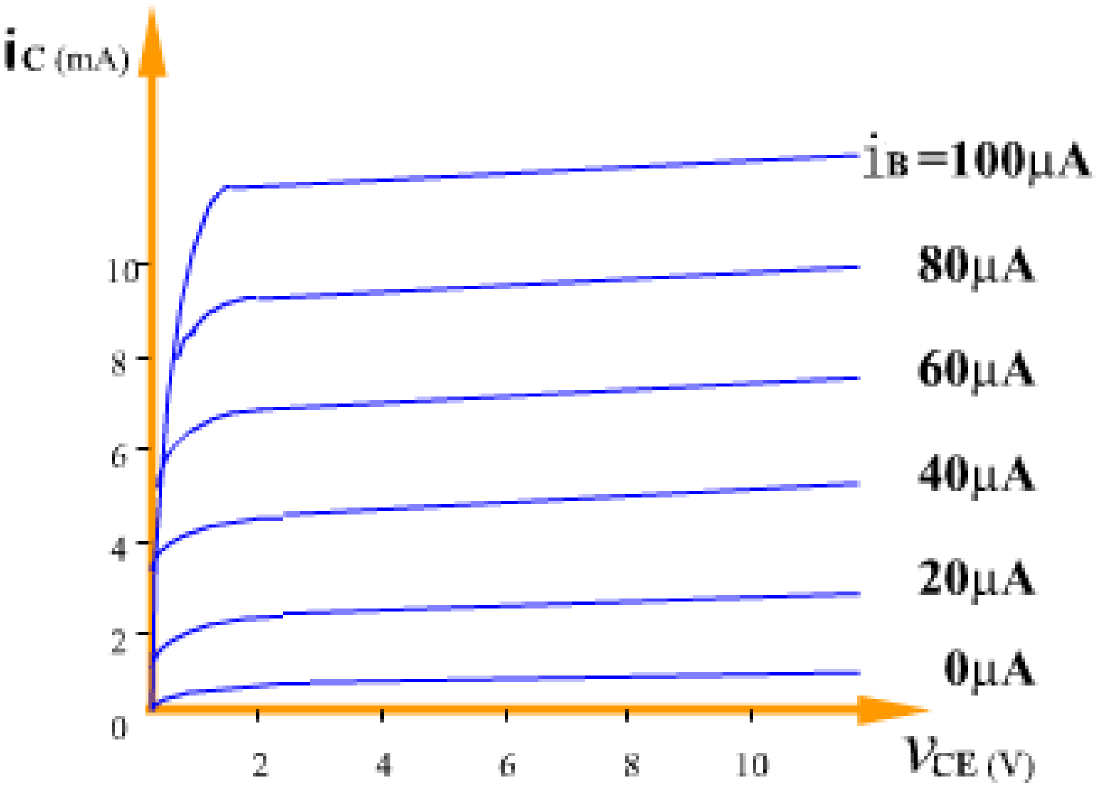




Bipolar junction transistors (BJTs)

C-E Circuits I-V Characteristics

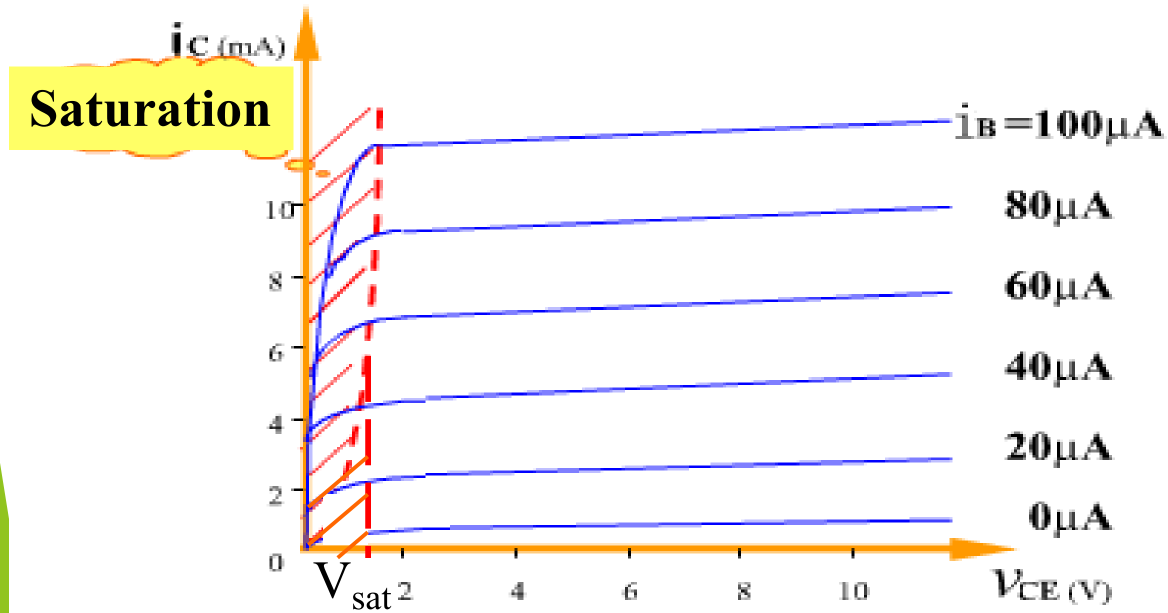
Collector characteristic (output characteristic) $i_C = f_{(V_{CE})}\Big|_{i_B=C}$

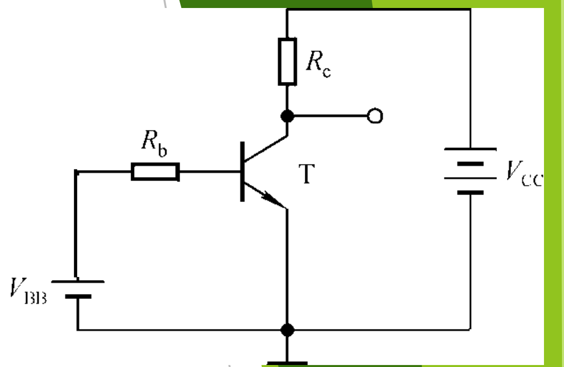


Bipolar junction transistors (BJTs)

C-E Circuits I-V Characteristics

Collector characteristic





Saturation occurs when the supply voltage, $V_{CC,}$ is across the total resistance of the collector circuit, R_C.

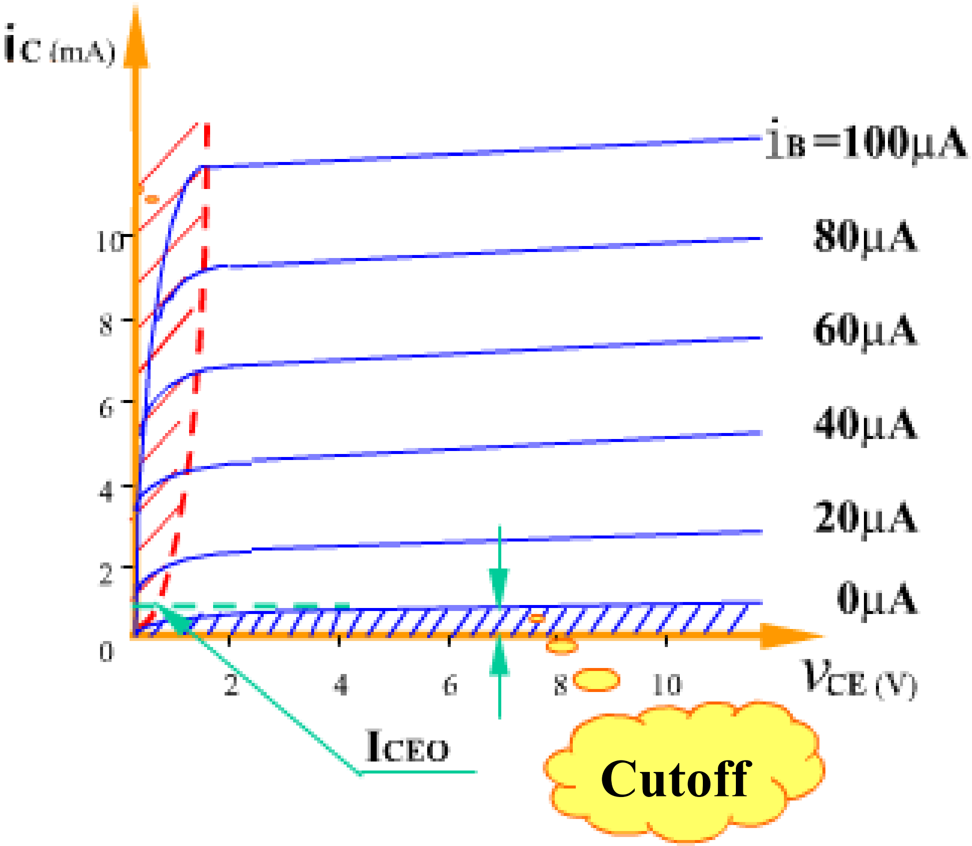
$$I_{C(sat)} = V_{CC}/R_C$$

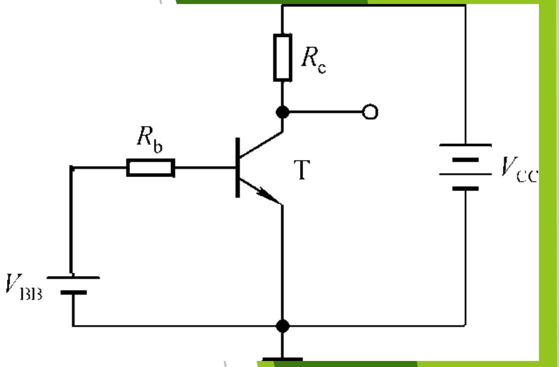
Once the base current is high enough to produce saturation, further increases in base current have no effect on the collector current and the relationship $I_C = \beta I_B$ is no longer valid. When V_{CE} reaches its saturation value, $V_{CE(sat)}$, the base-collector junction becomes forward-biased.

Bipolar junction transistors (BJTs)

C-E Circuits I-V Characteristics

Collector characteristic



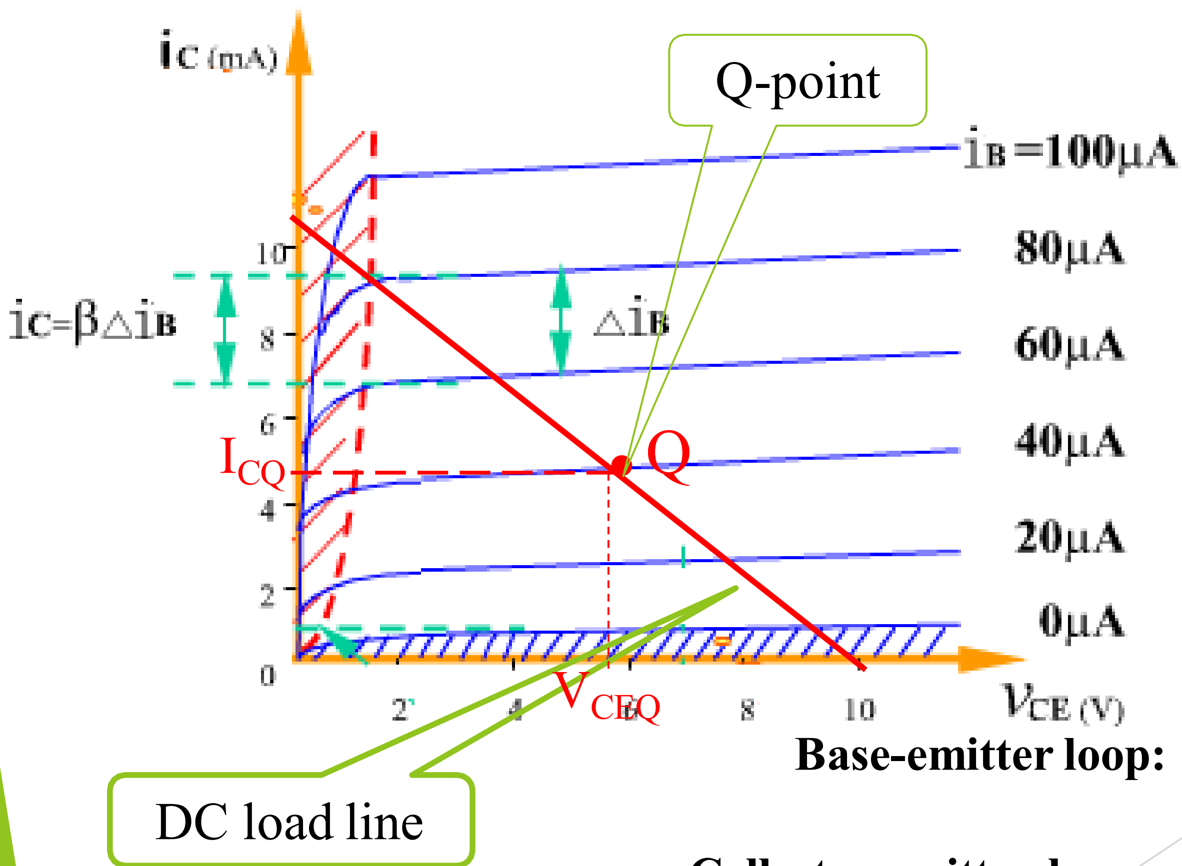


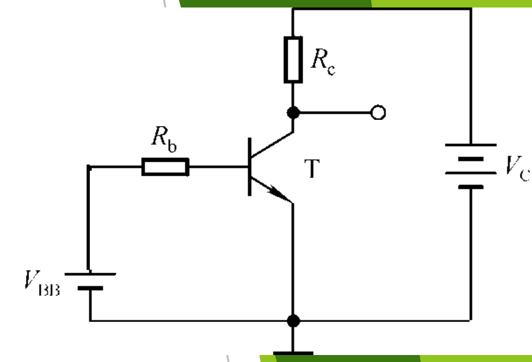
When $I_B = 0$, the transistor is in cutoff and there is essentially no collector current except for a very tiny amount of collector leakage current, I_{CEO}, which can usually be neglected. $I_C \approx 0$.

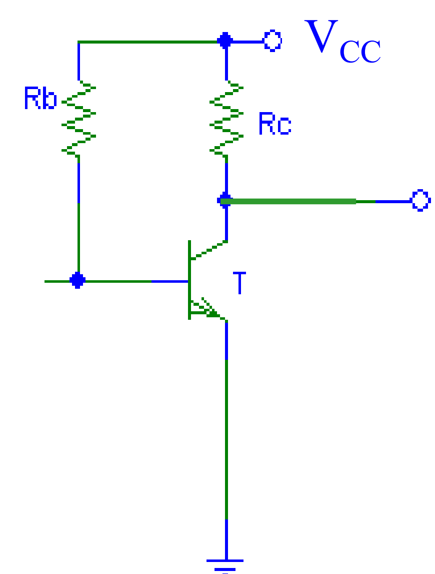
In cutoff both the base-emitter and the base-collector junctions are reverse-biased.

Bipolar junction transistors (BJTs)

DC Load Line and Quiescent Operation Point







Base-emitter loop: $I_B = \dfrac{V_{CC} - V_{BE}}{R_b} \approx \dfrac{V_{CC}}{R_b} = 40(\mu A)$

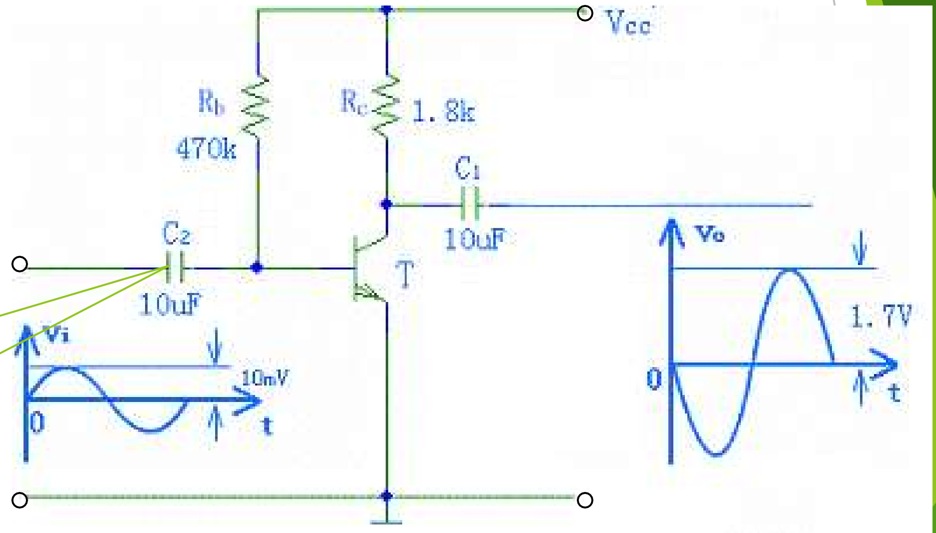
Collector-emitter loop: $v_{CE} = V_{CC} - i_C R_C = 10 - i_C \times 4k$

Single-Stage BJT Amplifiers

C-E Amplifiers

To operate as an amplifier, the BJT must be biased to operate in active mode and then superimpose a small voltage signal v_{be} to the base.

DC + small signal



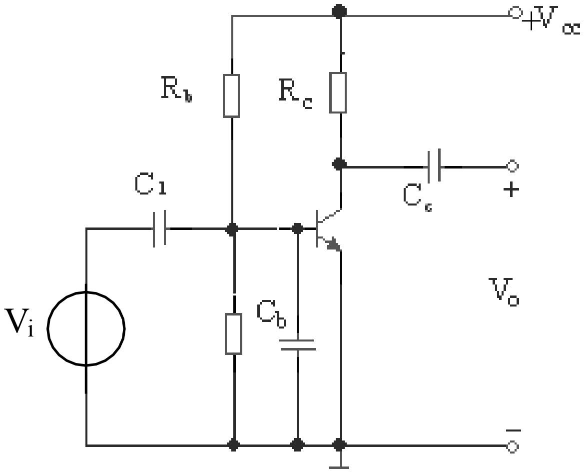
coupling capacitor
(only passes ac signals)

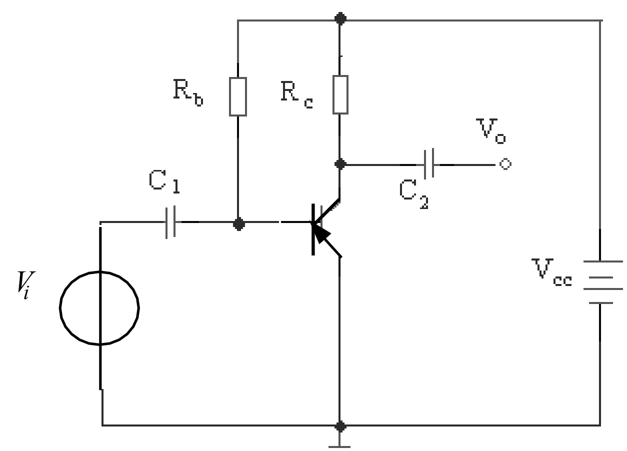
$$v_i \xrightarrow{C_2} \Delta v_{BE} \rightarrow \Delta i_B \rightarrow \xrightarrow{\Delta i_C = \beta \Delta i_B} \Delta i_c \xrightarrow{R_C} \Delta v_{CE} \xrightarrow{C_1} v_o$$

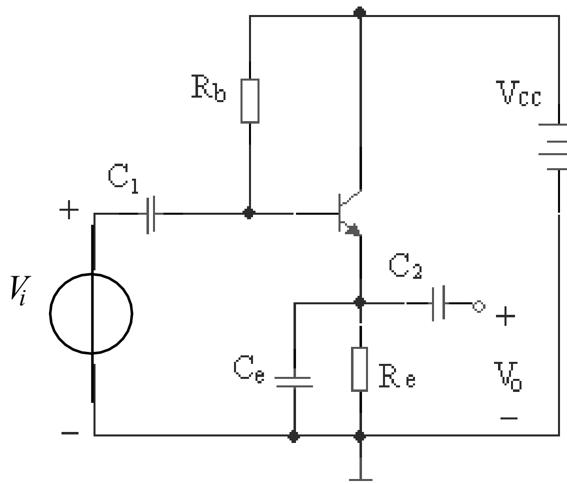
$v_i \rightarrow \Delta i_B$ $\quad$ $\Delta i_B \rightarrow \Delta i_C$ $\quad$ $\Delta i_C \rightarrow v_O$

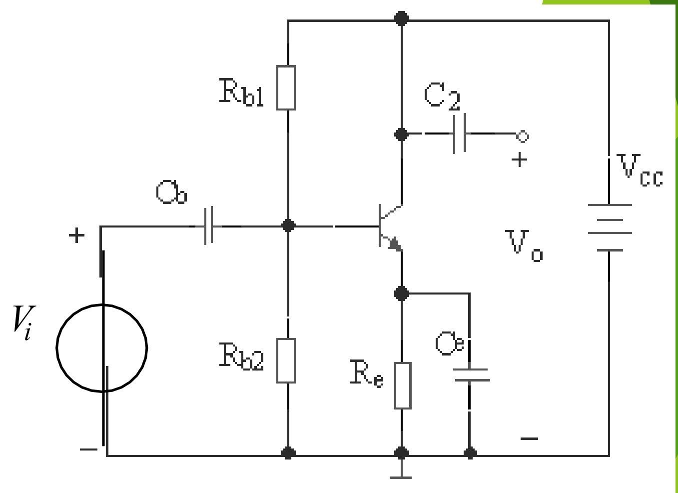
Single-Stage BJT Amplifiers

C-E Amplifiers



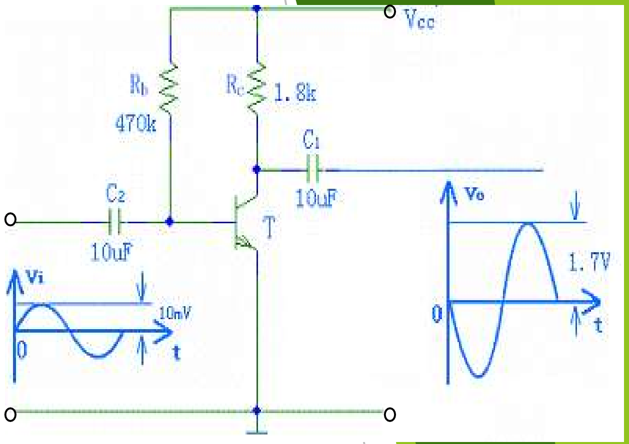




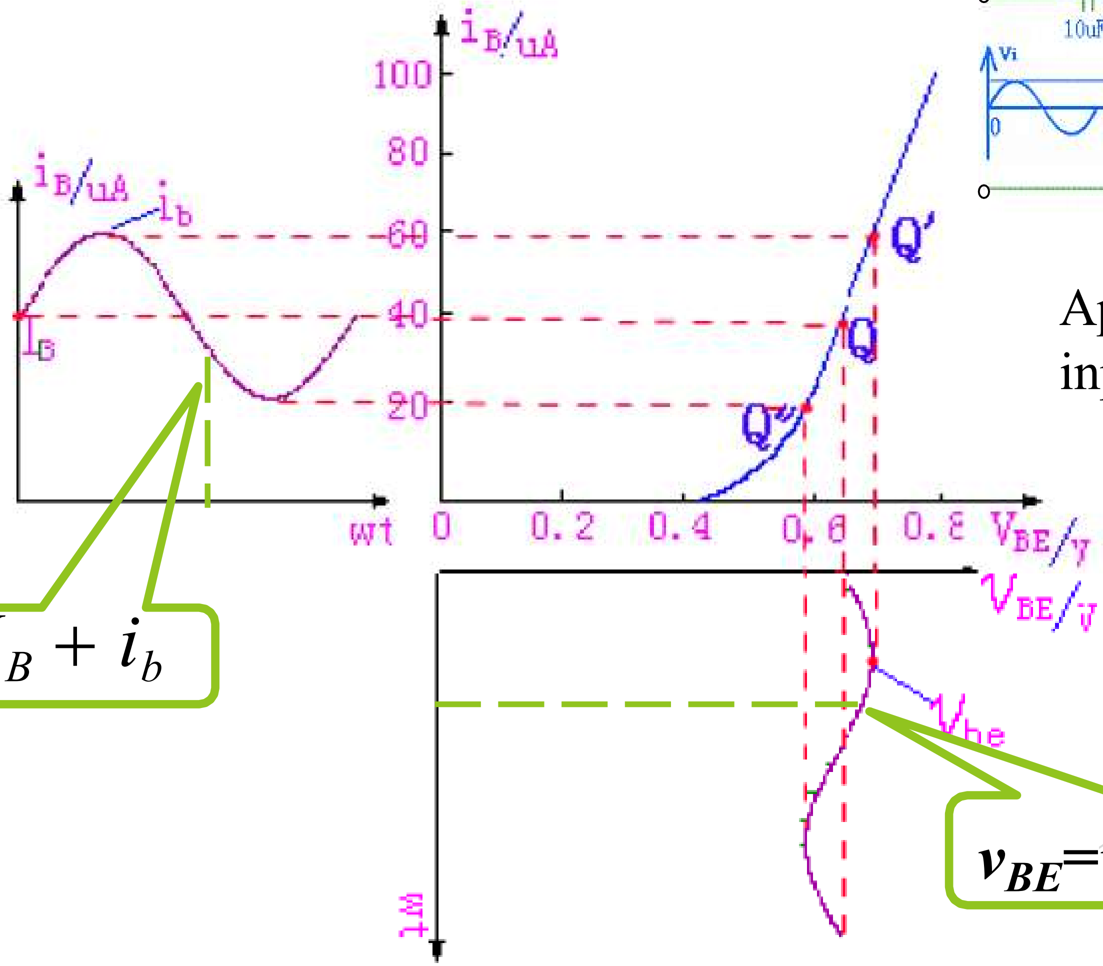


Single-Stage BJT Amplifiers

C-E Amplifiers



Apply a small signal input voltage and see i_b



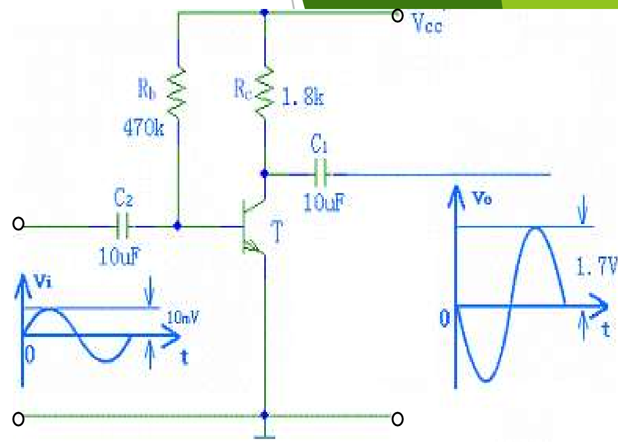
$$i_B = I_B + i_b$$

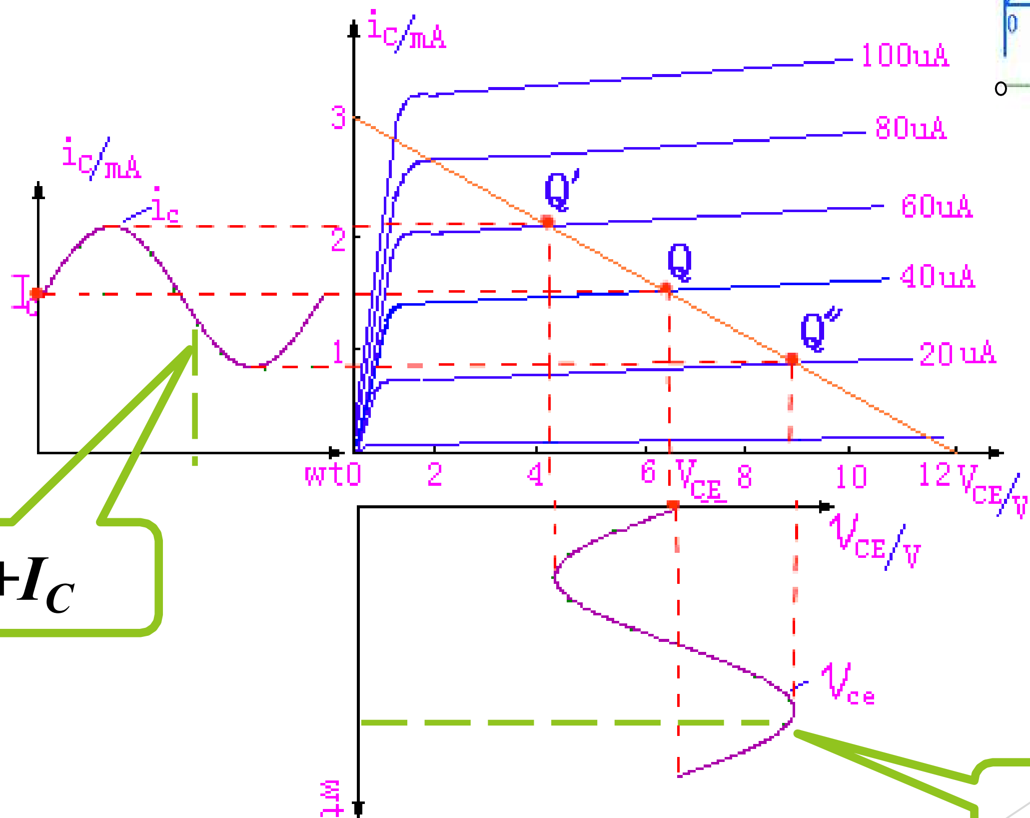
$$v_{BE} = v_i + V_{BE}$$

Single-Stage BJT Amplifiers

C-E Amplifiers

See how i_b translates into v_{ce}.





$i_C = i_c + I_C$

- $v_i = 0 \rightarrow I_B$、I_C、V_{CE}

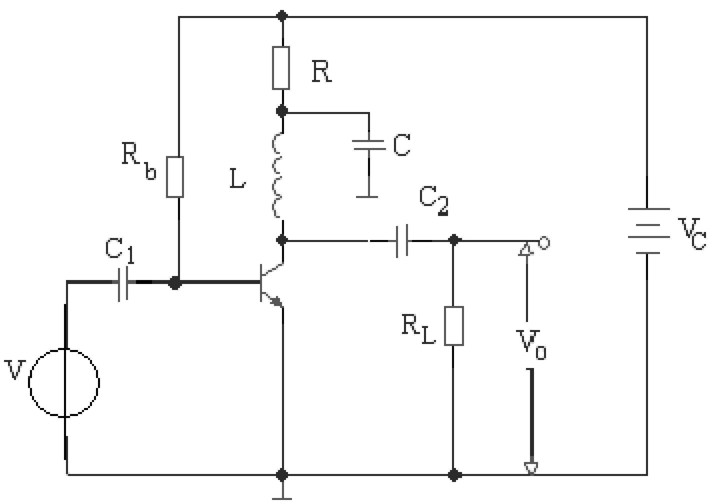
$$v_i \neq 0 \qquad \left.\begin{aligned} i_B &= I_B + i_b \\ i_C &= I_C + i_c \\ v_{CE} &= V_{CE} + v_{ce} \end{aligned}\right\}$$

- $V_{oM} >> V_{iM}$ $\qquad f_{(o)} = f_{(i)}$
- v_o *out of phase with* v_i

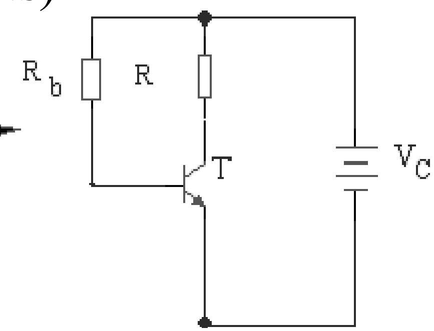
$v_{CE} = v_{ce} + V_{CE}$

Single-Stage BJT Amplifiers

C-E Amplifiers



Considering V_C (all the capaertors are replaced by open circuits)



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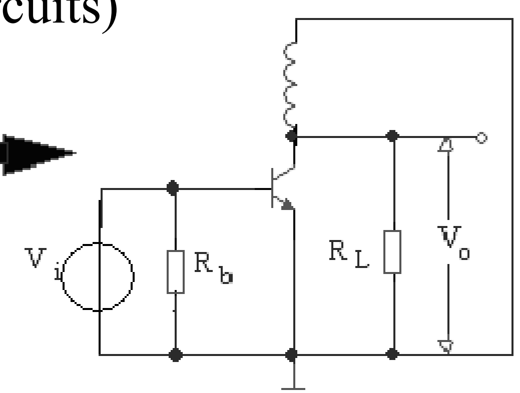
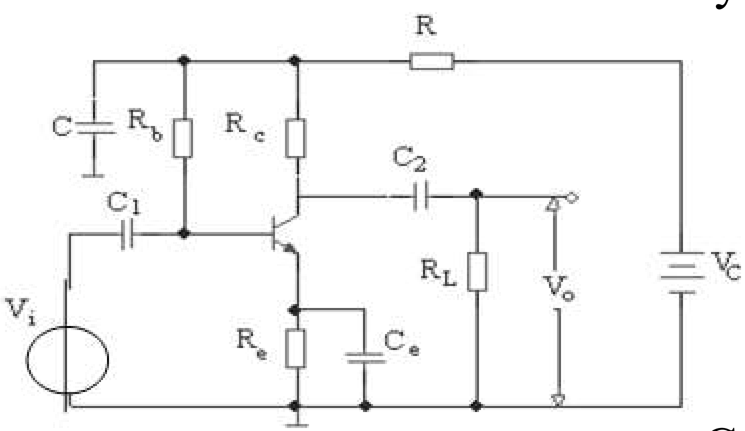


Single-Stage BJT Amplifiers

C-E Amplifiers



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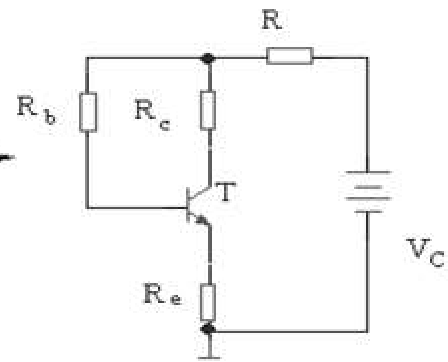

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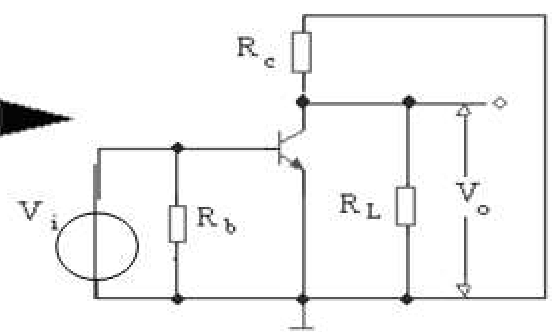
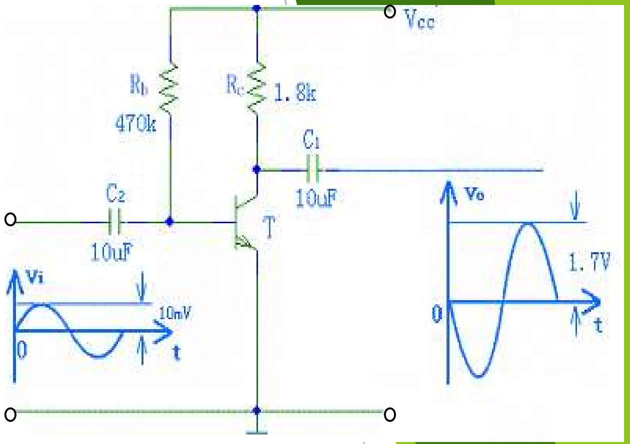
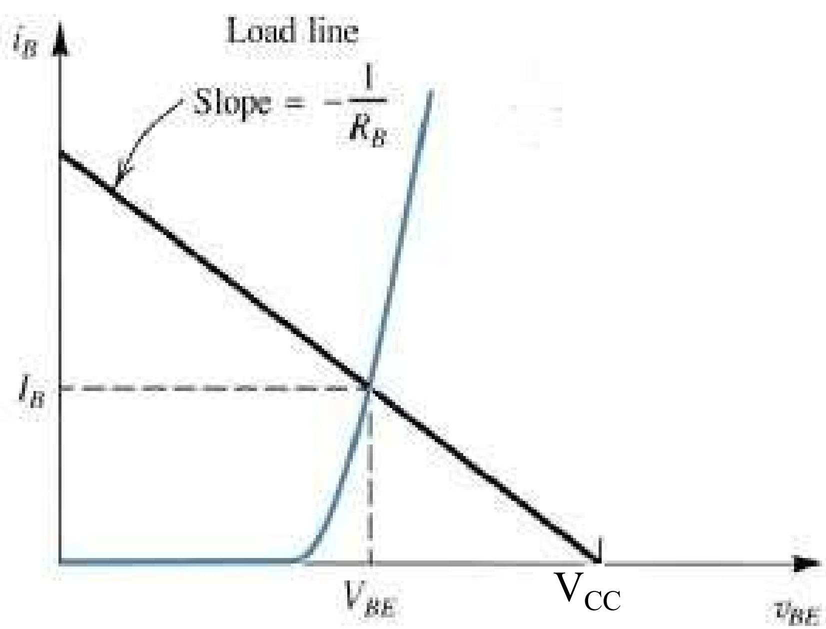


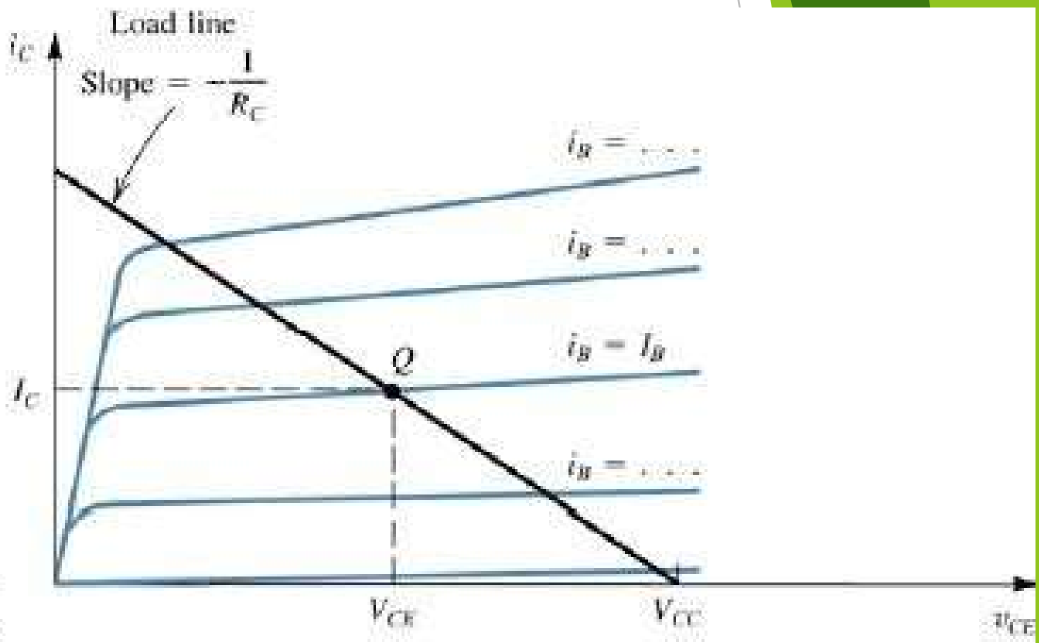
Single-Stage BJT Amplifiers

Graphical Analysis

- Can be useful to understand the operation of BJT circuits.
- First, establish DC conditions by finding I_B (or V_{BE})
- Second, figure out the DC operating point for I_C





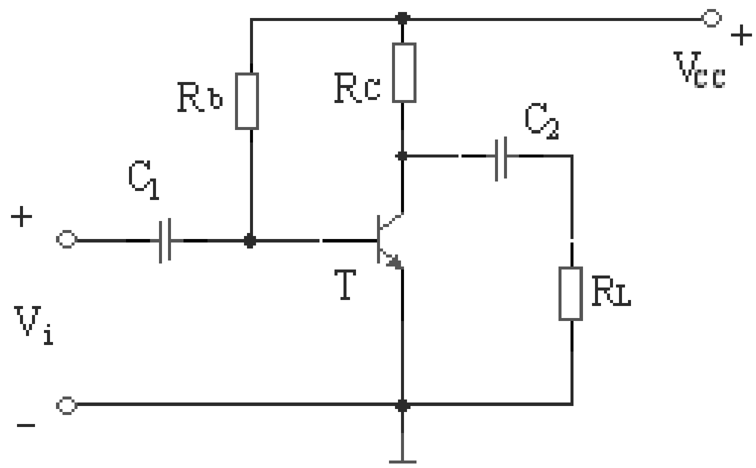


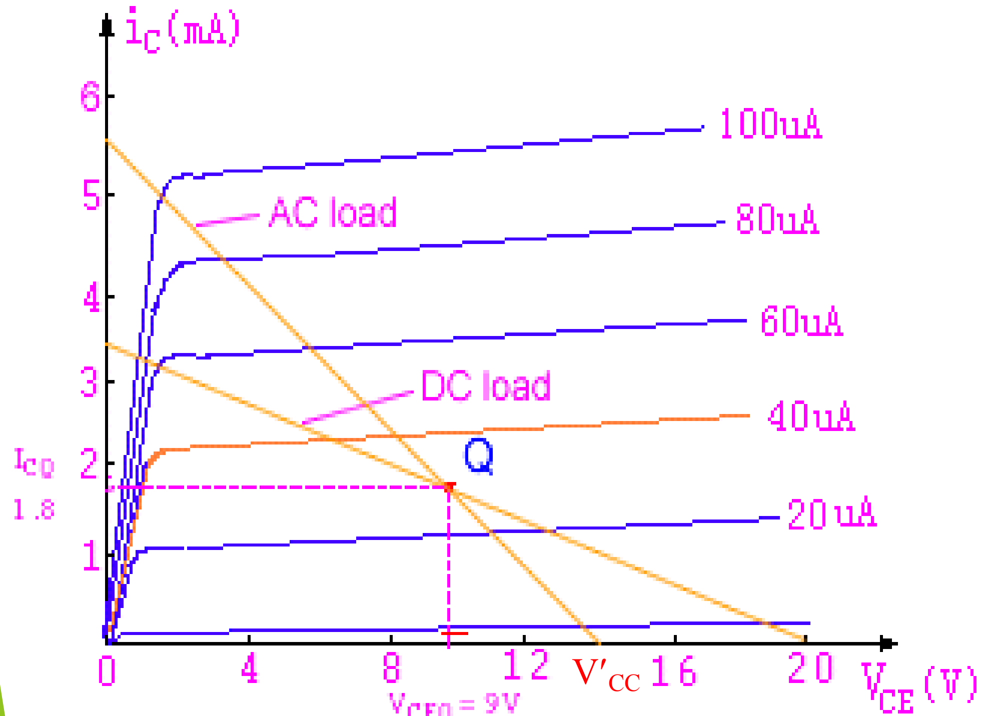
Can get a feel for whether the BJT will stay in active region of operation

– What happens if R_C is larger or smaller?

Single-Stage BJT Amplifiers

Graphical Analysis





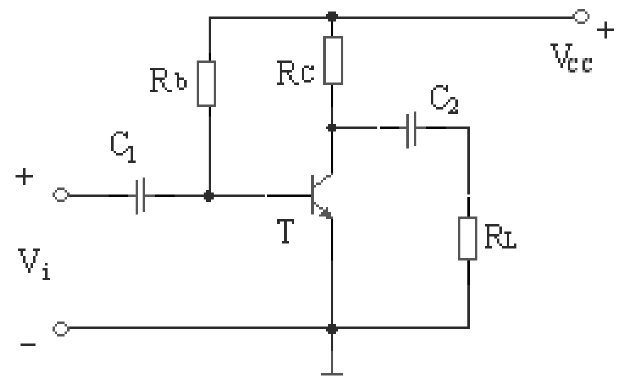
$$v_{ce} = -i_c (R_C // R_L) = -i_c R_L'$$

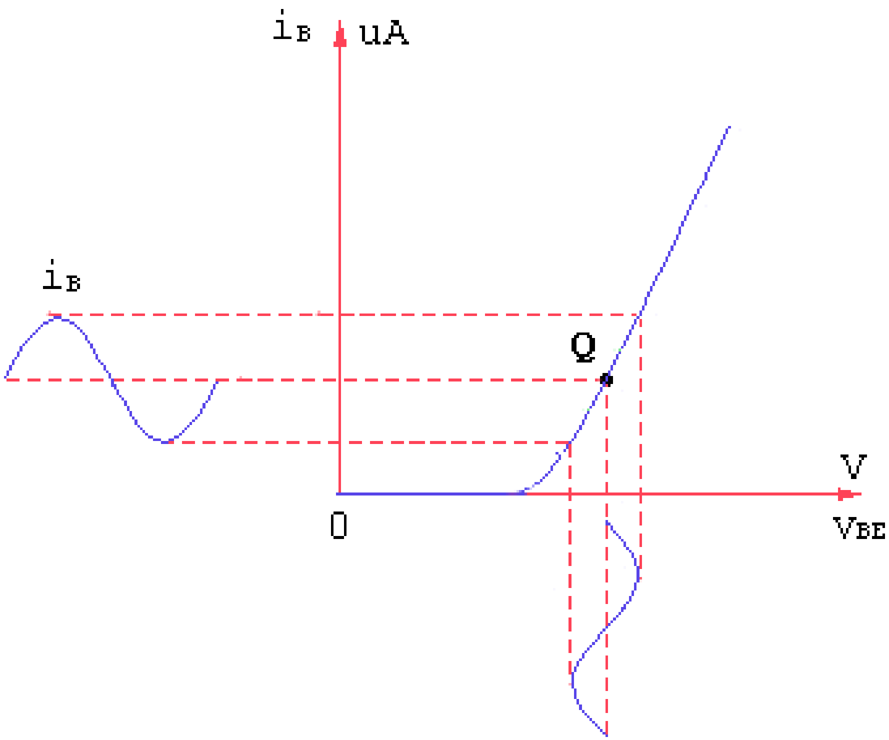
$$V_{CC}' = V_{CEQ} + I_{CQ} R_L'$$

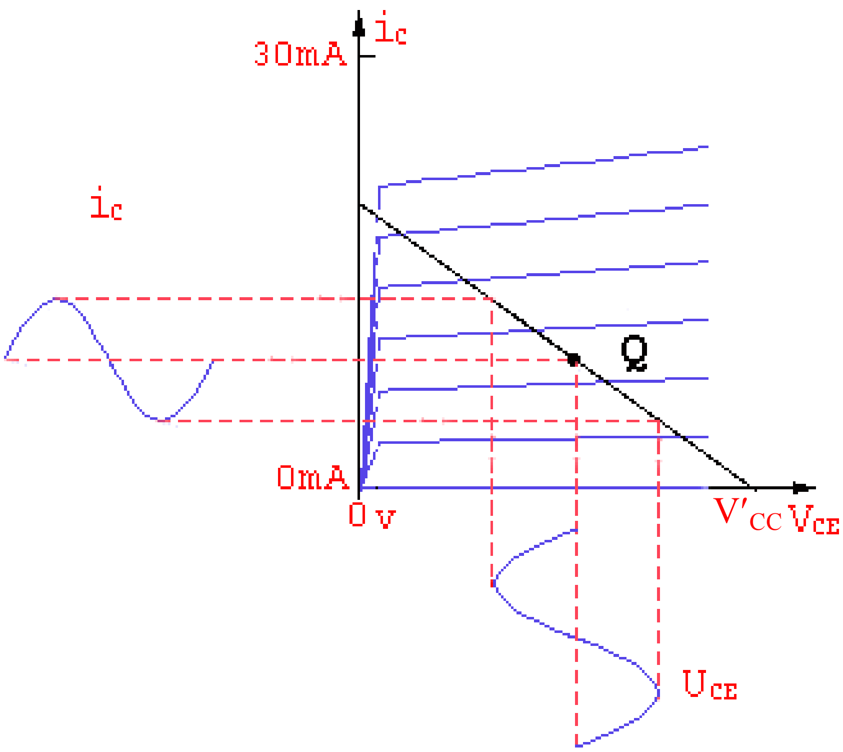
Single-Stage BJT Amplifiers

Graphical Analysis

Q-point is centered on the ac load line:



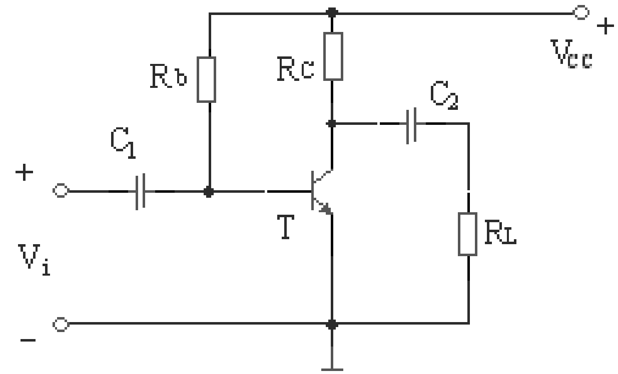


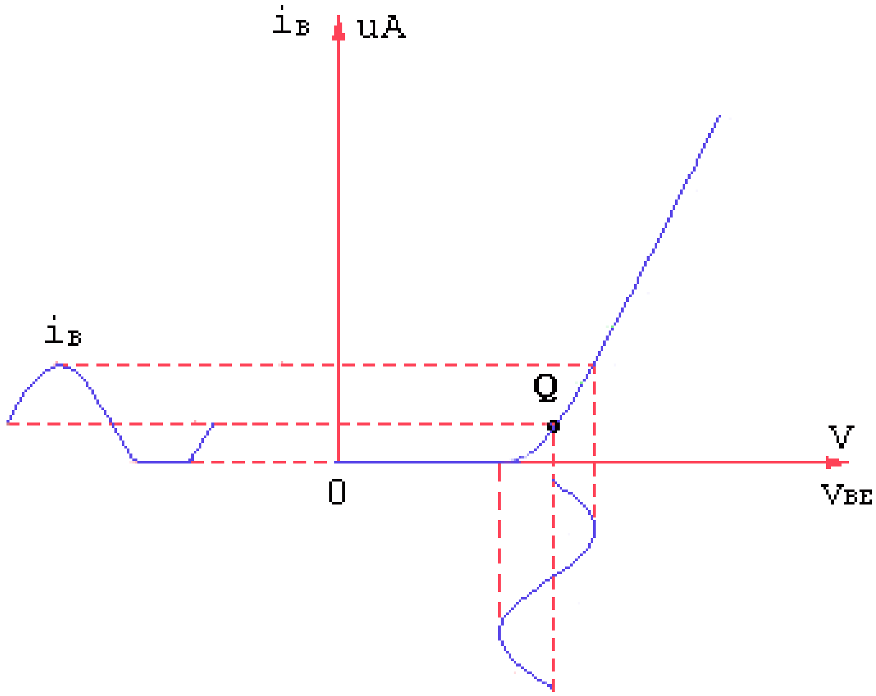


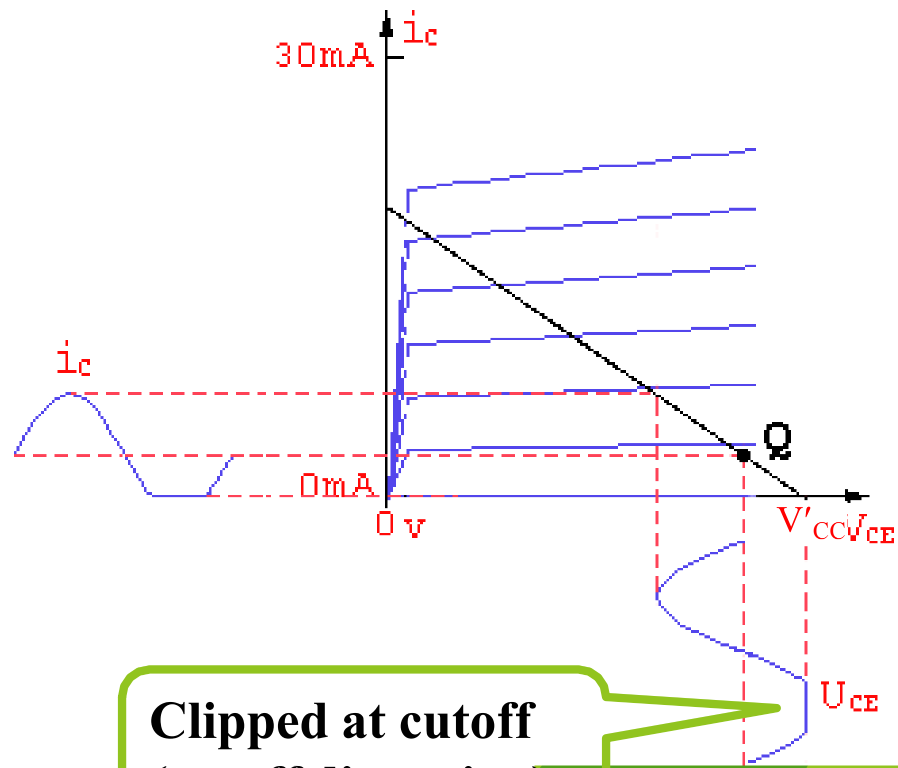
Single-Stage BJT Amplifiers

Graphical Analysis

Q-point closer to cutoff:





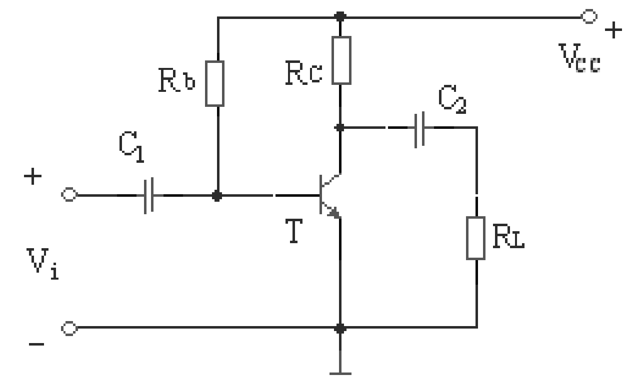


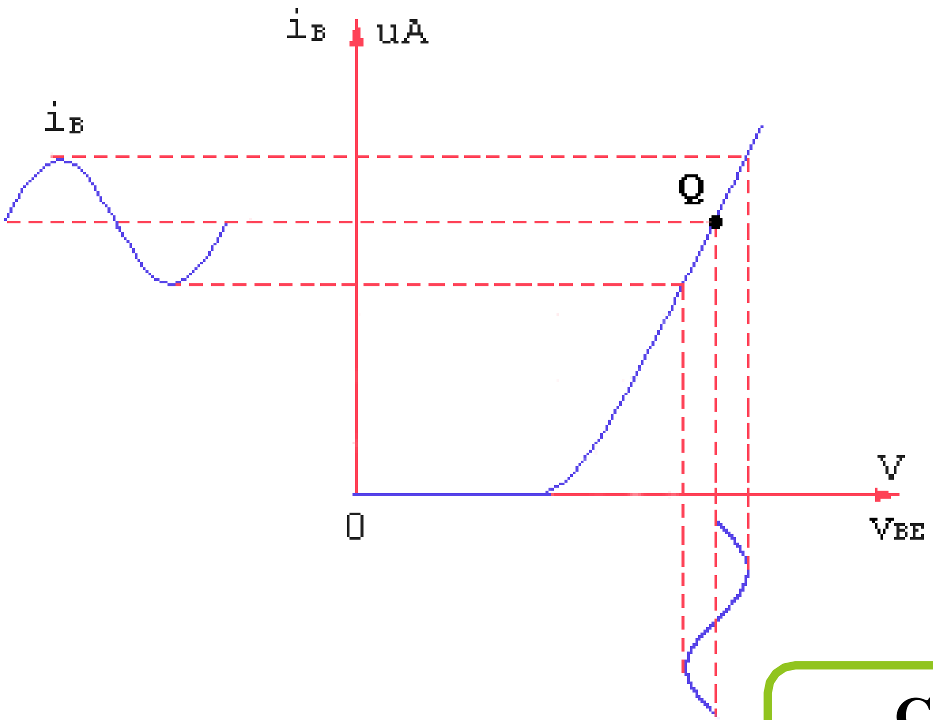
Clipped at cutoff (cutoff distortion)

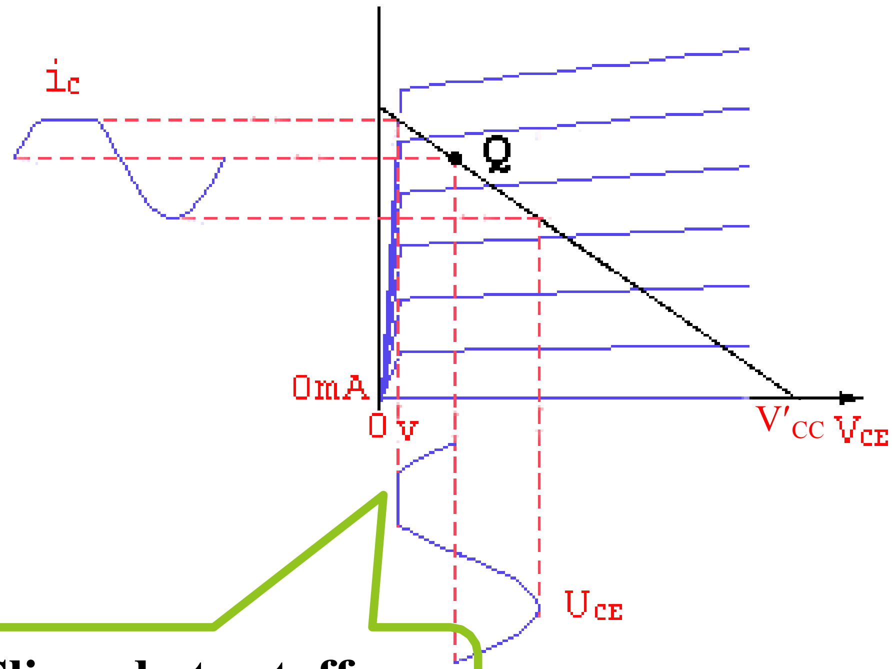
Single-Stage BJT Amplifiers

Graphical Analysis

Q-point closer to saturation:



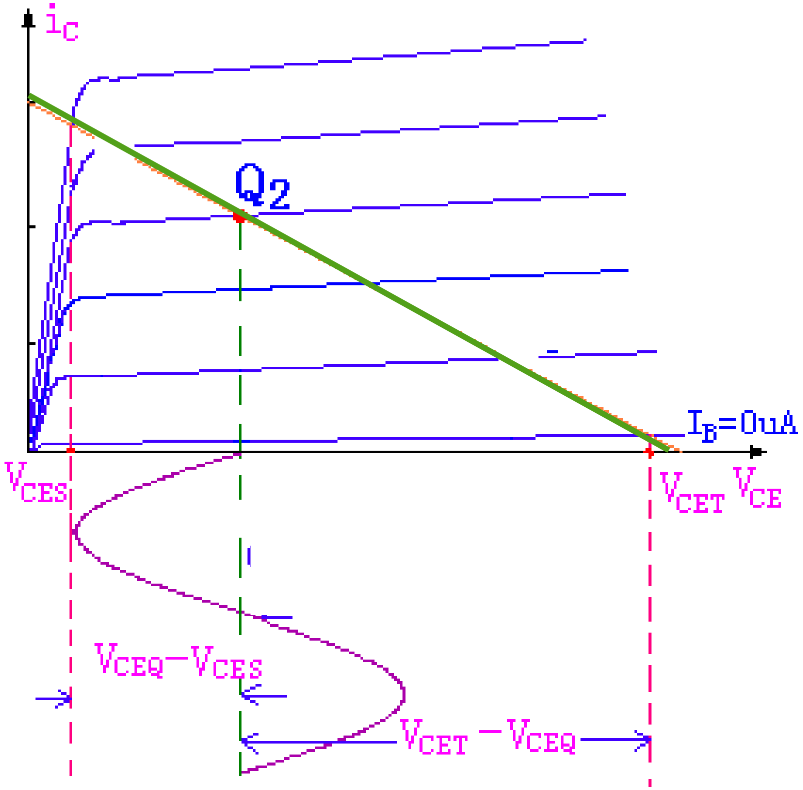


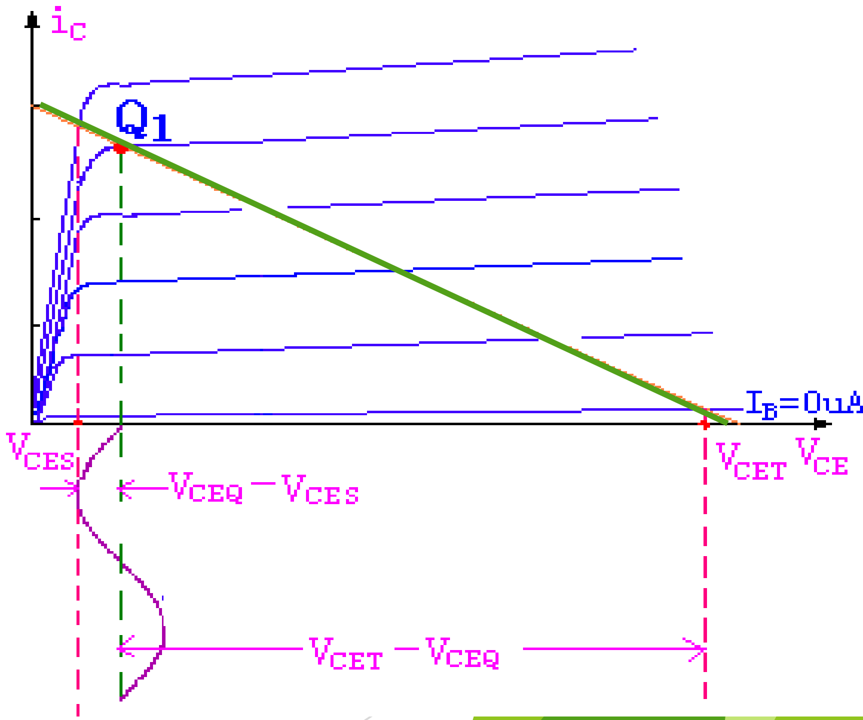


Clipped at cutoff (saturation distortion)

Single-Stage BJT Amplifiers

Graphical Analysis





Transistor hybrid model

Two Port Network

Types of Parameters:

i) Z - Parameters (or) Impedance Parameters

ii) Y - Parameters (or) Admittance Parameters

iii) H - Parameters (or) Hybrid Parameters

Z - Parameters (or) Impedance Parameters

Here i_1 and i_2 are taken as independent variables. The voltages V_1 and V_2 are given by the equations.

$$V_1 = Z_{11}i_1 + Z_{12}i_2$$

$$V_2 = Z_{21}i_1 + Z_{22}i_2$$

These four impedance parameters Z_{11}, Z_{22}, Z_{12} and Z_{21} are defined as follows.

$Z_{11} = V_1/i_1$ with $i_2=0$ = Input impedance with Output port open circuited.

$Z_{22} = V_2/i_2$ with $i_1=0$ = Output impedance with Input port open circuited.

$Z_{12} = V_1/i_2$ with $i_1=0$ = Reverse Transfer impedance with port1 open circuited.

$Z_{21} = V_2/i_1$ with $i_2=0$ = Forward Transfer impedance with port2 open circuited.

Y - Parameters (or) Admittance Parameters

Here V_1 and V_2 are taken as independent variables; the currents i_1 and i_2 are given by the equations.

$$i_1 = Y_{11} V_1 + Y_{12} V_2$$

$$i_2 = Y_{21} V_1 + Y_{22} V_2$$

Y_{11}, Y_{12}, Y_{21} and Y_{22} are called short circuited admittance parameters and that are defined as follows.

$Y_{11} = i_1/V_1$ with $V_2=0$ = Input Admittance with port 2 short circuited.

$Y_{22} = i_2/V_2$ with $V_1=0$ = Output Admittance with port 1 short circuited.

$Y_{12} = i_1/V_2$ with $V_1=0$ = Reverse Transfer Admittance with port 1 short circuited.

$Y_{21} = i_2/V_1$ with $V_2=0$ = Forward Transfer Admittance with port 2 short circuited.

H - Parameters (or) Hybrid Parameters

If the input current i_1 and the output voltage V_2 are taken as independent variables, the input voltage V_1 and output current i_2 can be written as

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11} = V_1/i_1$ with $V_2=0$ = Input impedance with output port short circuited.

$h_{22} = i_2/V_2$ with $i_1=0$ = Output Admittance with input port open circuited.

$h_{12} = V_1/V_2$ with $i_1=0$ = Reverse Voltage Transfer ratio with input port open circuited.

$h_{21} = i_2/i_1$ with $V_2=0$ = Forward current gain with output port short circuited.

Notation:

When h - parameters are applied to transistors, first subscript,

i - input;

o - output;

f - forward transfer;

r - reverse transfer

Second subscript to designate the type of configuration,

e - common emitter;

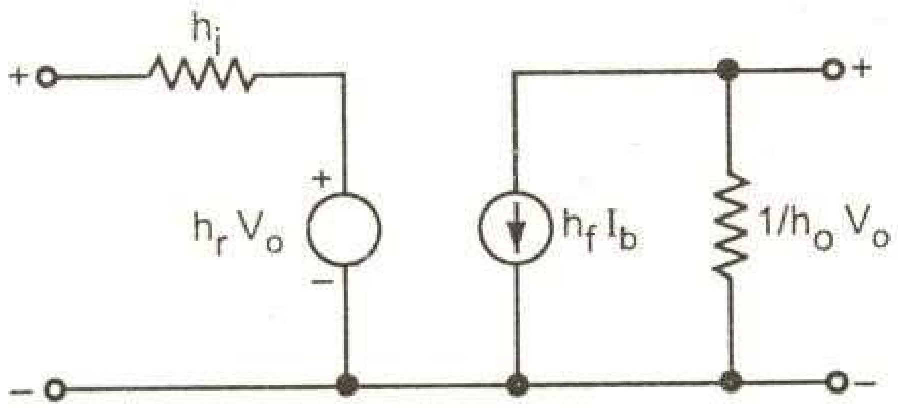
b - common base;

c - common collector.

The Hybrid model for two - port network

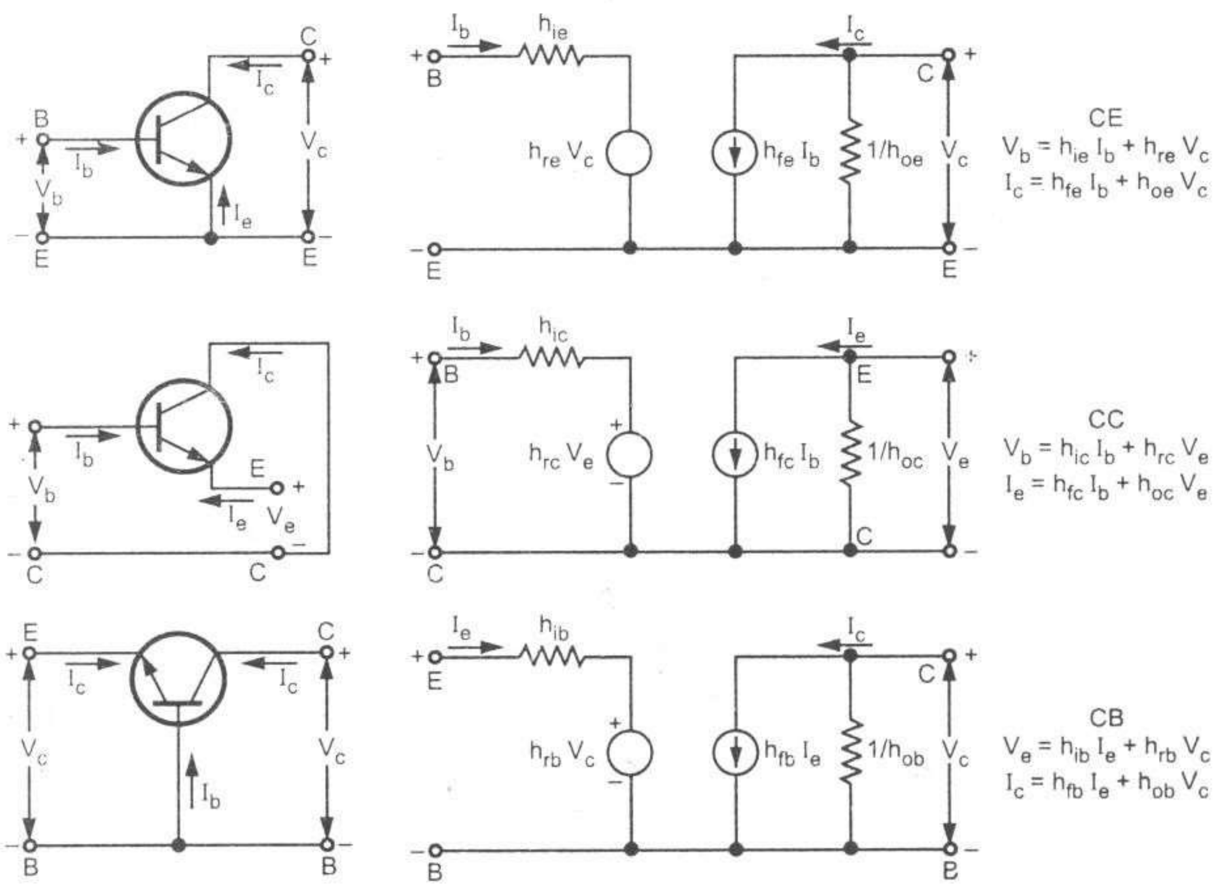
$$V_1 = h_i\, i_1 + h_r\, V_2$$

$$i_2 = h_f\, i_1 + h_o\, V_2$$



Hybrid model for two-port network

Hybrid models for the transistor in three different configu



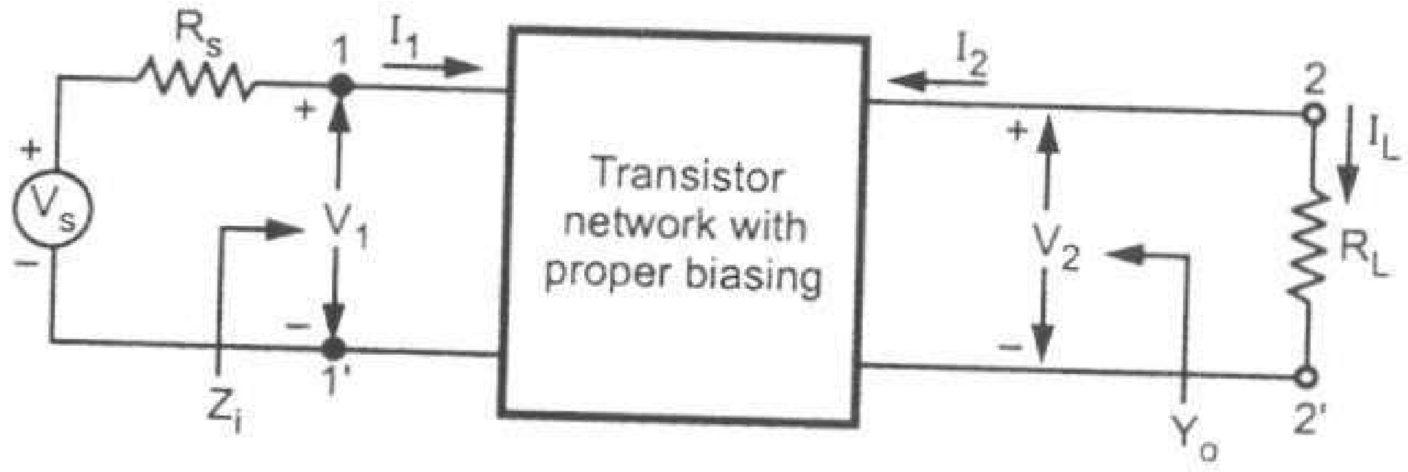
Typical Values

Parameters	CE	CC	CB
hi	1,100 Ω	1,100 Ω	21.6 Ω
hr	2.5×10^{-4}	1	2.9×10^{-4}
hf	50	-51	-0.98
ho	25 μA/v	25 μA/v	0.49 μA/v
1/h0	40K	40K	2.04M Ω

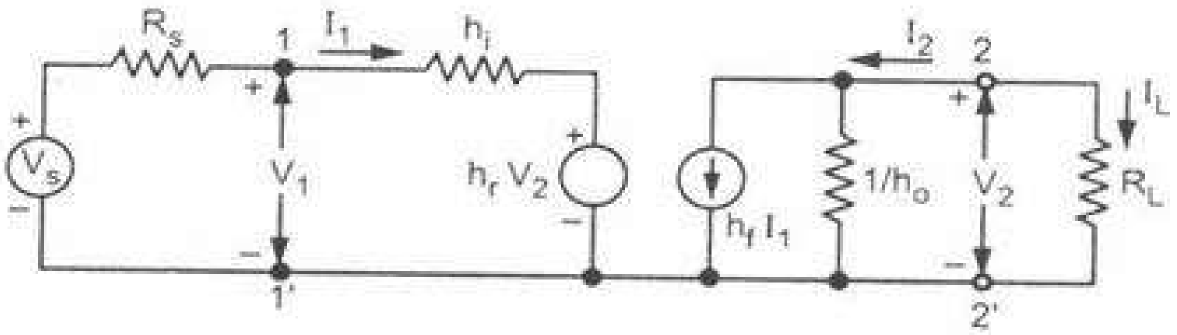
Conversion Table:

CC	CB
$h_{ic} = h_{ie}$	$hib = \frac{hie}{1 + hfe}$
$h_{rc} = 1$	$hrb = \frac{hiehoe}{1 + hfe} - hre$
$h_{fc} = -(1+h_{fe})$	$hfb = \frac{-hfe}{1 + hfe}$
$h_{oc} = h_{oe}$	$hob = \frac{hoe}{1 + hfe}$

Analysis of a Transistor Amplifier Circuit Using h- Parameters



Basic Amplifier circuit



Transistor amplifier in its h-parameter model

Current Gain:

$$A_I = \frac{-h_f}{1 + hoZ_L}$$

Voltage Gain:

$$\therefore A_V = \frac{A_I Z_L}{Z_i}$$

Input Impedance:

$$Z_i = hi - \frac{h_f h_r}{Y_L + ho}$$

Output Admittance:

$$\therefore Y_0 = h_0 - \frac{h_f h_r}{h_i}$$

Power Gain:

$$A_P = A_I^2 \left(\frac{R_L}{R_i} \right)$$

Current Gain With Source Resistance:

$$A_{IS} = A_{VS} \cdot \frac{R_S}{Z_L}$$

Voltage Gain With Source Resistance:

$$\therefore A_{VS} = \frac{A_I Z_L}{Z_i + R_S}$$

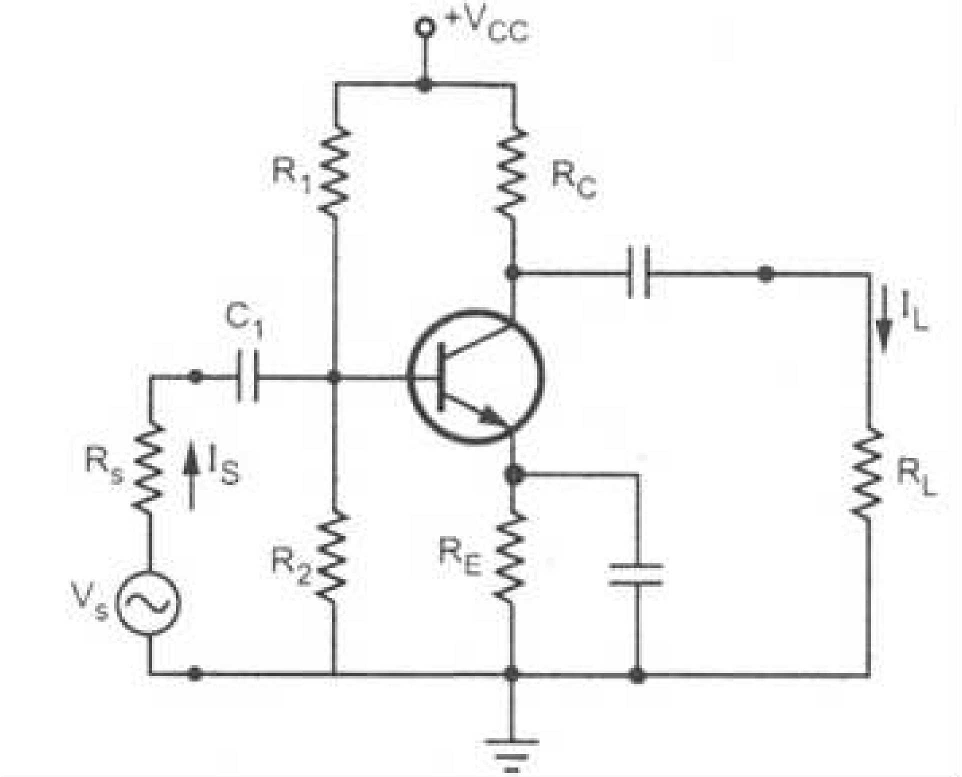
Input Impedance With Source Resistance:

$$Z_{is} = R_s + Z_i$$

Output Admittance With Source Resistance:

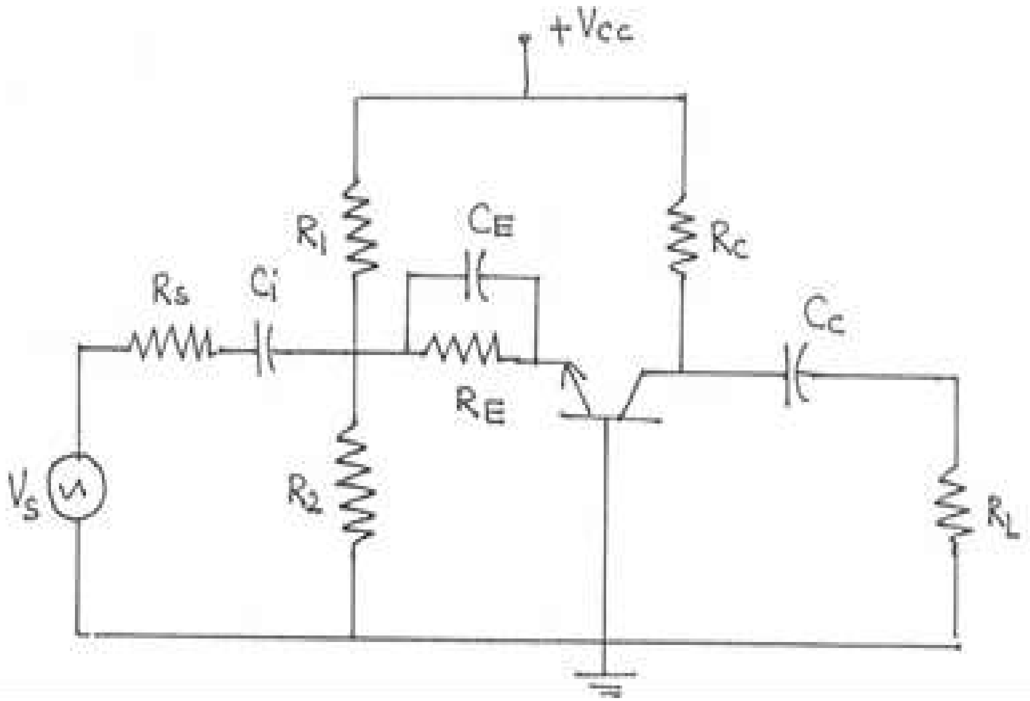
$$\therefore Y_0 = h_0 - \frac{h_f h_r}{R_S + h_i}$$

Analysis of CE amplifier using h-parameter model:



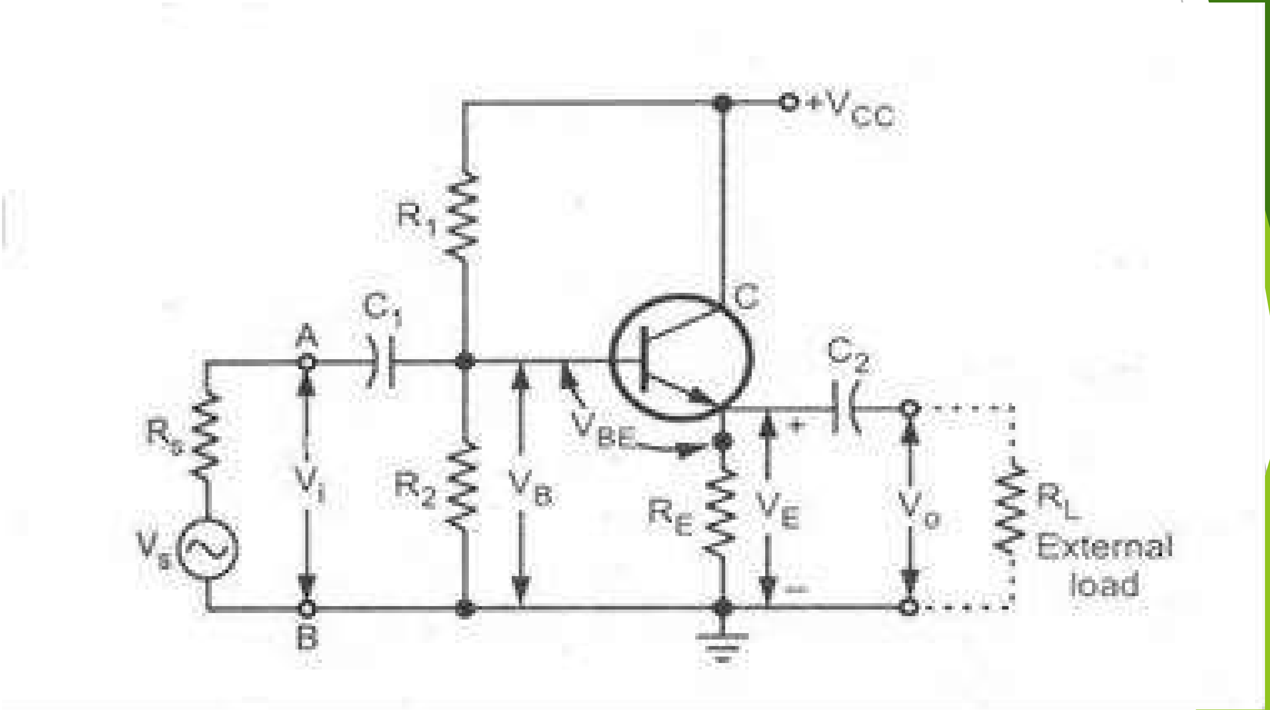
Common Emitter Amplifier

Analysis of CB amplifier using h-parameter model



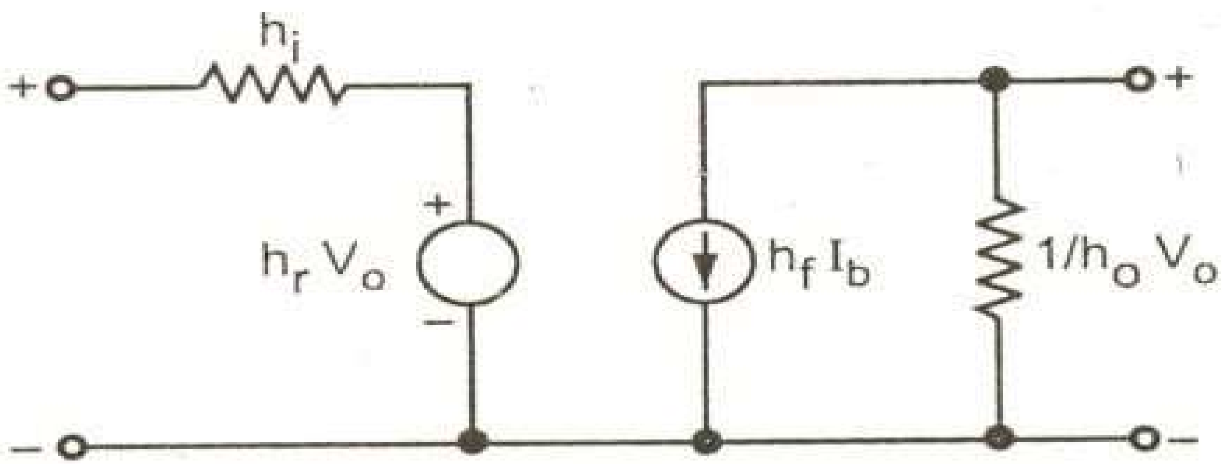
Common Base Amplifier

Analysis of CC amplifier using h-parameter model

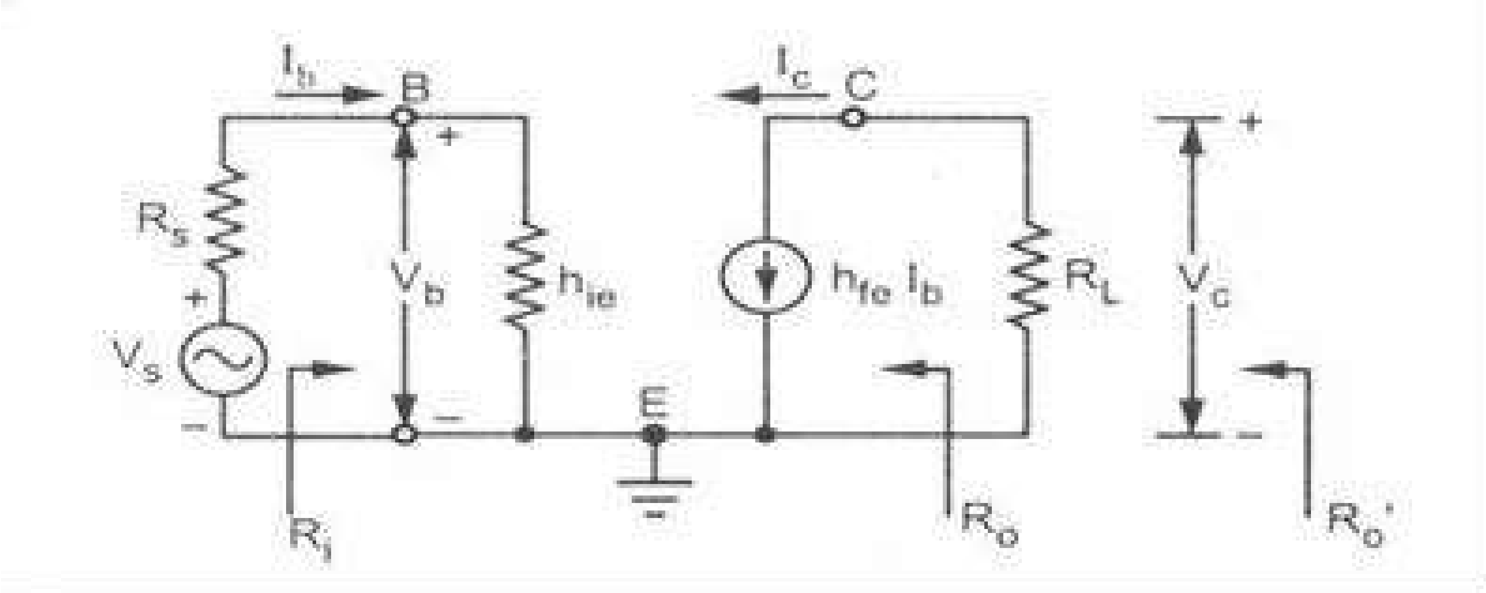


Common Collector Amplifiers

Simplified CE hybrid model:

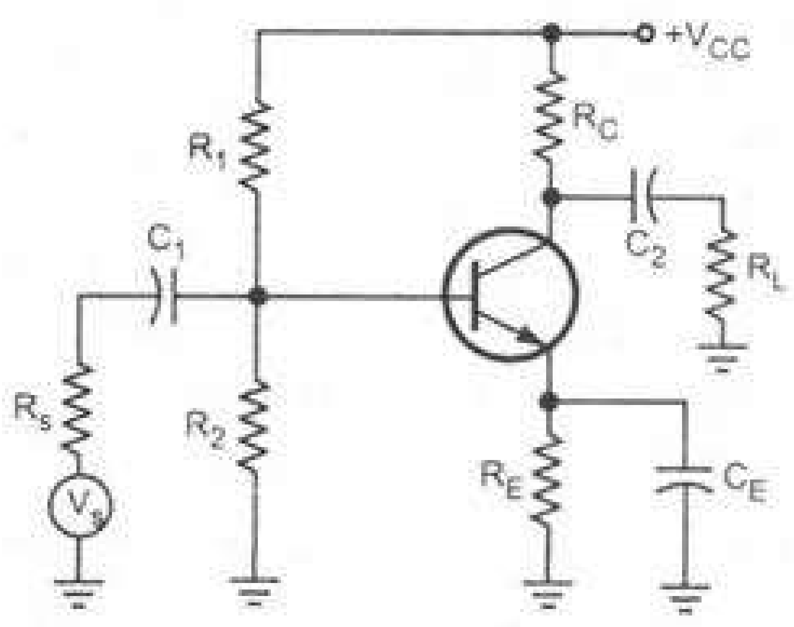


Exact CE hybrid model



Approximate CE hybrid model

Analysis of CE amplifier using approximate model:



Current Gain (A_I): $$\therefore A_I = -h_{fe}$$

Input Impedance (Z_i): $$\therefore Z_i = h_{ie}$$

Voltage Gain (A_V): $$\therefore A_V = \frac{-h_{fe} Z_L}{h_{ie}}$$

Output Impedance (Z_0): $Y_0 = 0$ $Z_0 = \infty$

Characteristics of CB Amplifier:

i) Current gain of less than unity.
ii) High voltage gain.
iii) Power gain approximately equal to voltage gain.
iv) No phase shift for current (or) voltage.
v) Small input impedance.
iv) Large output impedance.

Applications:

1) Matching a very low impedance source.
2) As a non-inverting amplifier with voltage gain exceeding unity.
3) For driving a high impedance load.
4) As a constant current source.

Characteristics of CC Amplifier:

1) High current gain.
2) Voltage gain of approximately unity.
3) Power gain approximately equal to current gain.
4) No current (or) voltage phase shift.
5) Large input impedance.
6) Small output impedance.

Applications:

The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load. The CC amplifier is called the emitter follower

Characteristics of CE amplifier:

1. Large current gain.
2. Large voltage gain.
3. Large power gain.
4. Voltage phase shift of 180^0.
5. Moderate input impedance.
6. Moderate output impedance.

Applications:

Of the three configurations CE amplifier alone is capable of providing both voltage gain and current gain. The input resistance $\mathbf{R_i}$ and the output resistance **Ro** are moderately high.

Hence the CE amplifier is widely used for amplification purpose.

Single-Stage BJT Amplifiers

Small-Signal Models Analysis

Steps for using small-signal models

1. Determine the DC operating point of the BJT

    — in particular, the collector current

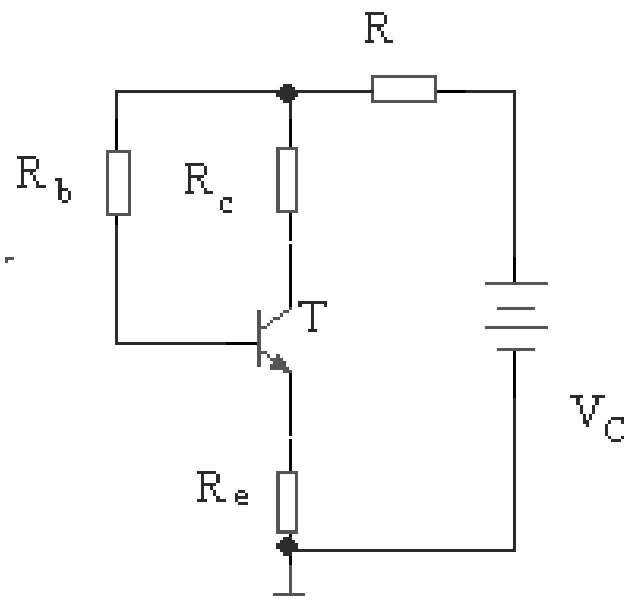
2. Calculate small-signal model parameters: r_{be}
3. Eliminate DC sources

    – replace voltage sources with shorts and current sources with open circuits

4. Replace BJT with equivalent small-signal models
5. Analysis

Single-Stage BJT Amplifiers

Small-Signal Models Analysis



$$V_C = (I_B + I_C)R + I_B R_b + V_{BE} + I_E R_e$$

$$\rightarrow I_B = \frac{V_C - V_{BE}}{R_b + (1+\beta)(R + R_e)}$$

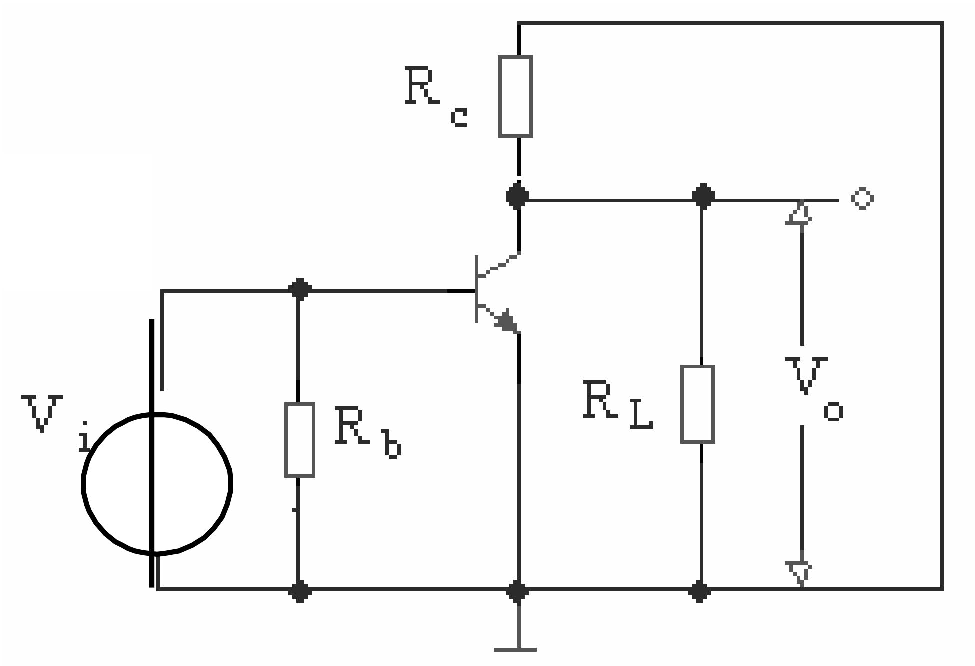
$$I_C \approx \beta I_B,$$
$$I_E = I_C + I_B = (1+\beta) I_B$$

$$V_{CE} = V_C - I_C R_C - I_E (R + R_e)$$

Single-Stage BJT Amplifiers

Small-Signal Models Analysis

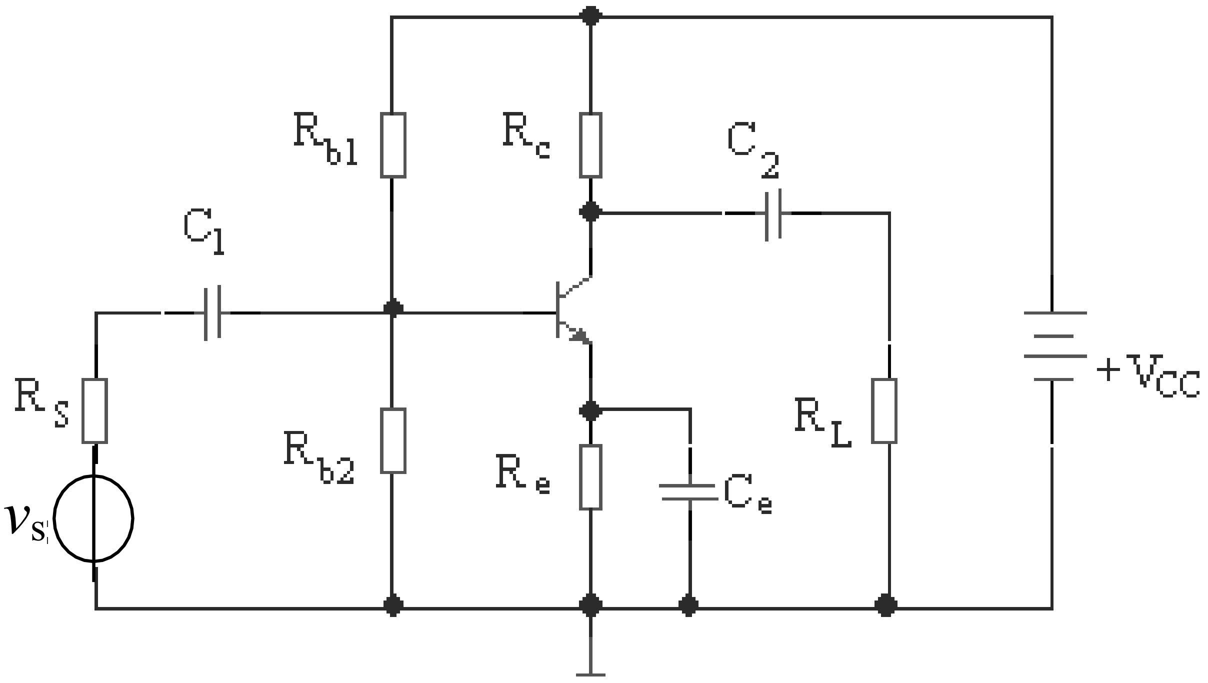
Example 1



Single-Stage BJT Amplifiers

Small-Signal Models Analysis

Example 2



$$V_B = \frac{R_{b2}}{R_{b1} + R_{b2}} V_{CC}$$

$$I_C \approx I_E = \frac{V_B - V_{BE}}{R_e} \approx V_B / R_e$$

$$I_B = \frac{I_C}{\beta}$$

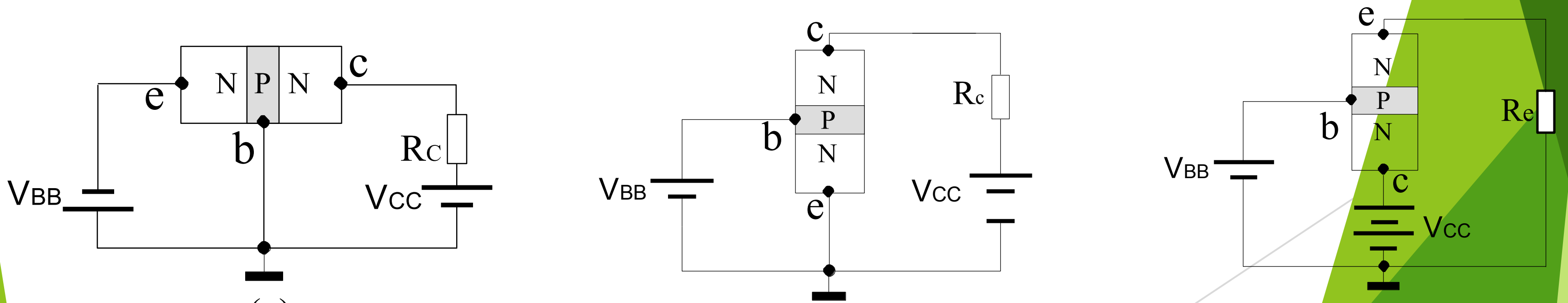
$$V_{CE} = V_{CC} - I_C (R_C + R_e)$$

Single-Stage BJT Amplifiers

Small-Signal Models Analysis

There are three basic configurations for single-stage BJT amplifiers:

- – Common-Emitter
- – Common-Base
- – Common-Collector



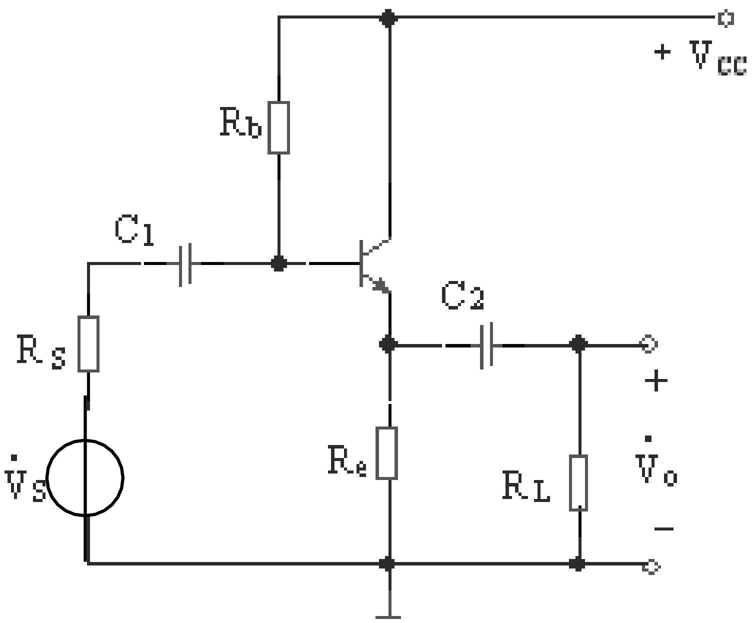
(a) $V_E < V_B < V_C$

(b) $V_E < V_B < V_C$

(c) $V_E < V_B < V_C$

Single-Stage BJT Amplifiers

Common-Collector Amplifier



$$V_{CC} = I_B R_b + V_{BE} + I_E R_e = I_B R_b + V_{BE} + (1+\beta) I_B R_e$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_b + (1+\beta) R_e} \approx \frac{V_{CC}}{R_b + (1+\beta) R_e}$$

$$I_C = \beta I_B$$

$$V_{CC} = V_{CE} + I_E R_e \approx V_{CE} + I_C R_e$$

$$V_{CE} \approx V_{CC} - I_C R_e$$

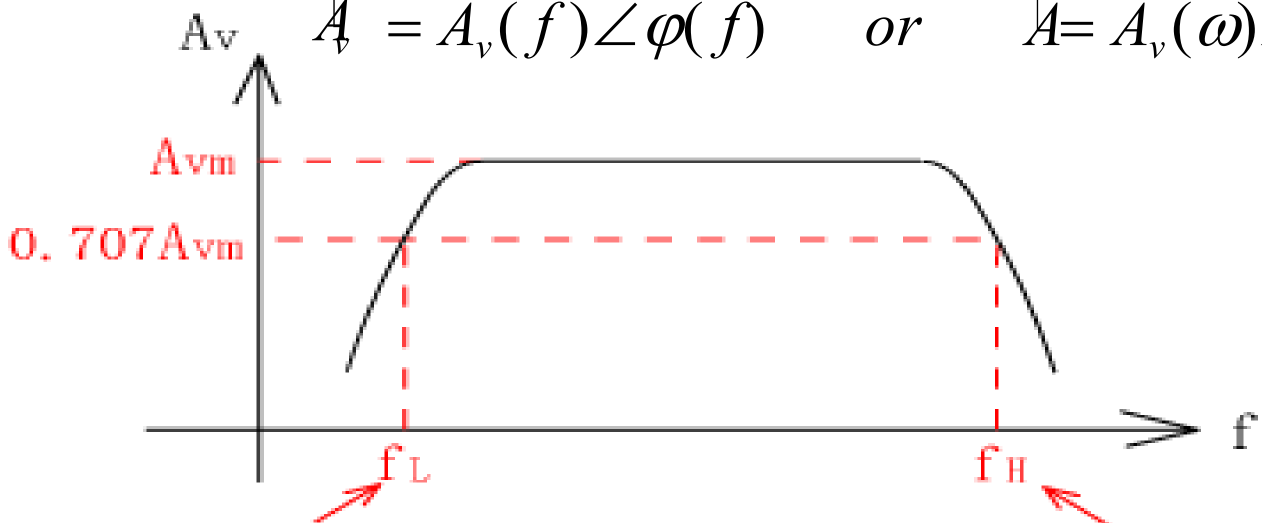
Note : $\dot{V}_o$ is slightly less than $\dot{V}_i$ due to the voltage drop introduced by V_{BE}

$$A_V \cong 1$$

Frequency Response

Basic Concepts

$$\dot{A}_v = A_v(f)\angle\varphi(f) \quad or \quad \dot{A}_v = A_v(\omega)\angle\varphi(\omega)$$



Lower cut off frequency　　　　Upper cut off frequency

The drops of voltage gain (output/input) is mainly due to:

1、Increasing reactance of C C C (at low f)

2、Porasitic capacetine elements of the net work (at high f)

3、Dissappearance of changing current(for trasformer coupled amp)

Classification of Amplifiers

- **Amplifiers can be classified as follows**
- **Based on the transistor configuration**

a)CE b) CB c)CC

- **Based on the active device a)FET b)BJT**
- **Based on the Q-point**

a)Class A b)class B c)class AB d)class C

- **Based on the No.of stages a) Single stage b) Multi stage**
- **Based on the output a)Voltage amplifier b)Current amplifier**
- **Based on the frequency response a) AF b) IF c)RF**
- **Based on the Bandwidth a)Narrow band b)Wide band**

DISTORTION IN AMPLIFIER

- If the output wave shape is not an exact replica of input then it is called as distortion
- There are three important distortions occurs in amplifiers
- 1.Frequency distortion : The gain of an amplifier is constant over a certain range of frequency band and reduces sharply in the low and high frequencies this causes distortion of the output signal called frequency distortion
- 2. Phase or Delay distortion: phase distortion is said to occur if the phase relationship between output and input is not same.
- The time of transmission or delay introduced by the amplifier is different for various frequencies.
- Harmonic or Amplitude distortion :this type of distortion is said to occur when the output contains new frequency components that are not present in the input signal.

CE,CB,CC Amplifiers comparison

Property	CB	CE	CC
Ri	Low(about 100Ω)	Moderate(about 750Ω)	High(about750kΩ)
Ro	High (about 450kΩ)	Moderate(about 45kΩ)	Low(about 25Ω)
Ai	1	High	High
Av	about 150	about 500	Less than 1
Phase shift b/w i/p & o/p (Degrees)	0 or 360	180	0 or 360

- Applications:

for high frequency circuits, for AF circuits ,for impedance matching

Unit-1(b)
FEEDBACK AMPLIFIERS

Agenda

- Introduction
- Need of Feedback
- Types of Feedback
- Classification of Feedback
- Working and Analysis
- Results
- Applications

Feedback

For negative feedback: *βA > 0 ;* For positive feedback: *βA < 0*

Advantages of Negative feedback

➢ Negative feedback can reduce the gain of the amplifier, but it has many advantages, such as gain stabilization, reduction of nonlinear distortion and noise, control of input and output impedances, and extension of bandwidth.

❑ Gain stabilization

$$A_f = \frac{A}{(1+\beta A)}$$

$$\frac{dA_f}{A} = \frac{1}{(1+\beta A)^2}$$

$$\frac{dA_f}{A_f} = \frac{1}{(1+\beta A)}\frac{dA}{A}$$

Therefore percentage change in A_f *(due to variations in some* circuit parameter) is reduced by (1+βA) times compared to without feedback.

Introduction

- A portion the output signal is fed back to the input of the amplifier is called “Feedback Amplifier”.

- Feedback is very useful in amplifiers in electronics.

Need of Feedback

- Practical realization of precision VLSI circuits is complicated

Why---

1. physical circuit components deviate from nominal values due to temperature, process variation

2. circuit performance changes with frequency, load variations

There are two types of feedbacks.

1. Positive feedback

Source signal +feedback Signal → circuit

2. Negative feedback

Source signal - feedback Signal input → circuit

Positive Feedback

- If the feedback signal X_f is in phase with input signal Xs, then the type of feedback is said to be positive (or) regenerative feedback.

For positive feedback, $Xi=Xs+X_f$

$$Xs=X_i-X_f$$

Gain of the amplifier with feedback,

$$A_f = \frac{A}{1-A\beta}$$

- The product of the open loop gain and the feedback factor is called the Loop gain = Aβ.

- Gain is Infinity.

- Positive feedback increases the instability of an amplifier, reduces the bandwidth and increases the distortion and noise.

Negative Feedback

- If the feedback signal X_f is out of phase with input signal Xs, then the type of feedback is said to be Negative (or) de-generative feedback.

Therefore, for Negative feedback, $X_i = Xs - X_f$

$$Xs = X_i + X_f$$

Gain of the amplifier with feedback,

$$A_f = \frac{A}{1 + A\beta}$$

- If $|A\beta| >> 1$ then $A_f \approx 1/\beta$ where β is a feedback ratio. The gain may be made to depend entirely in the feedback network.

- If the feedback network contains only stable passive elements, the gain of the amplifier using Negative feedback is also stable.

- Effects of the product *AB*
  - If *AB* is negative
    - If *AB* is negative and less than 1, $(1 + AB) < 1$
    - In this situation $G > A$ and we have **positive feedback**
  - If *AB* is positive
    - If *AB* is positive then $(1 + AB) > 1$
    - In this situation $G < A$ and we have **negative feedback**
    - If *AB* is positive *and AB* $>>1$

$$G = \frac{A}{1 + AB} \approx \frac{A}{AB} = \frac{1}{B}$$

- gain is inde … th *A*

Negative Feedback Properties

- Negative feedback takes a sample of the output signal and applies it to the input to get several desirable properties. In amplifiers, negative feedback can be applied to get the following properties
  - Desensitized gain : gain less sensitive to circuit component variations

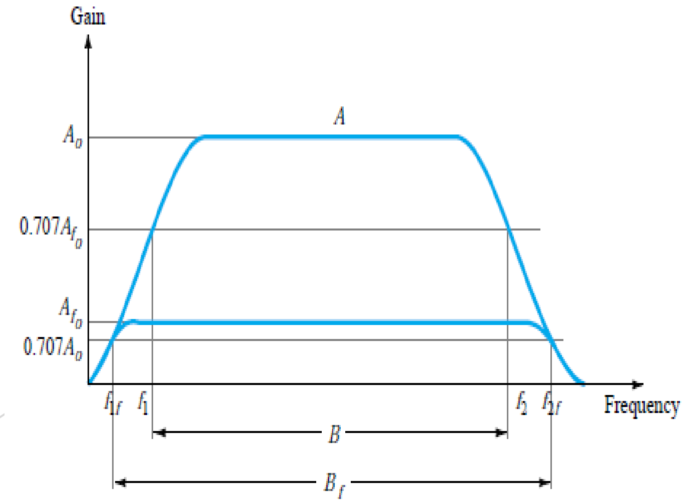
Gain of the amplifier with feedback, $A_f = \frac{X_0}{X_S} = \frac{AX_i}{X_i + X_f} = \frac{AX_i}{X_i + \beta X_0} = \frac{AX_i}{X_i + A\beta X_i} = \frac{A}{1 + A\beta}$

$$A_f = \frac{A}{1 + A\beta}$$

Differentiate on both sides then, we get

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{(1 + A\beta)}$$

Sensitivity $$\frac{\frac{dA_f}{A_f}}{\frac{dA}{A}} = \frac{1}{1 + A\beta}$$



The Effects of Negative Feedback

- **Effects on Gain**
  – negative feedback produces a gain given by

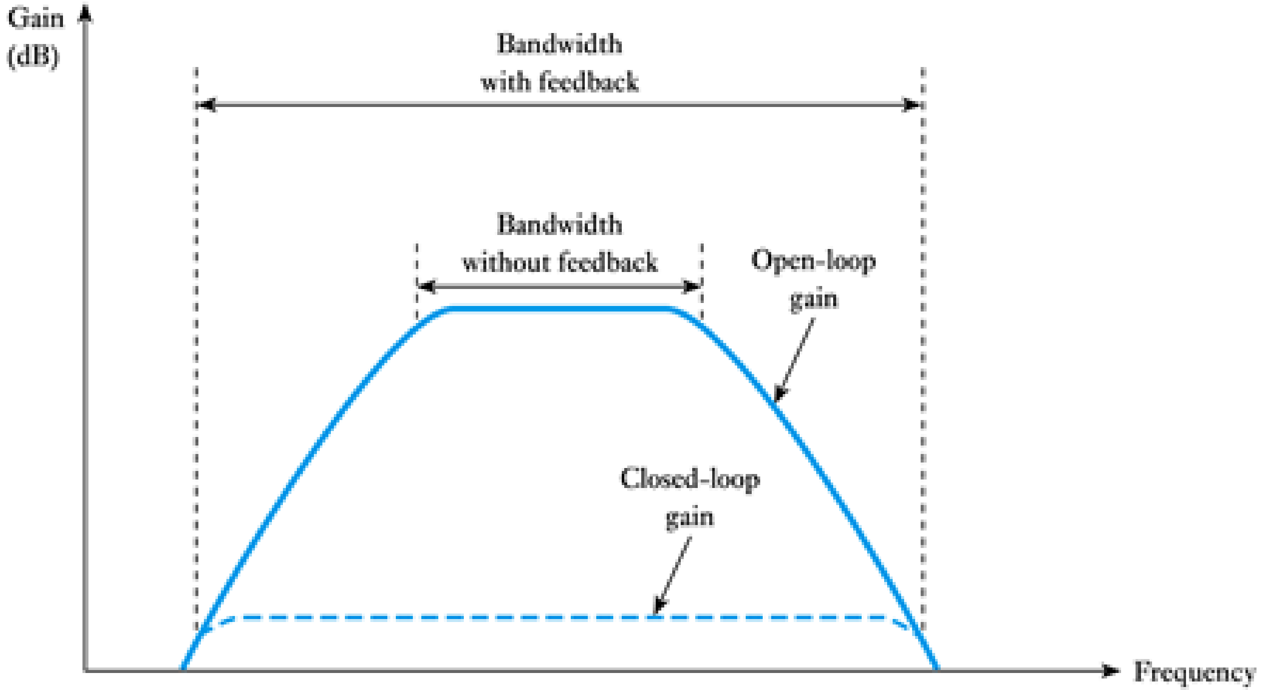
$$G = \frac{A}{1 + AB}$$

  – there, feedback *reduces* the gain by a factor of 1 + *AB*
  – this is the price we pay for the beneficial effects of negative feedback

- **Effects on frequency response**
  - from earlier lectures we know that all amplifiers have a limited frequency response and bandwidth
  - with feedback we make the overall gain largely independent of the gain of the active amplifier
  - this has the effect of increasing the bandwidth, since the gain of the feedback amplifier remains constant as the gain of the active amplifier falls
  - however, when the open-loop gain is no longer much greater than the closed-loop gain the overall gain falls

– therefore the bandwidth *increases* as the gain is *reduced* with feedback

– in some cases the **gain x bandwidth = constant**



- **Effects on input and output resistance**
  - Negative feedback can either *increase* or *decrease* the input or output resistance depending on how it is used.
    - if the output voltage is fed back this tends to make the output voltage more stable by *decreasing* the output resistance
    - if the output current is fed back this tends to make the output current more stable by *increasing* the output resistance
    - if a voltage related to the output is subtracted from the input voltage this *increases* the input resistance
    - if a current related to the output is subtracted from the input current this *decreases* the input resistance
    - the factor by which the resistance changes is $(1 + AB)$

- **Effects on distortion and noise**
  - many forms of **distortion** are caused by a non-linear amplitude response
    - that is, the gain varies with the amplitude of the signal
  - since feedback tends to stabilise the gain it also tends to reduce distortion - often by a factor of $(1 + AB)$
  - **noise** produced *within* an amplifier is also reduced by negative feedback – again by a factor of $(1 + AB)$
    - note that noise already corrupting the input signal is *not* reduced in this way – this is amplified along with the signal

Contd…

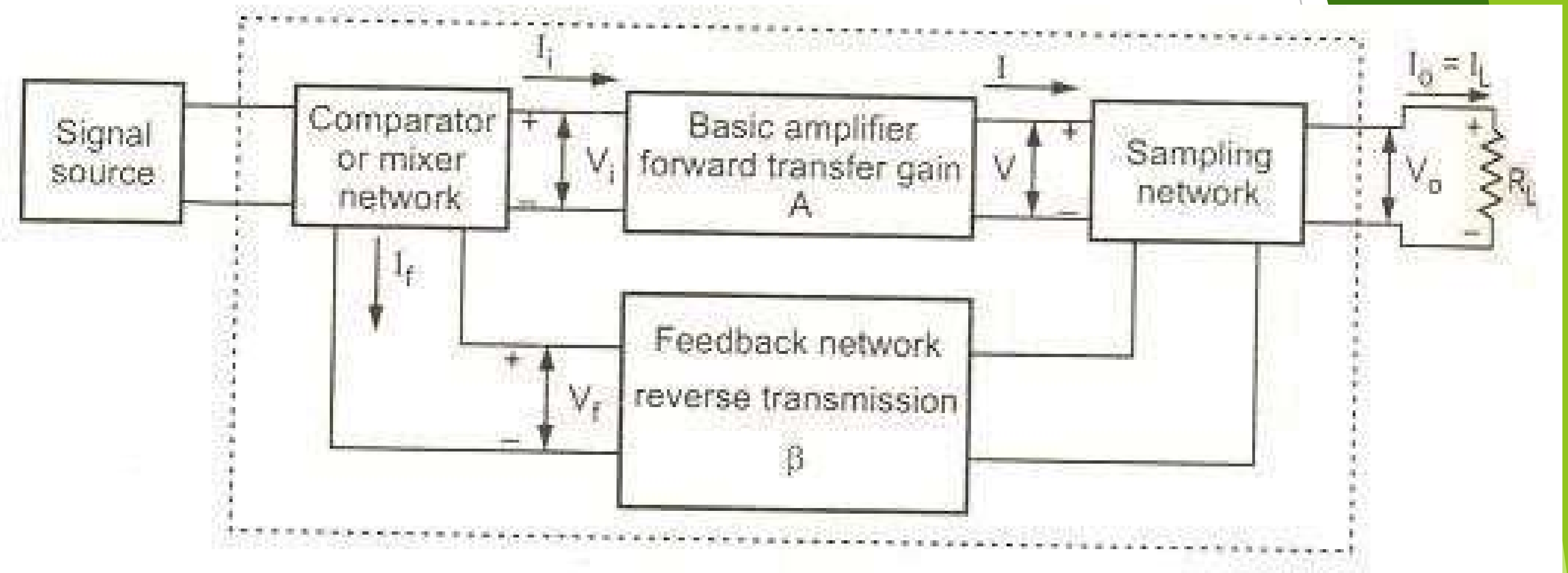
Extend bandwidth of amplifier

1. The product o voltage gain and bandwidth of an amplifier without feedback and with feedback remains the same.i.e., $A_{f.}(B.W_f) = A. (B.W)$

Contd…

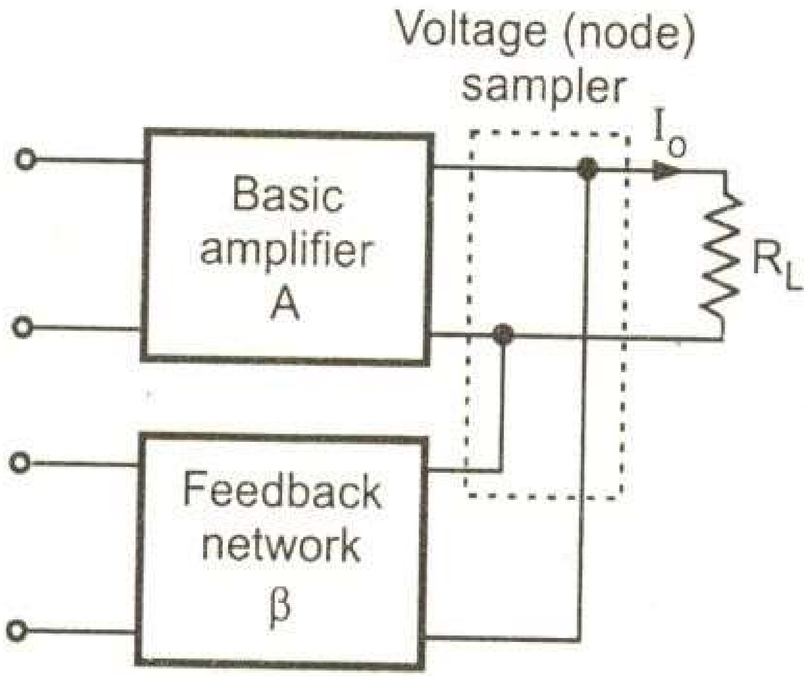
- Reduce nonlinear distortion : output proportional to input (constant gain independent of signal level)
- Reduce effect of noise
- Control input and output impedances by applying appropriate feedback topologies

Application of Negative Feedback

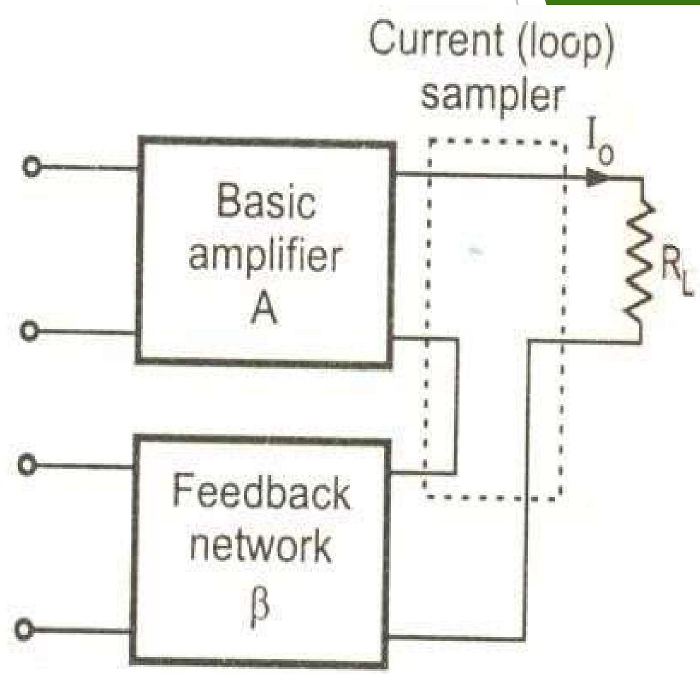


Types of Samplers

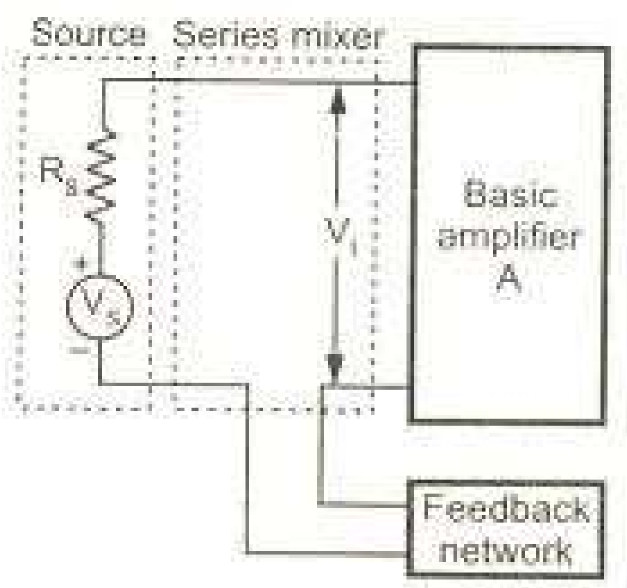
Voltage sampling networks

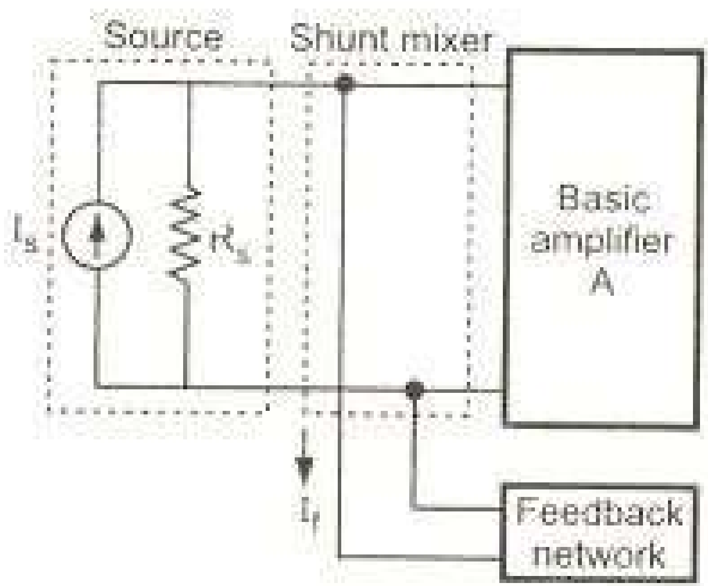


Current sampling network

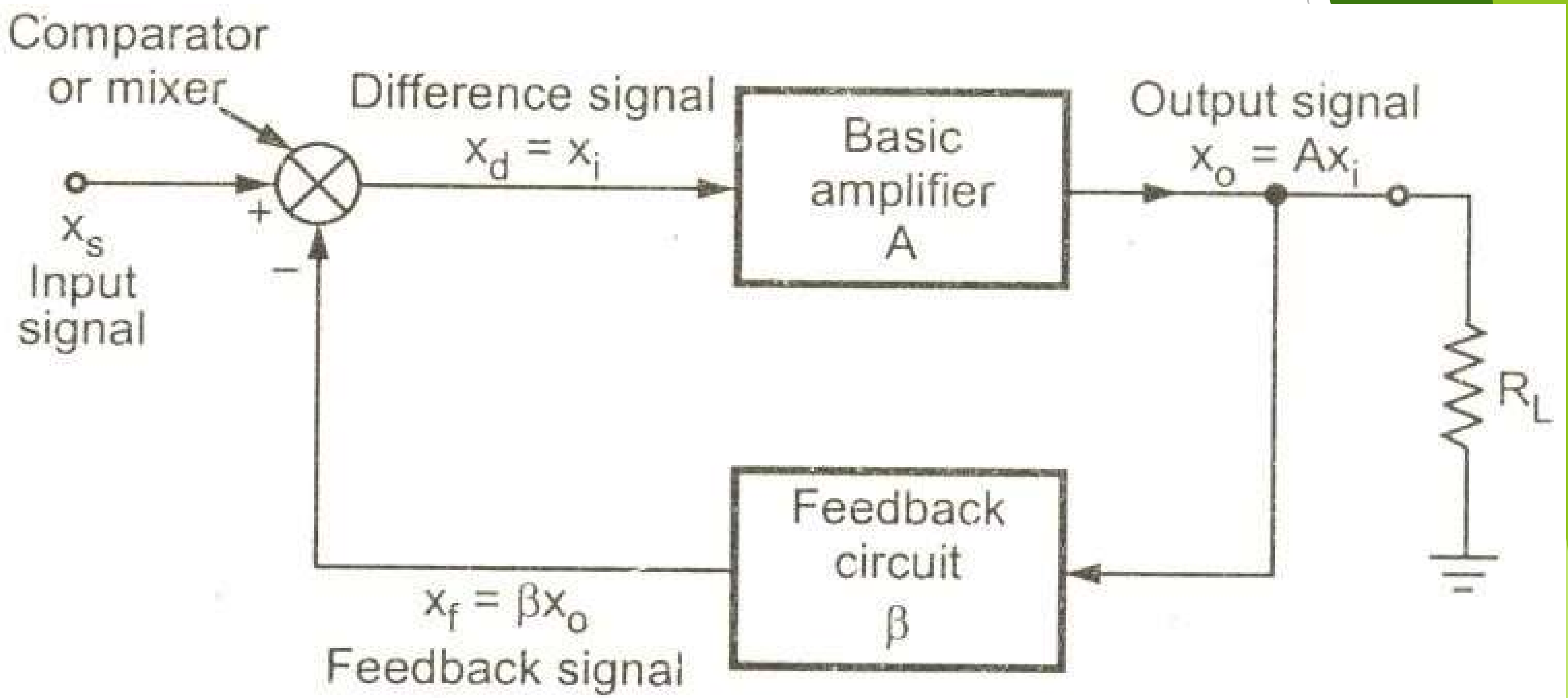


Types of Mixers





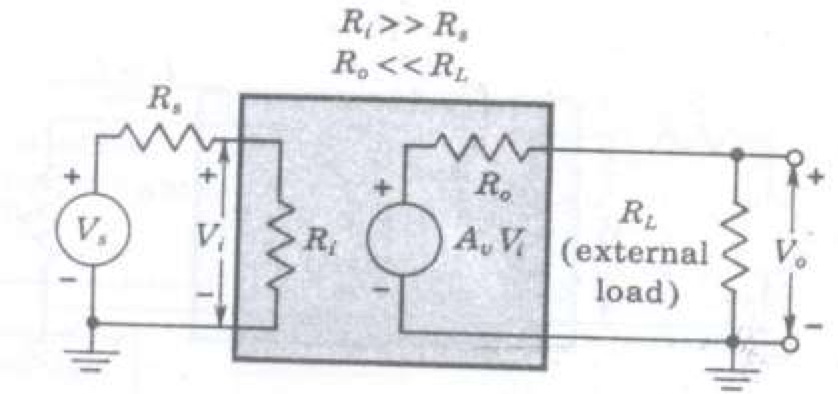
Ideal Single-Loop Feedback Amplifier



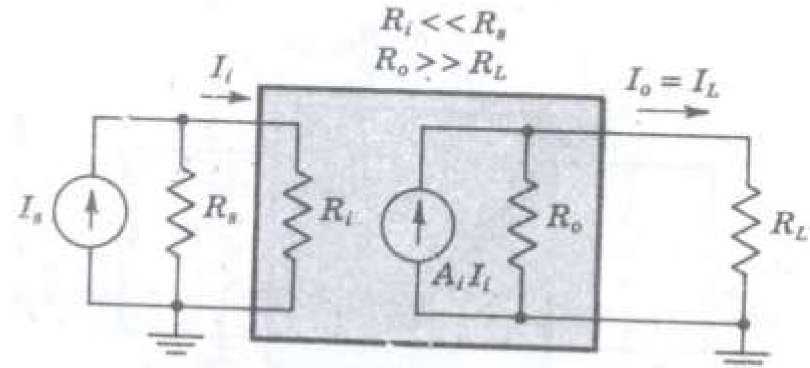
Classification of Amplifiers

- Based on the magnitudes of the of the input and output impedance, amplifiers are divided into four types.

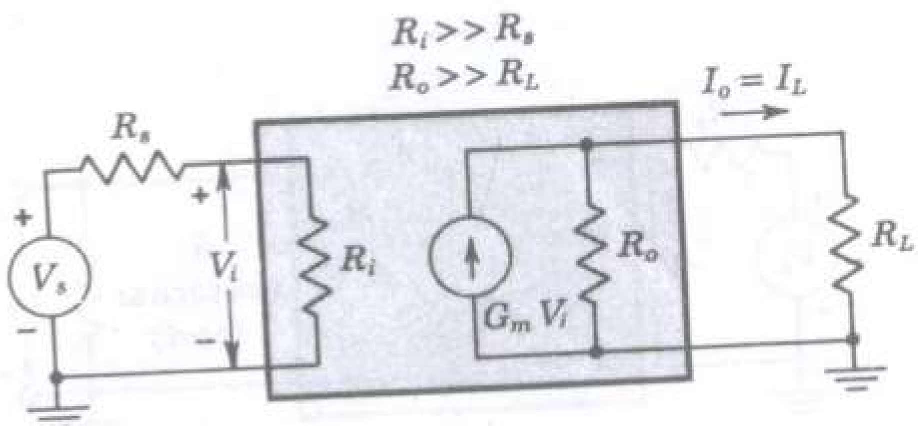
1. Voltage Amplifier
2. Current Amplifier
3. Transconductance Amplifier
4. Transresistance Amplifier



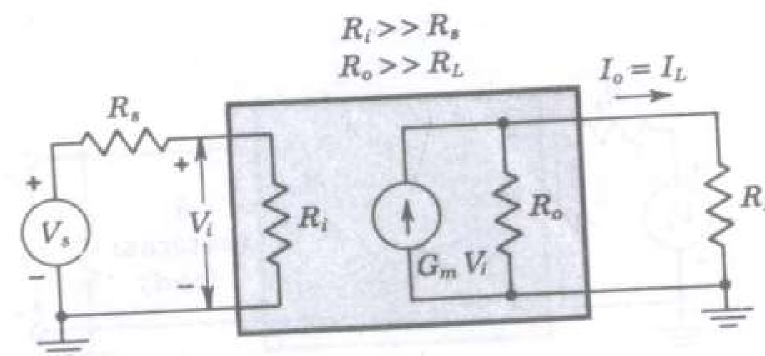
Voltage Amplifier



Current Amplifier



Transconductance Amplifier

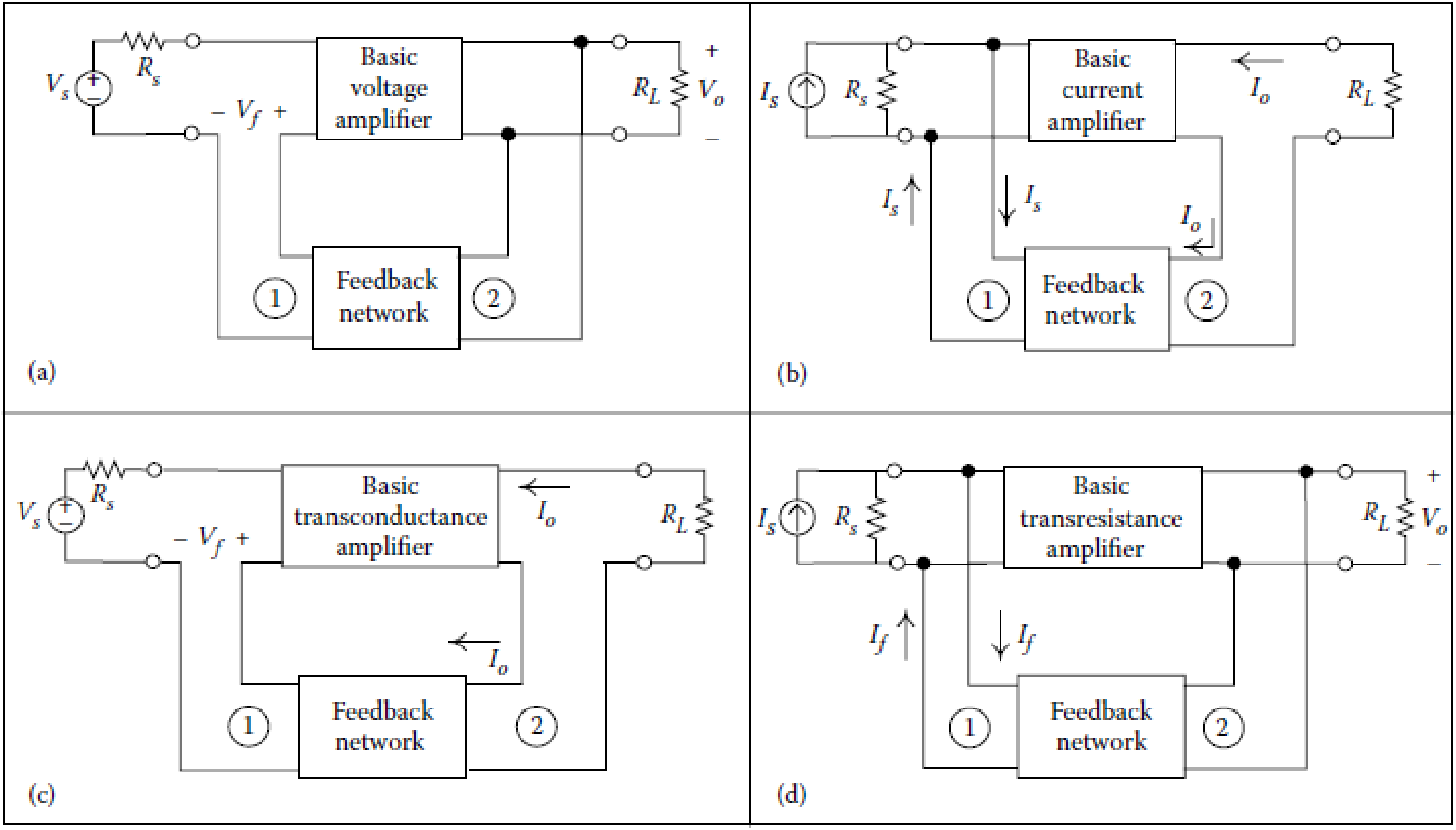


Transresistance Amplifier

Basic Feedback Topologies

Depending on the input signal (voltage or current) to be amplified and form of the output (voltage or current), amplifiers can be classified into four categories. Depending on the amplifier category, one of four types of feedback structures should be used.

(Type of Feedback)	**(Type of Sensing)**
(1) Series (Voltage)	Shunt (Voltage) (Voltage Amplifier)
(2) Series (Voltage)	Series (Current) (Transconductance Amplifier)
(3) Shunt (Current)	Shunt (Voltage) (Transresistance Amplifier)
(4) Shunt (Current)	Series (Current) (Current Amplifier)



The four basic feedback topologies: (a) voltage-sampling series mixing (series-shunt) topology; (b) current-sampling shunt mixing (shunt-series) topology; (c) current-sampling series-mixing (series-series) topology; (d) voltage-sampling shunt-mixing (shunt-shunt) topology.

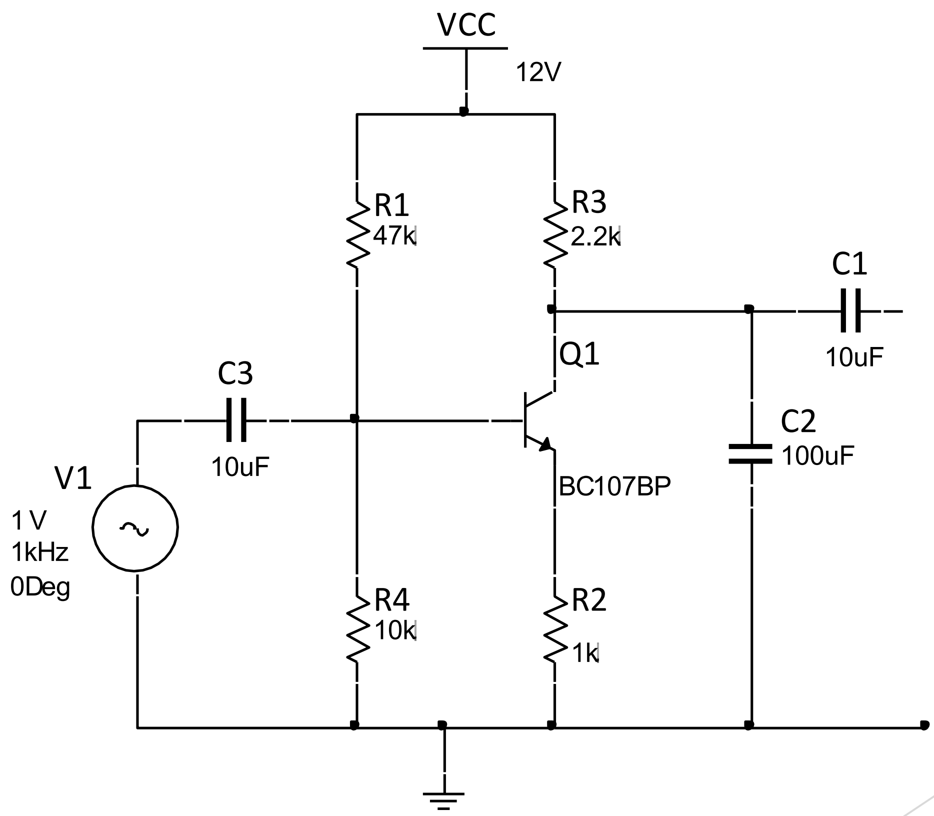
		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	A	$\frac{V_o}{V_i}$	$\frac{V_o}{I_i}$	$\frac{I_o}{V_i}$	$\frac{I_o}{I_i}$
Feedback	β	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$
Gain with feedback	A_f	$\frac{V_o}{V_s}$	$\frac{V_o}{I_s}$	$\frac{I_o}{V_s}$	$\frac{I_o}{I_s}$

Type of feedback	Input impedance (1+Aβ)	Output impedance (1+Aβ)
Voltage Series	Increased	Decreased
Voltage Shunt	Decreased	Decreased
Current Shunt	Decreased	Increased
Current Series	Increased	Increased

Feedback Amplifier

Feedback amplifier	**Source signal**	**Output signal**	**Transfer function**	**Input Resistance**	**Output Resistance**
Series-Shunt (voltage amplifier)	Voltage	Voltage	$A_{vf} = \frac{A_v}{1+\beta_v A_v}$	$(1+\beta_v A_v)R_i$	$\frac{R_o}{(1+\beta_v A_v)}$
Shunt-Series (current amplifier)	Current	Current	$A_{if} = \frac{A_i}{1+\beta_i A_i}$	$\frac{R_i}{(1+\beta_i A_i)}$	$(1+\beta_i A_i)R_o$
Series-Series (transconductance amplifier)	Voltage	Current	$A_{gf} = \frac{A_g}{1+\beta_g A_g}$	$(1+\beta_g A_g)R_i$	$(1+\beta_g A_g)R_o$
Shunt-Shunt (transresistance amplifier)	Current	Voltage	$A_{zf} = \frac{A_z}{1+\beta_z A_z}$	$\frac{R_i}{(1+\beta_z A_z)}$	$\frac{R_o}{(1+\beta_z A_z)}$

Voltage Series Feedback Amplifier(Practical)



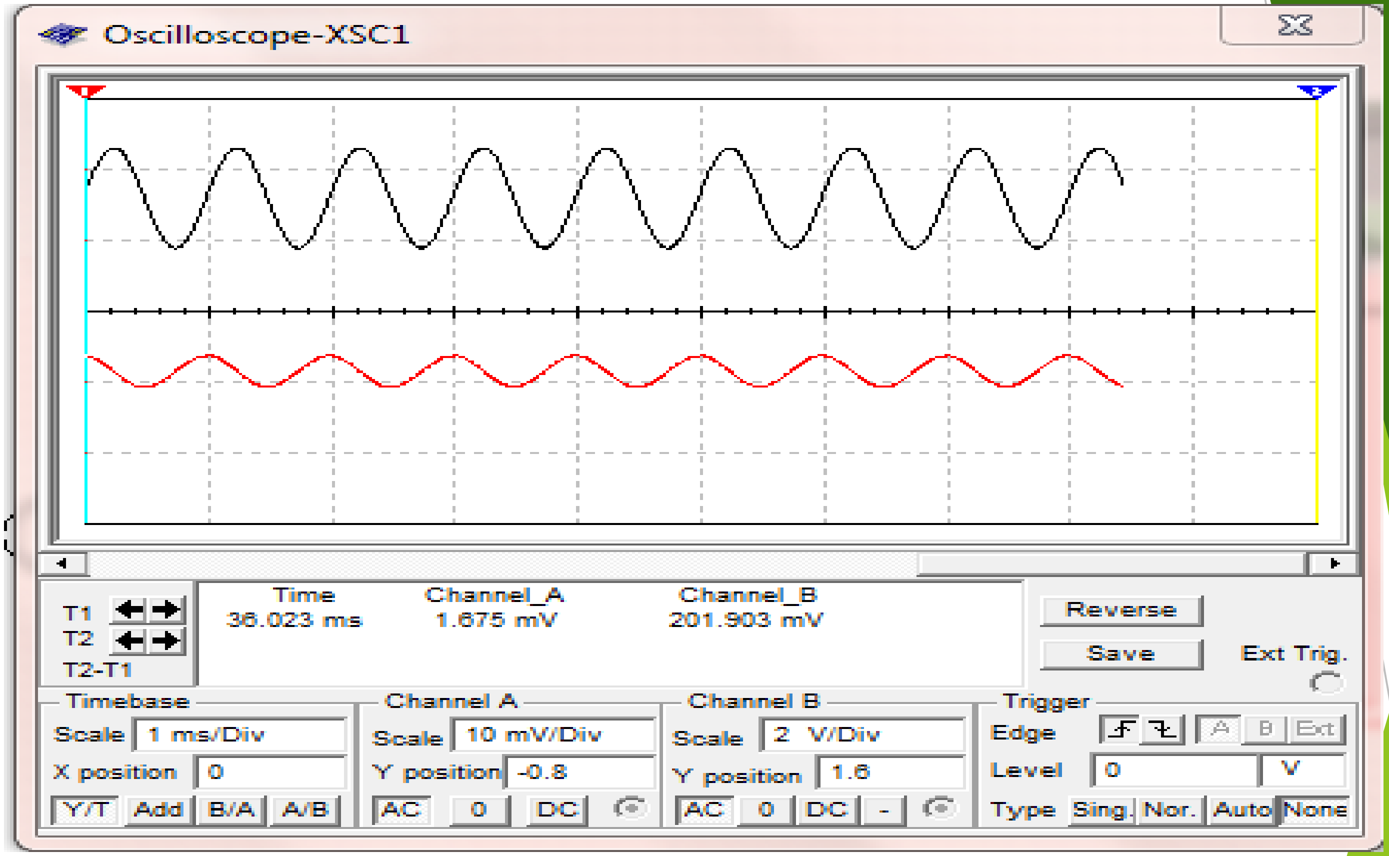


Fig: Transient response

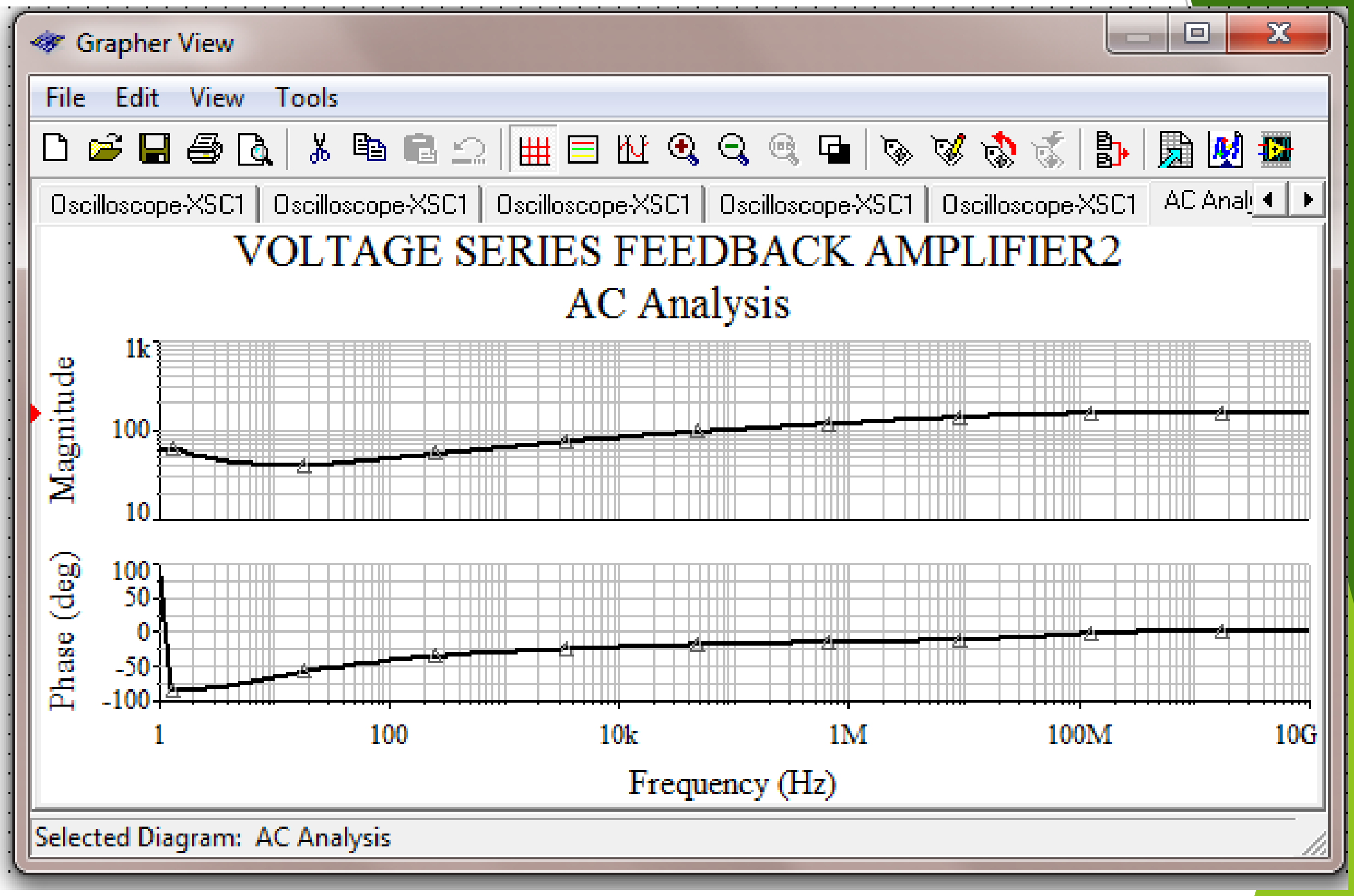
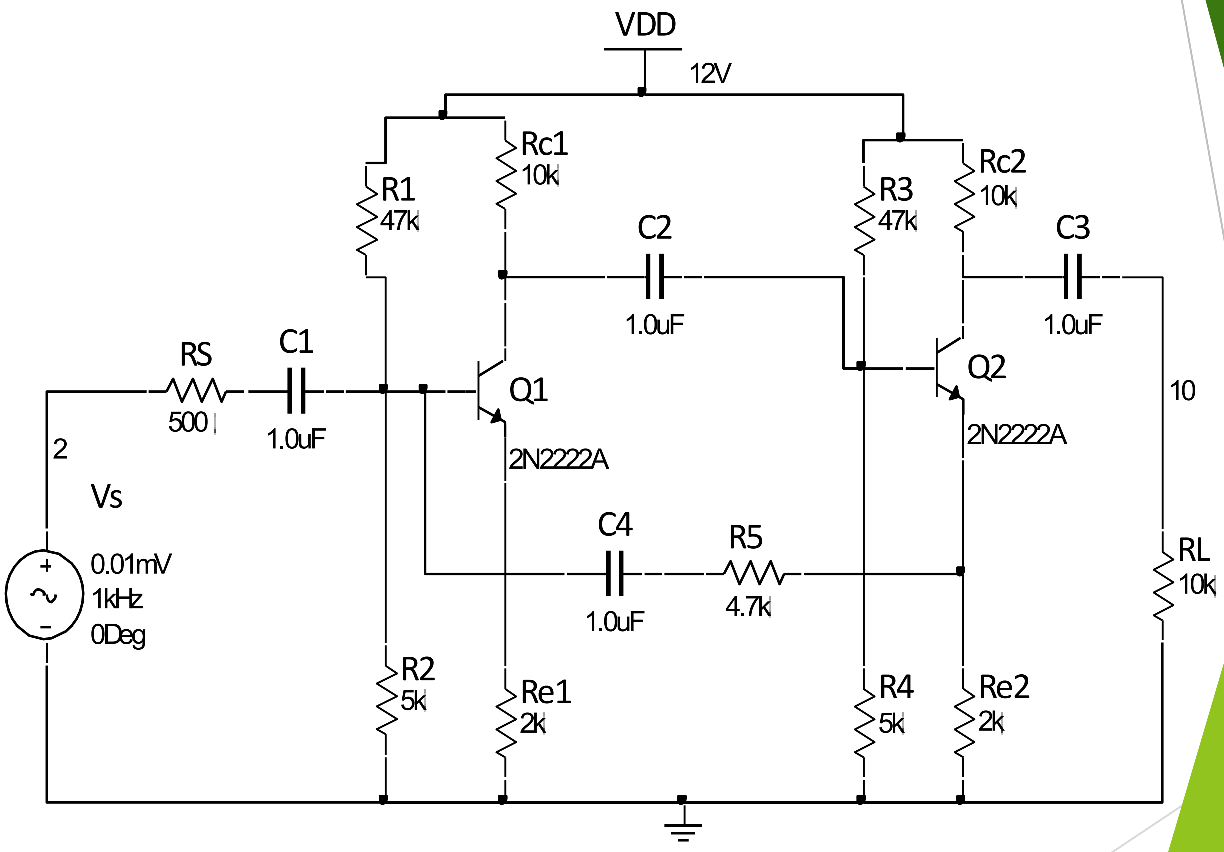


Fig: Frequency Response

Current Shunt Feedback Amplifier(Practical)



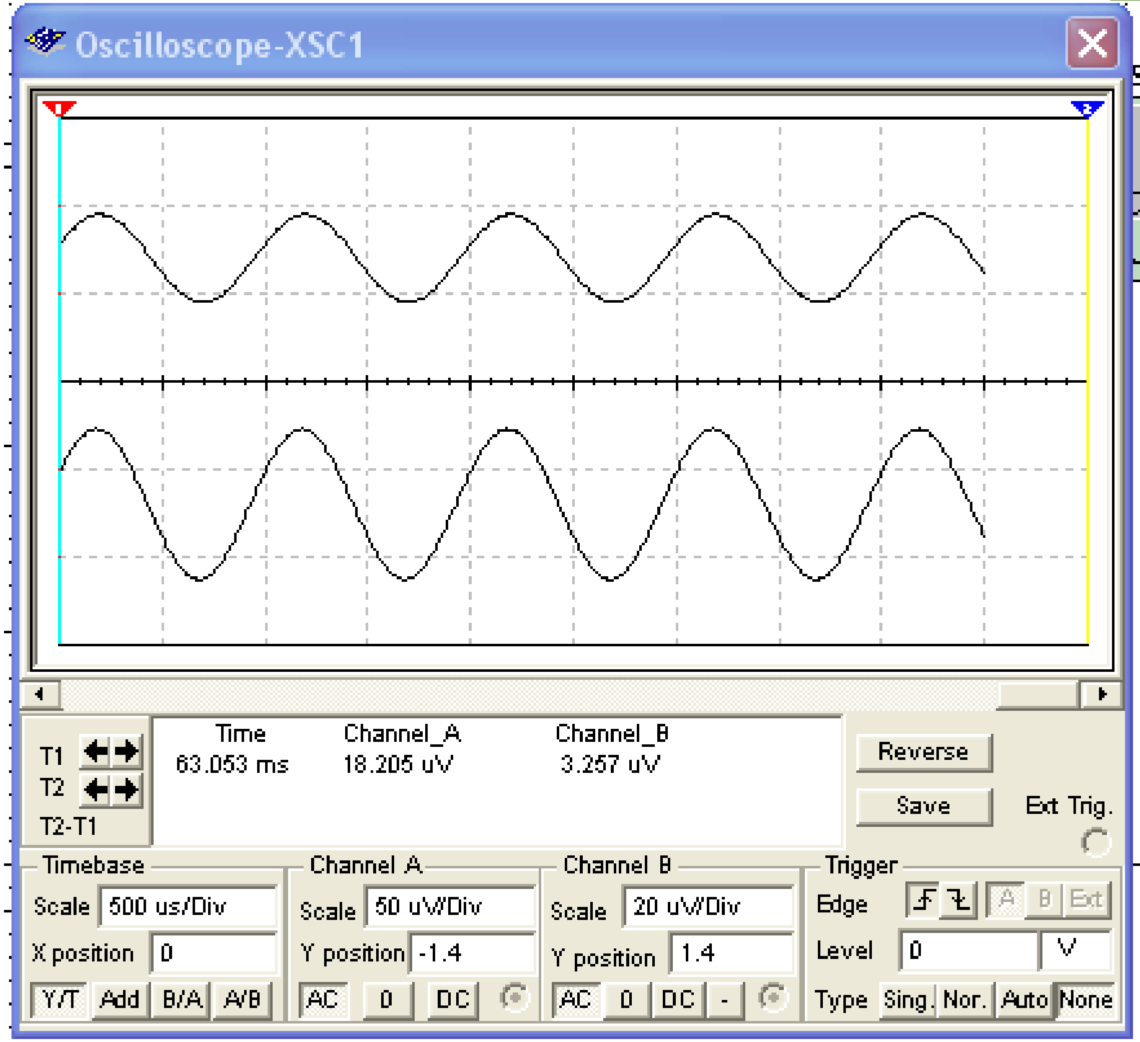


Fig: Transient Response

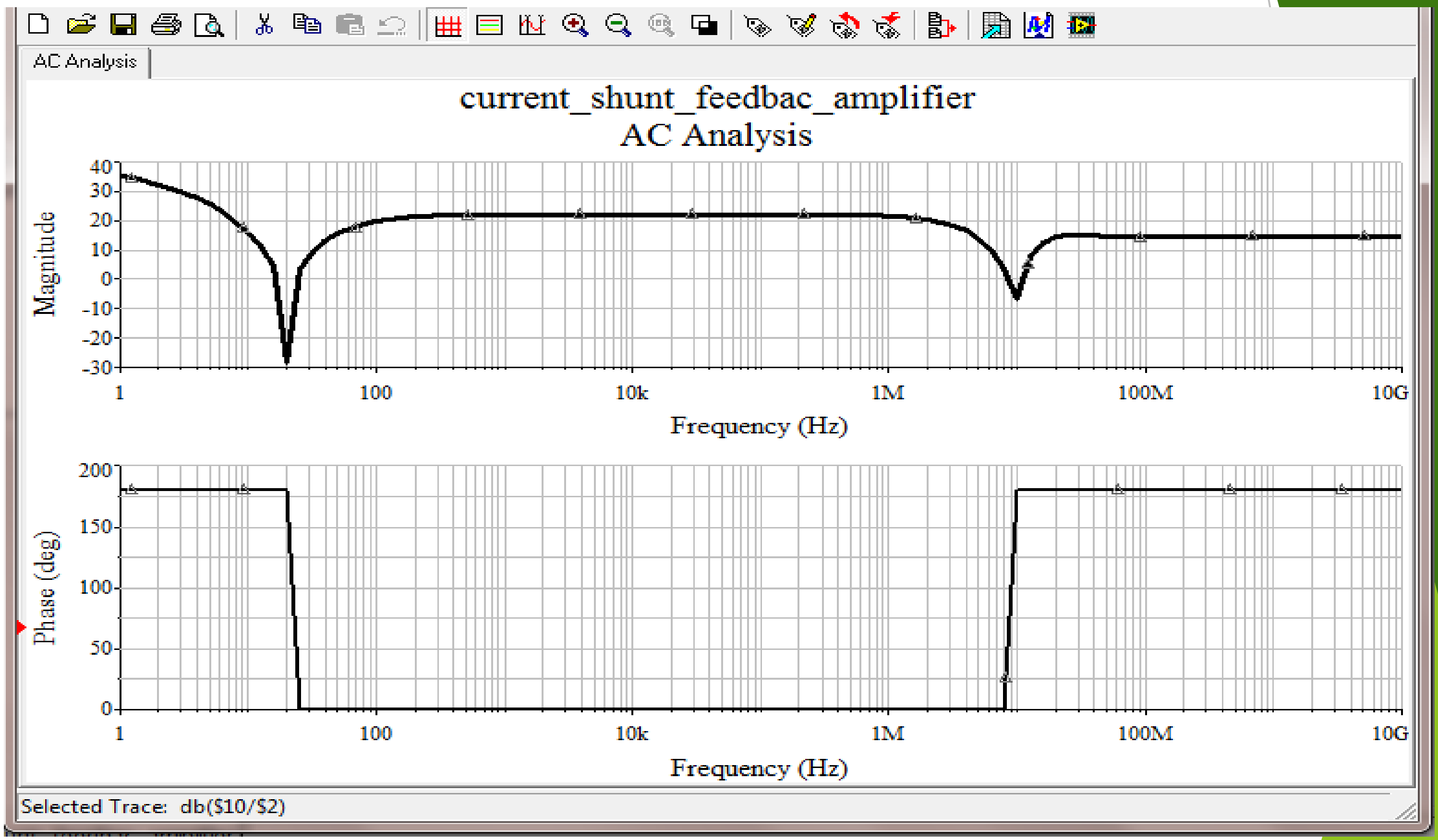


Fig: Frequency Response

Methodology

Step 1: Identify topology. (Type of feedback).

To find the type of sampling network

- By shorting the output i.e., Vo=0, if feedback signal (X_f) becomes zero then we can say that it is "Voltage Sampling".
- By opening the output loop i.e., Io=0, if feedback signal (X_f) becomes zero then we can say that it is "Current Sampling".

To find the type of mixing network.

- If the feedback signal is subtracted from the input voltage source, then we can say that it is "Series Mixing".
- If the feedback signal is subtracted from the input current source, then we can say that it is "Shunt Mixing".

Step 2: To find the input circuit.

For voltage sampling Vo=0

For current sampling Io=0

Step 3: To find the output circuit.

For series mixing $I_i=0$

For shunt mixing $V_i=0$

Step 4: Replace the active device by its h-parameter model at low frequency.

Step 5: Find the open loop gain (without feedback), 'A' of the amplifier.

Step 6: Indicate X_f and Xo on the circuit and evaluate.

Step 7: From 'A' and 'β' find A_f, R_{if}, R_{of}.

Feedback

For negative feedback: $\beta A > 0$; For positive feedback: $\beta A < 0$

Advantages of Negative feedback

➢ Negative feedback can reduce the gain of the amplifier, but it has many advantages, such as gain stabilization, reduction of nonlinear distortion and noise, control of input and output impedances, and extension of bandwidth.

❑ Gain stabilization

$$A_f = \frac{A}{(1+\beta A)}$$

$$\frac{dA_f}{A} = \frac{1}{(1+\beta A)^2}$$

$$\frac{dA_f}{A_f} = \frac{1}{(1+\beta A)}\frac{dA}{A}$$

Therefore percentage change in A_f *(due to variations in some* circuit parameter) is reduced by (1+βA) times compared to without feedback.

UNIT-II:
BJT & FET Frequency Response

BJT and FET Frequency Response Characteristics:

- *Logarithms and Decibels:*

Logarithms taken to the base 10 are referred to as *common logarithms,* while logarithms taken to the base e are referred to as *natural logarithms*. In summary: Some relationships hold true for logarithms to any base

$$\boxed{\text{Common logarithm:} \quad x = \log_{10} a}$$

$$\boxed{\text{Natural logarithm:} \quad y = \log_e a}$$

The two are related by

$$\boxed{\log_e a = 2.3 \log_{10} a}$$

Some relationships hold true for logarithms to any base

$$\boxed{\log_{10} 1 = 0}$$

$$\boxed{\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b}$$

$$\boxed{\log_{10} \frac{1}{b} = -\log_{10} b}$$

$$\boxed{\log_{10} ab = \log_{10} a + \log_{10} b}$$

The background surrounding the term *decibel* (dB) has its origin in the established fact that power and audio levels are related on a logarithmic basis.

That is, an increase in power level, say 4 to 16 W, does not result in an audio level increase by a factor of 16/4 = 4. It will increase by a factor of 2 as derived from the power of 4 in the following manner: $(4)^2 = 16$.

The term *bel* was derived from the surname of Alexander Graham Bell. For standardization, the bel (B) was defined by the following equation to relate power levels P_1 and P_2:

$$\boxed{G = \log_{10} \frac{P_2}{P_1}} \quad \text{bel}$$

There exists a second equation for decibels that is applied frequently. It can be best described through the system with R_i, as an input resistance.

$$G_{dB} = 10 \log_{10} \frac{P_2}{P_1} = 10 \log_{10} \frac{V_2^2/R_i}{V_1^2/R_i} = 10 \log_{10} \left(\frac{V_2}{V_1}\right)^2$$

and

$$\boxed{G_{dB} = 20 \log_{10} \frac{V_2}{V_1}} \quad \text{dB}$$

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages. In words, the equation states that the decibel gain of a cascaded system is simply the sum of the decibel gains of each stage.

General Frequency Considerations:

- The frequency of the applied signal can have a pronounced effect on the response of a single-stage or multistage network. The analysis thus far has been for the mid frequency spectrum.
- At low frequencies, we shall find that the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements.
- The frequency-dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system.
- An increase in the number of stages of a cascaded system will also limit both the high- and low-frequency responses.

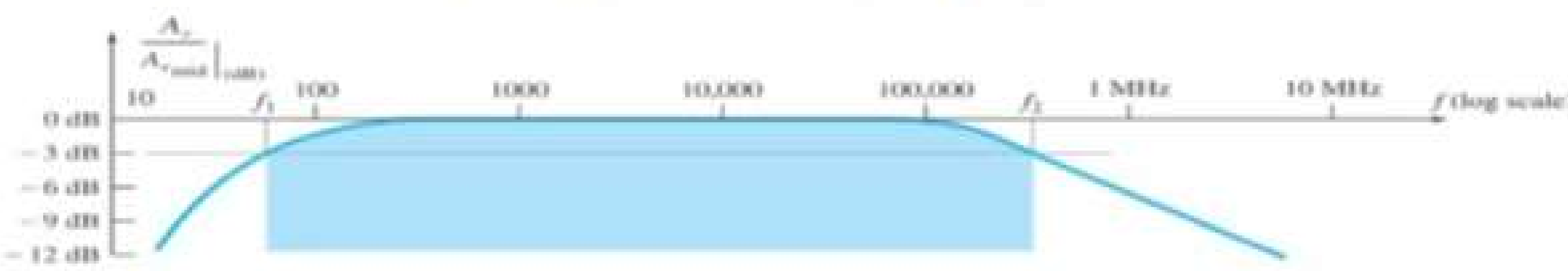
- For any system, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the mid band value.
- To fix the frequency boundaries of relatively high gain, $0.707A_{v\text{mid}}$ was chosen to be the gain at the cutoff levels.
- The corresponding frequencies f_1 and f_2 are generally called the *corner, cutoff, band, break*, or *half-power frequencies*.
- The multiplier 0.707 was chosen because at this level the output power is half the mid band power output, that is, at mid frequencies.

- The bandwidth (or pass band) of each system is determined by f_1 and f_2, that is,

$$\text{bandwidth (BW)} = f_2 - f_1$$

- For applications of a communications nature (audio, video), a decibel plot of the voltage gain versus frequency is more useful.
- Before obtaining the logarithmic plot, however, the curve is generally normalized as shown in this figure, the gain at each frequency is divided by the mid band value. Obviously, the mid band value is then 1 as indicated. At the half-power frequencies, the resulting level is 0.707= 1/. 2

- **Fig. Normalized gain versus frequency plot.**



- **Fig. Decibel plot of the normalized gain versus frequency plot**

General Frequency Considerations

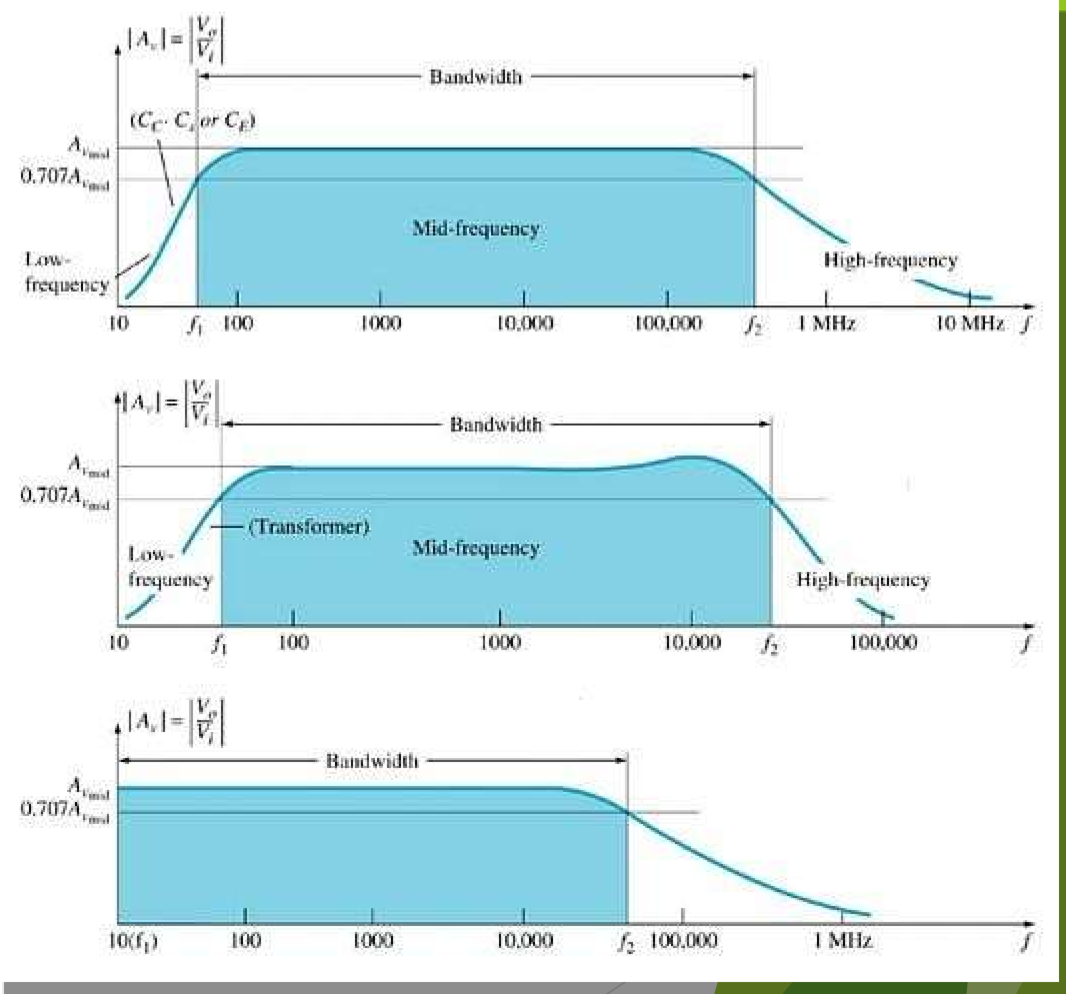
The **frequency response** of an amplifier refers to the frequency range in which the amplifier will operate with negligible effects from capacitors and device internal capacitance. This range of frequencies can be called the **mid-range**.

- At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier.
- At low frequencies the coupling and bypass capacitors lower the gain.
- At high frequencies stray capacitances associated with the active device lower the gain.
- Also, cascading amplifiers limits the gain at high and low frequencies.

Bode Plot

A Bode plot indicates the frequency response of an amplifier.

The horizontal scale indicates the frequency (in Hz) and the vertical scale indicates the gain (in dB).

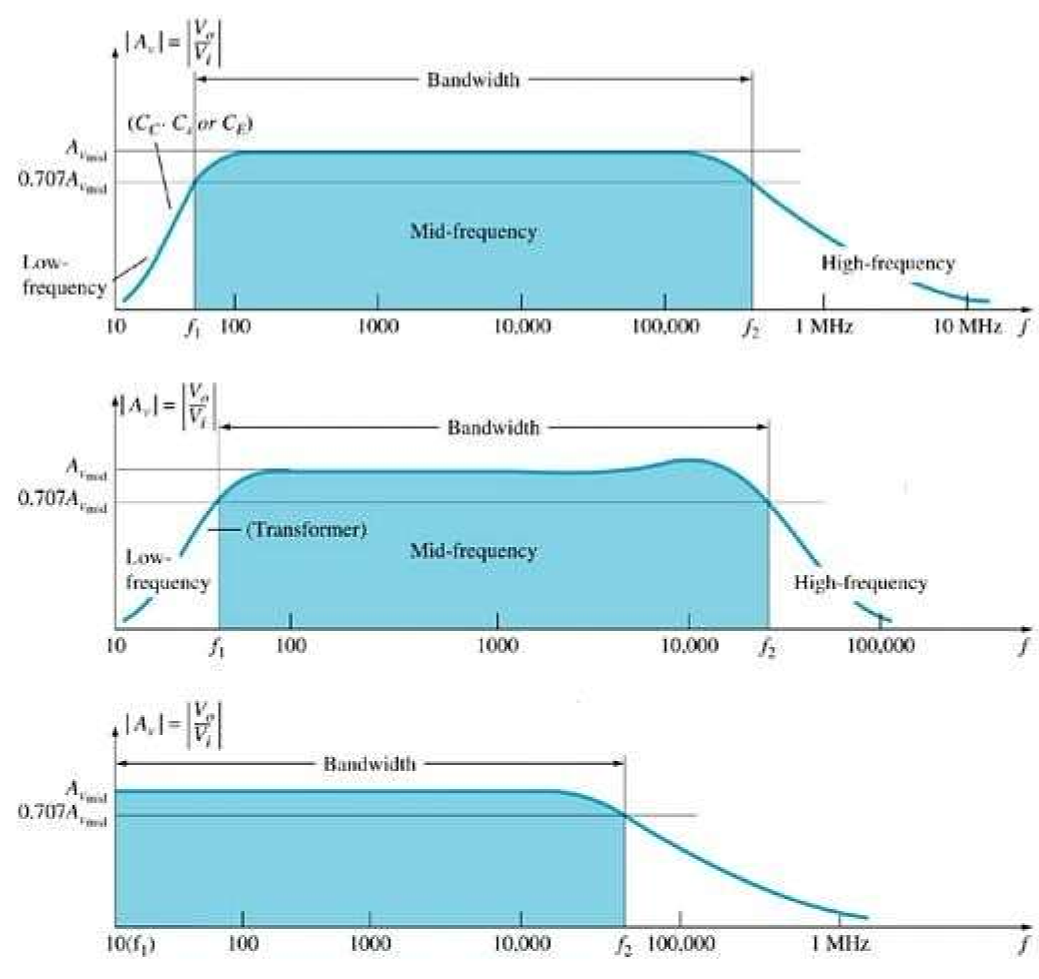


Cutoff Frequencies

The mid-range frequency range of an amplifier is called the bandwidth of the amplifier.

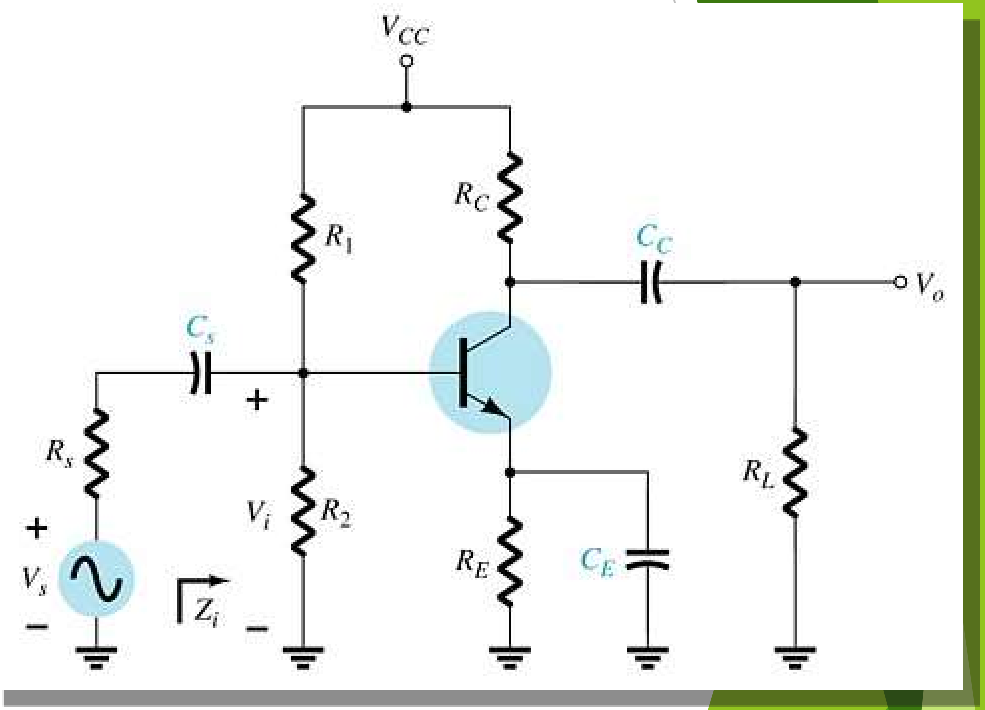
The bandwidth is defined by the lower and upper cutoff frequencies.

Cutoff – any frequency at which the gain has dropped by 3 dB.



BJT Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_S, C_C) and bypass capacitor (C_E) reactances affect the circuit impedances.



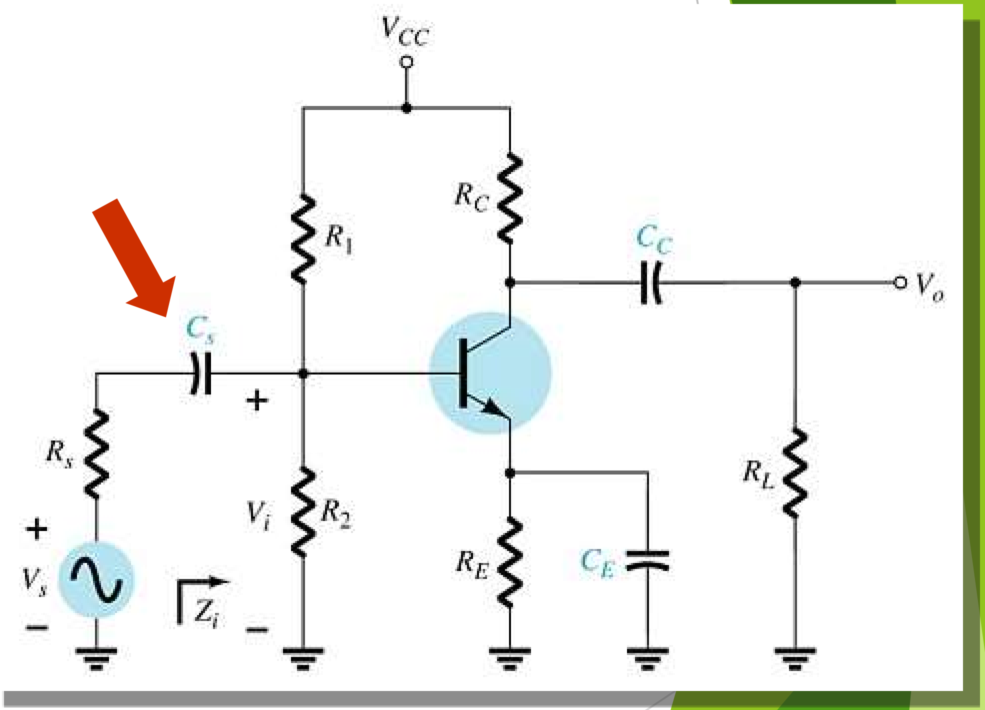
Coupling Capacitor (C_S)

The cutoff frequency due to C_S can be calculated by

$$f_{Ls} = \frac{1}{2\pi(R_s + R_i)C_s}$$

where

$$R_i = R_1 \parallel R_2 \parallel \beta r_e$$



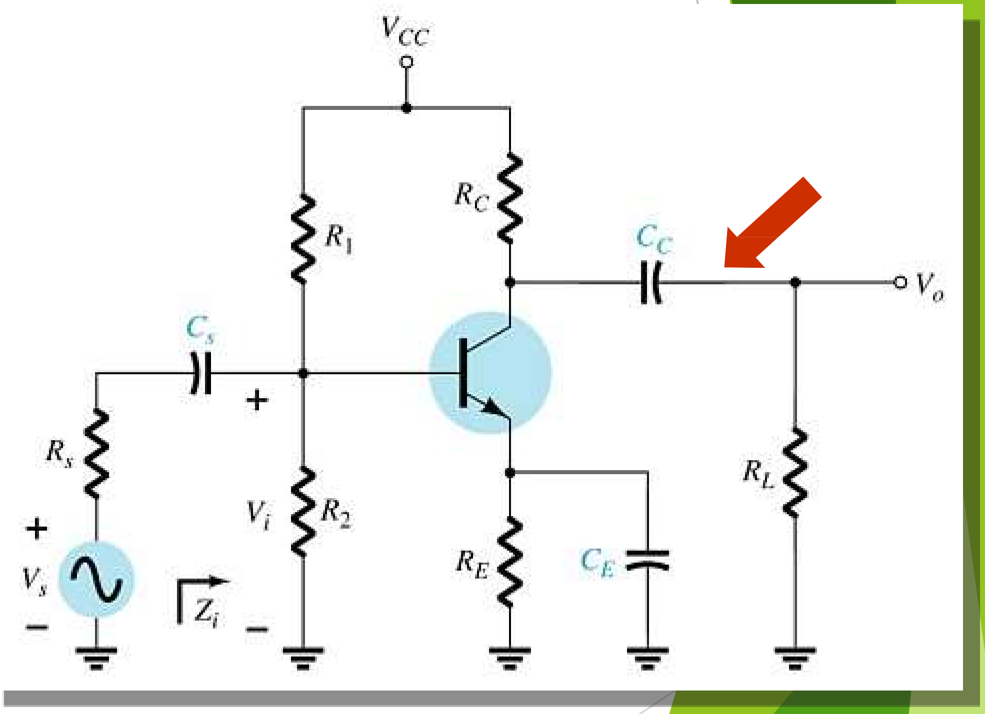
Coupling Capacitor (C_C)

The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_c}$$

where

$$R_o = R_C \parallel r_o$$



Bypass Capacitor (C_E)

The cutoff frequency due to C_E can be calculated with

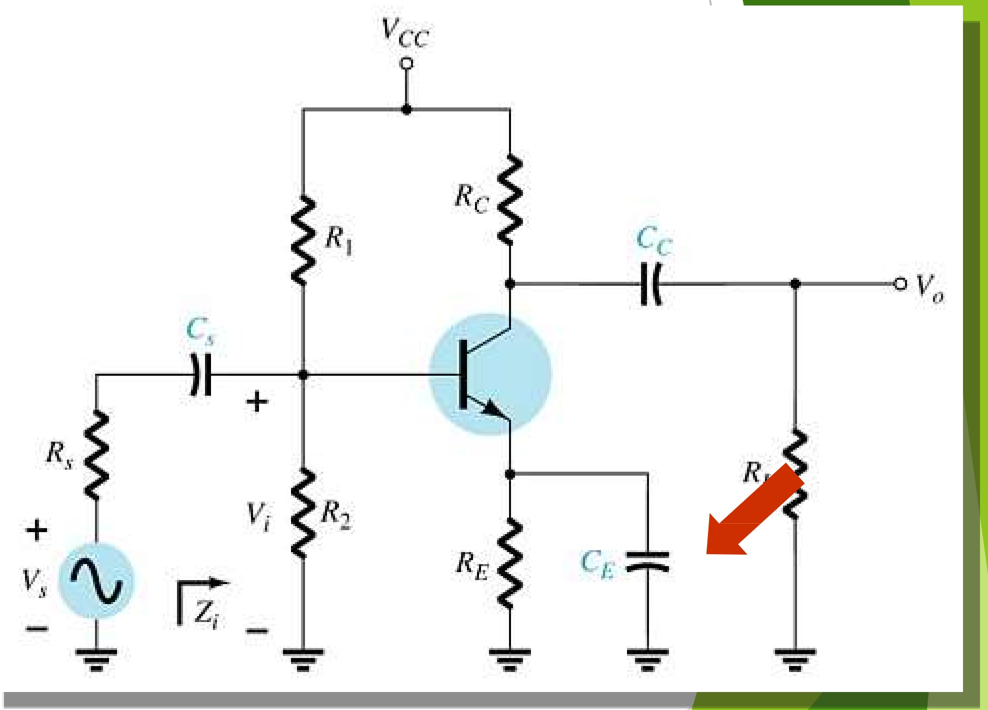
$$f_{LE} = \frac{1}{2\pi R_e C_E}$$

where

$$R_e = R_E \parallel \left(\frac{R'_s}{\beta} + r_e\right)$$

and

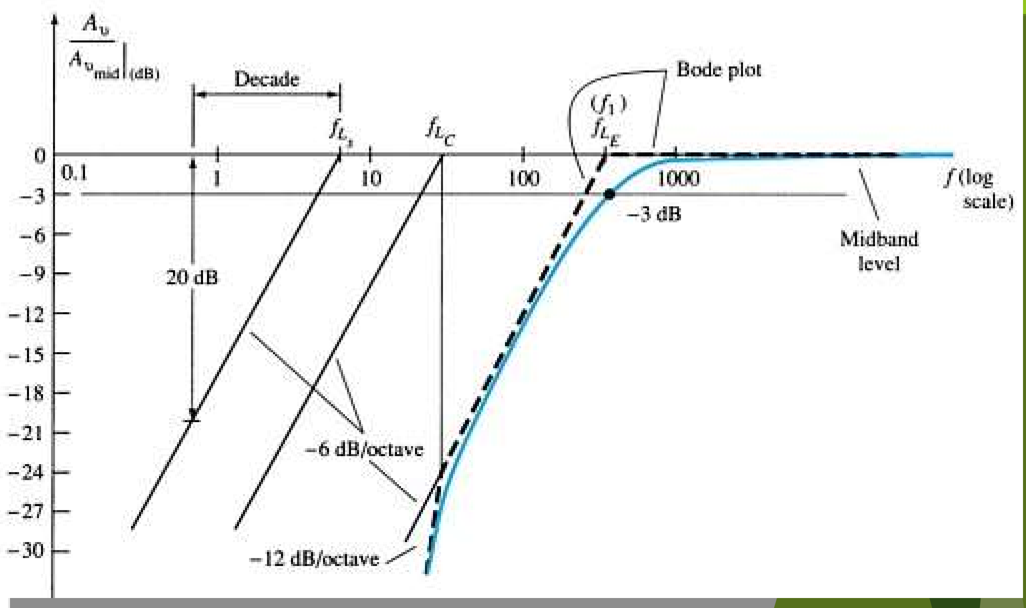
$$R'_s = R_s \parallel R_1 \parallel R_2$$



BJT Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

It is the device that has the *highest* lower cutoff frequency (f_L) that dominates the overall frequency response of the amplifier.

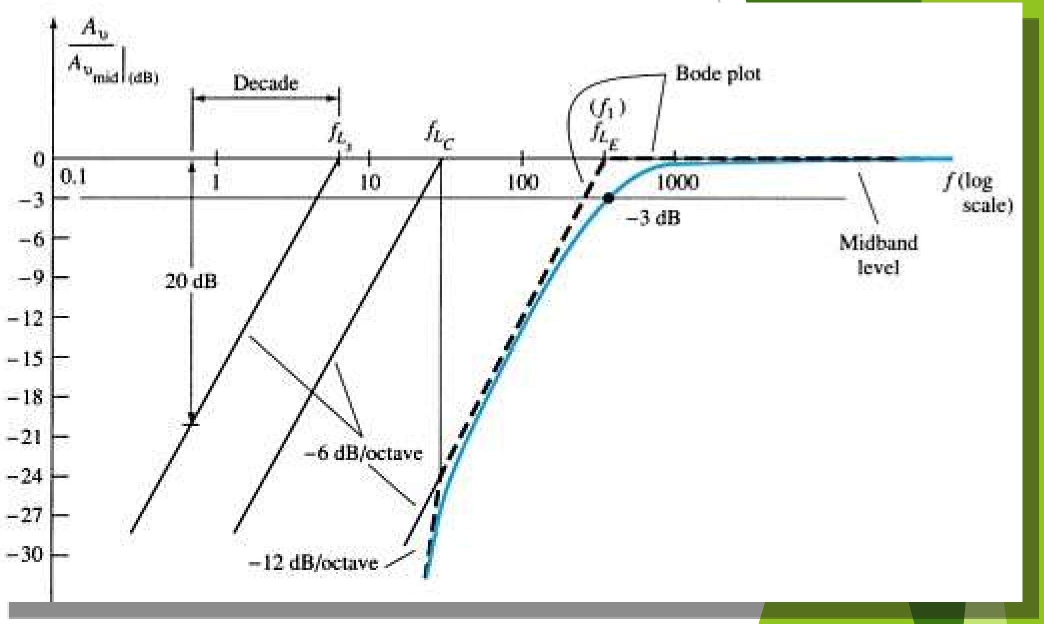


Roll-Off of Gain in the Bode Plot

The Bode plot not only indicates the cutoff frequencies of the various capacitors it also indicates the amount of attenuation (loss in gain) at these frequencies.

The amount of attenuation is sometimes referred to as **roll-off**.

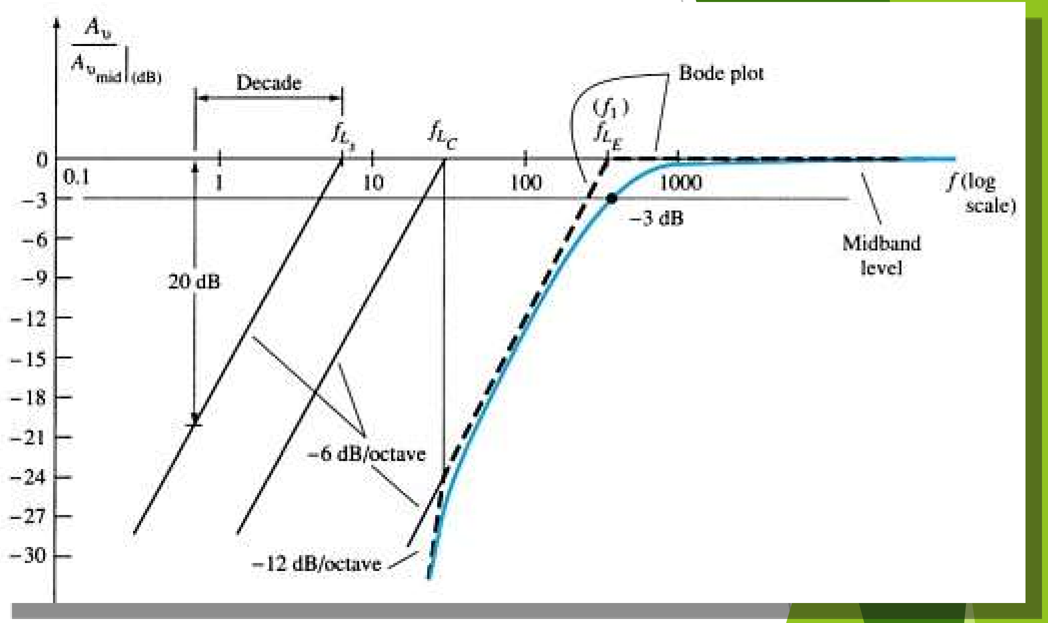
The roll-off is described as dB loss-per-octave or dB loss-per-decade.



Roll-off Rate (-dB/Decade)

-dB/decade refers to the attenuation for every 10-fold change in frequency.

For attenuations at the low-frequency end, it refers to the loss in gain from the lower cutoff frequency to a frequency that is one-tenth the cutoff value.

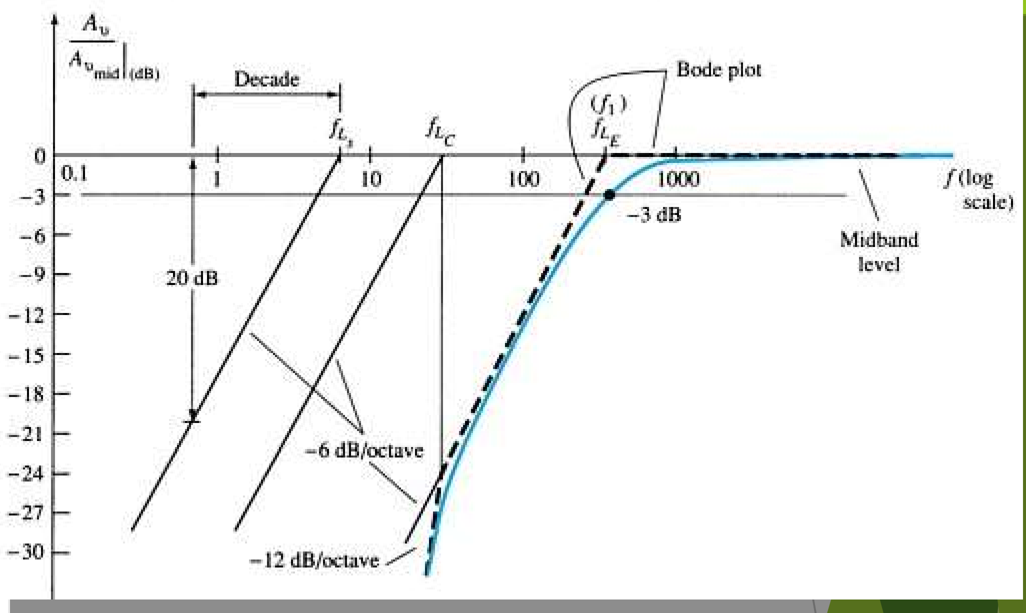


In this example:

f_{LS} = 9kHz gain is 0dB
f_{LS}/10 = .9kHz gain is –20dB
Thus the roll-off is 20dB/decade
The gain decreases by –20dB/decade

Roll-Off Rate (–dB/Octave)

-dB/octave refers to the attenuation for every 2-fold change in frequency.
For attenuations at the low-frequency end, it refers to the loss in gain from the lower cutoff frequency to a frequency one-half the cutoff value.



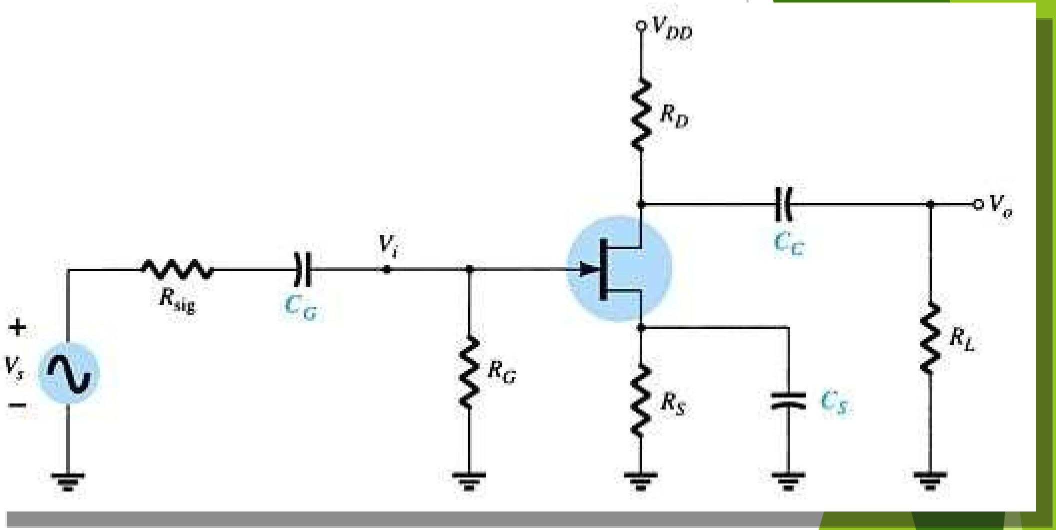
In this example:

f_{LS} = 9kHz gain is 0dB
f_{LS} / 2 = 4.5kHz gain is –6dB
Therefore the roll-off is 6dB/octave.

This is a little difficult to see on this graph because the horizontal scale is a logarithmic scale.

FET Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_G, C_C) and bypass capacitor (C_S) reactances affect the circuit impedances.



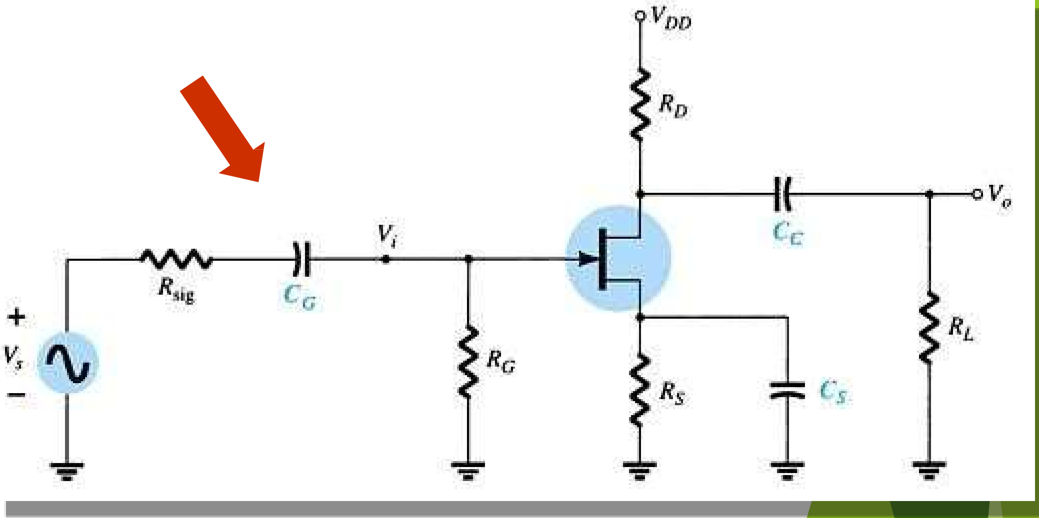
Coupling Capacitor (C_G)

The cutoff frequency due to C_G can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_{sig} + R_i)C_G}$$

where

$$R_i = R_G$$



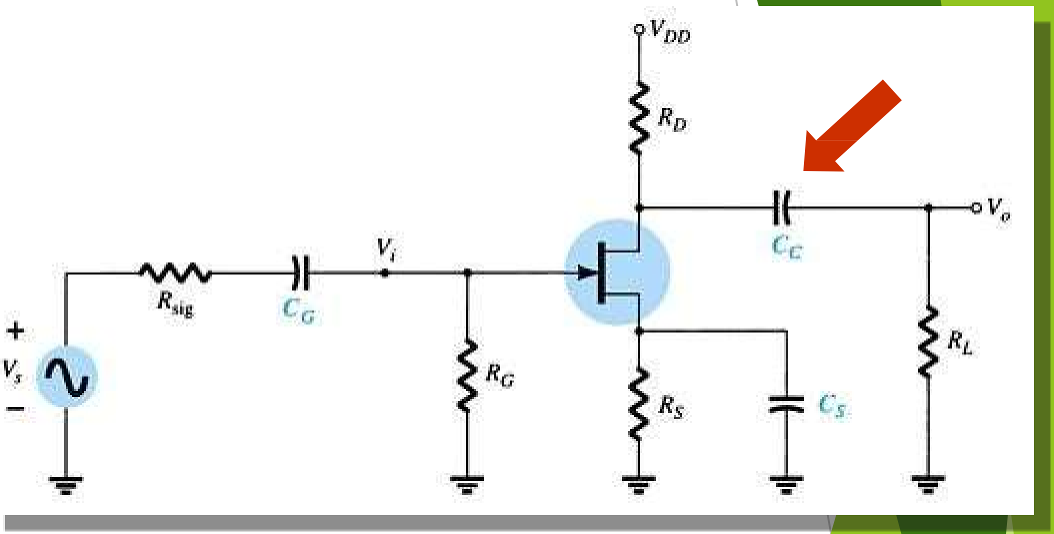
Coupling Capacitor (C_C)

The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_C}$$

where

$$R_o = R_D \parallel r_d$$



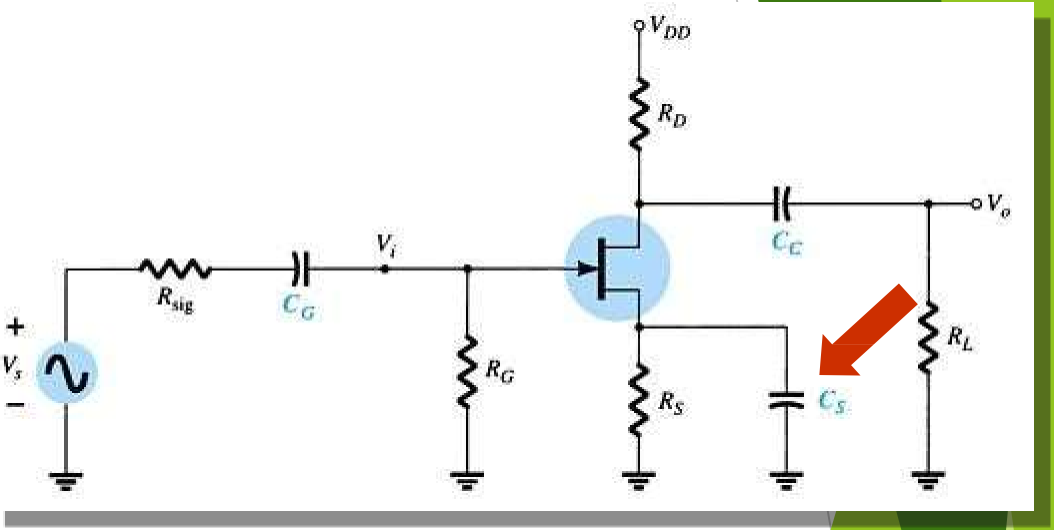
Bypass Capacitor (C_S)

The cutoff frequency due to C_S can be calculated with

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S}$$

where

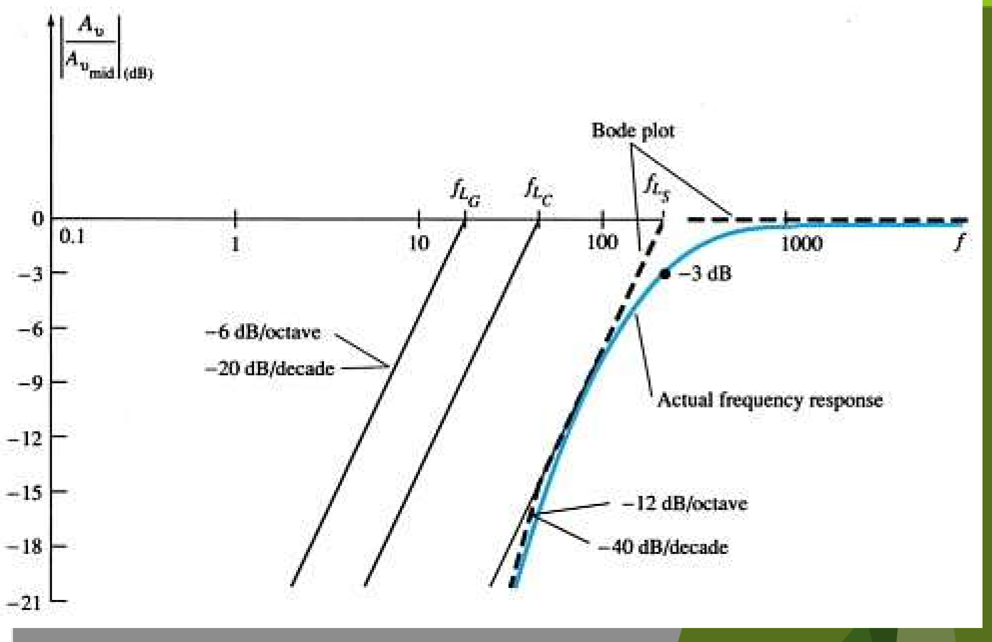
$$R_{eq} = R_S \,||\, \frac{1}{g_m}\Big|_{r_d \cong \infty\Omega}$$



FET Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

The capacitor that has the *highest* lower cutoff frequency (f_L) is closest to the actual cutoff frequency of the amplifier.



Miller Capacitance

Any *p-n* junction can develop capacitance. In a BJT amplifier, this capacitance becomes noticeable across:

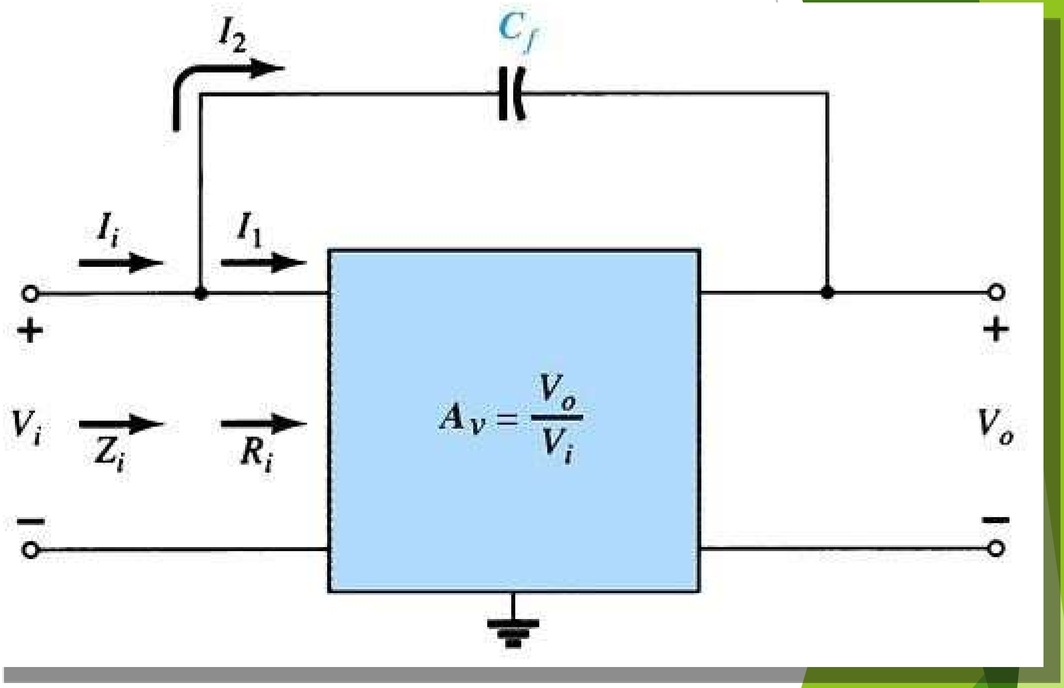
- **The base-collector junction at high frequencies in common-emitter BJT amplifier configurations**
- **The gate-drain junction at high frequencies in common-source FET amplifier configurations.**

These capacitances are represented as separate input and output capacitances, called the Miller Capacitances.

Miller Input Capacitance (C_{Mi})

$$C_{Mi} = (1 - A_v)C_f$$

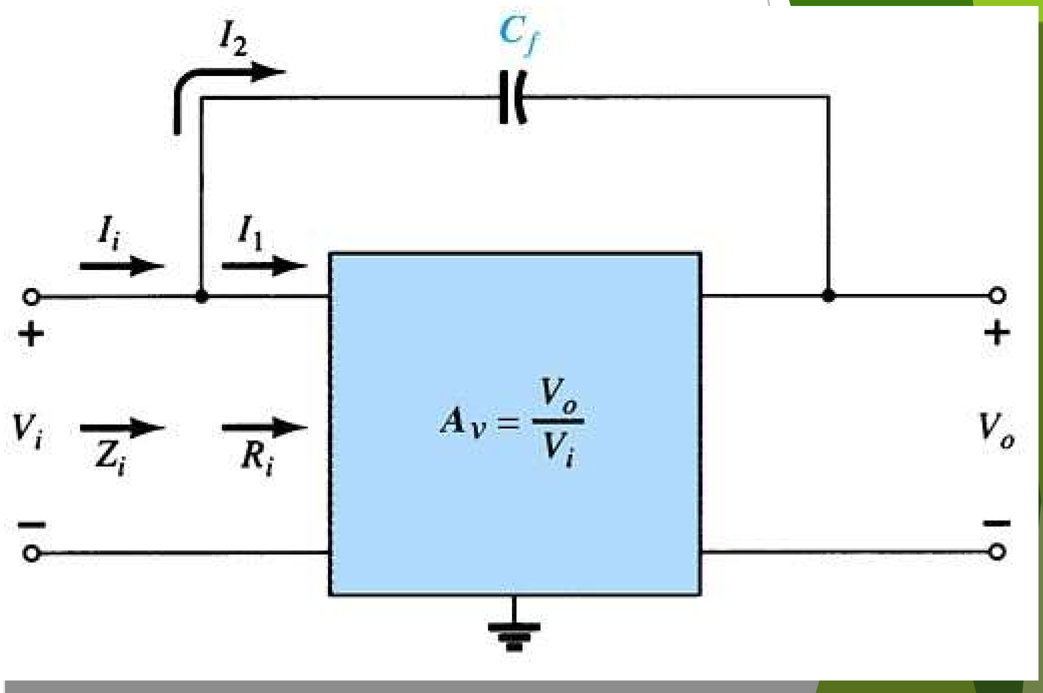
Note that the amount of Miller capacitance is dependent on inter-electrode capacitance from input to output (C_f) and the gain (A_v).



Miller Output Capacitance (C_{Mo})

If the gain (A_v) is considerably greater than 1, then

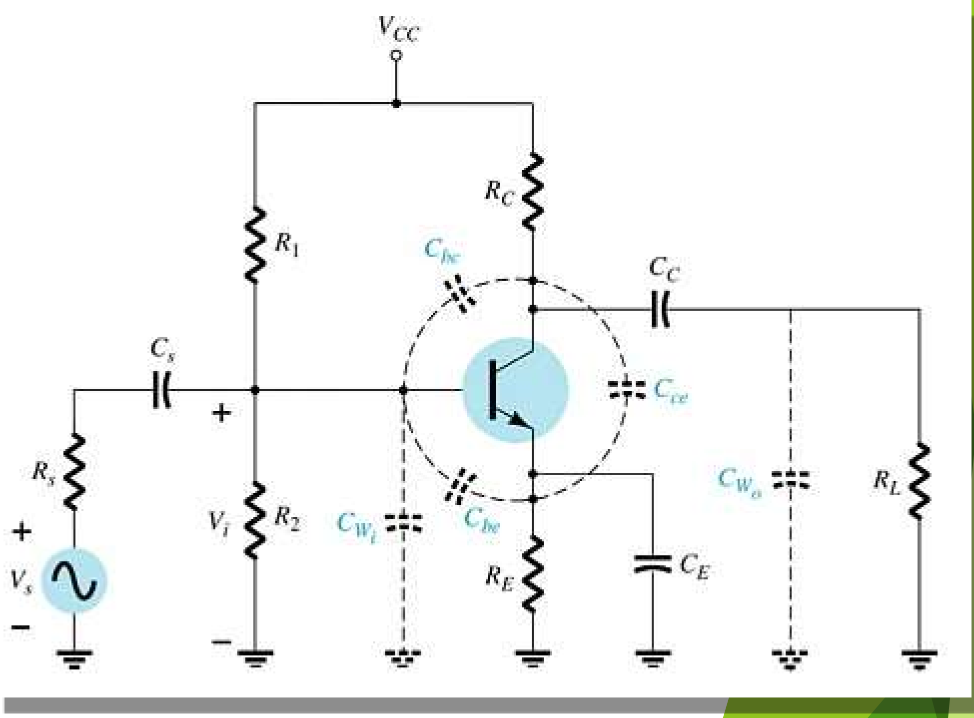
$$C_{Mo} \cong C_f$$



BJT Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- Junction capacitances C_{be}, C_{bc}, C_{ce}
- Wiring capacitances C_{wi}, C_{wo}
- Coupling capacitors C_S, C_C
- Bypass capacitor C_E



Input Network (f_{Hi}) High-Frequency Cutoff

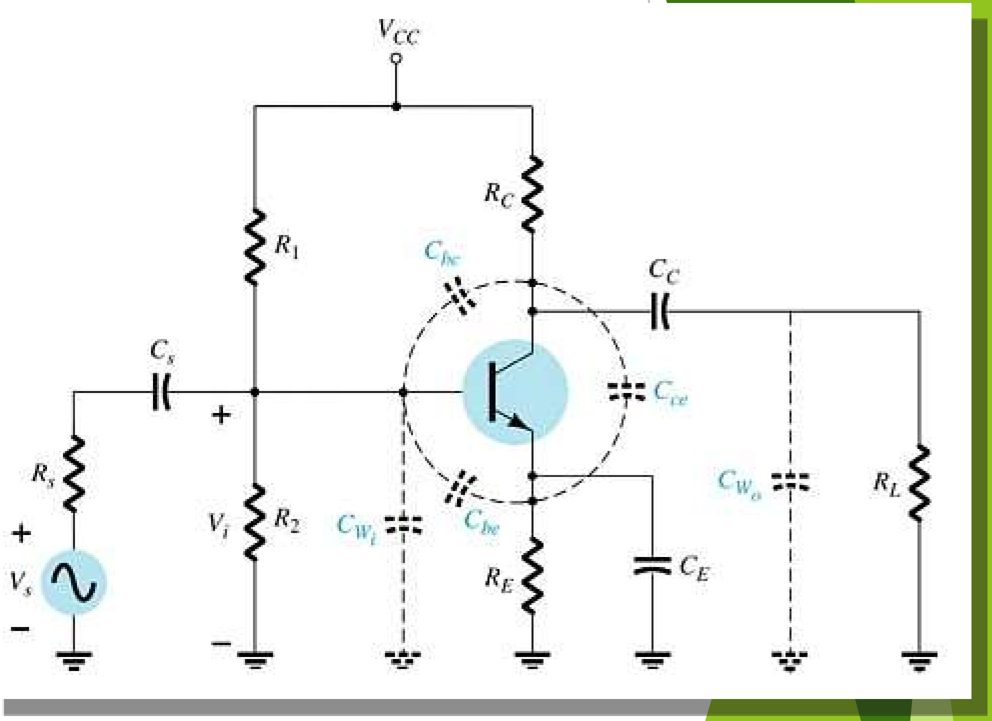
$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

where

$$R_{Thi} = R_s || R_1 \; || \; R_2 \; || \; R_i$$

and

$$C_i = C_{Wi} + C_{be} + C_{Mi}$$
$$= C_{Wi} + C_{be} + (1 - A_v) C_{bc}$$



Output Network (f_{Ho}) High-Frequency Cutoff

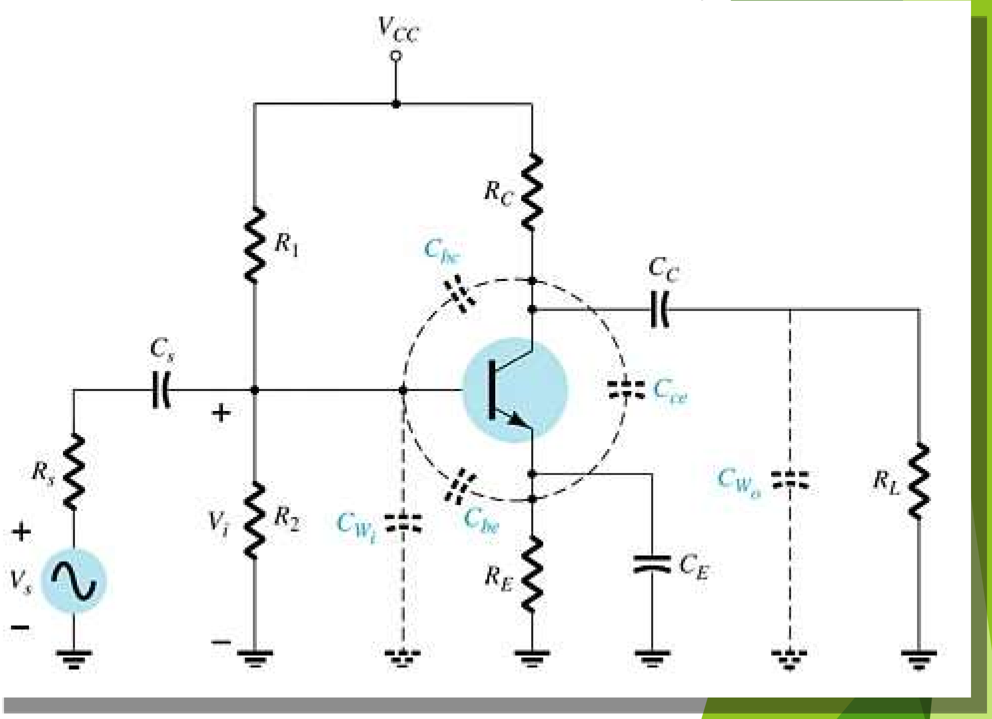
$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

where

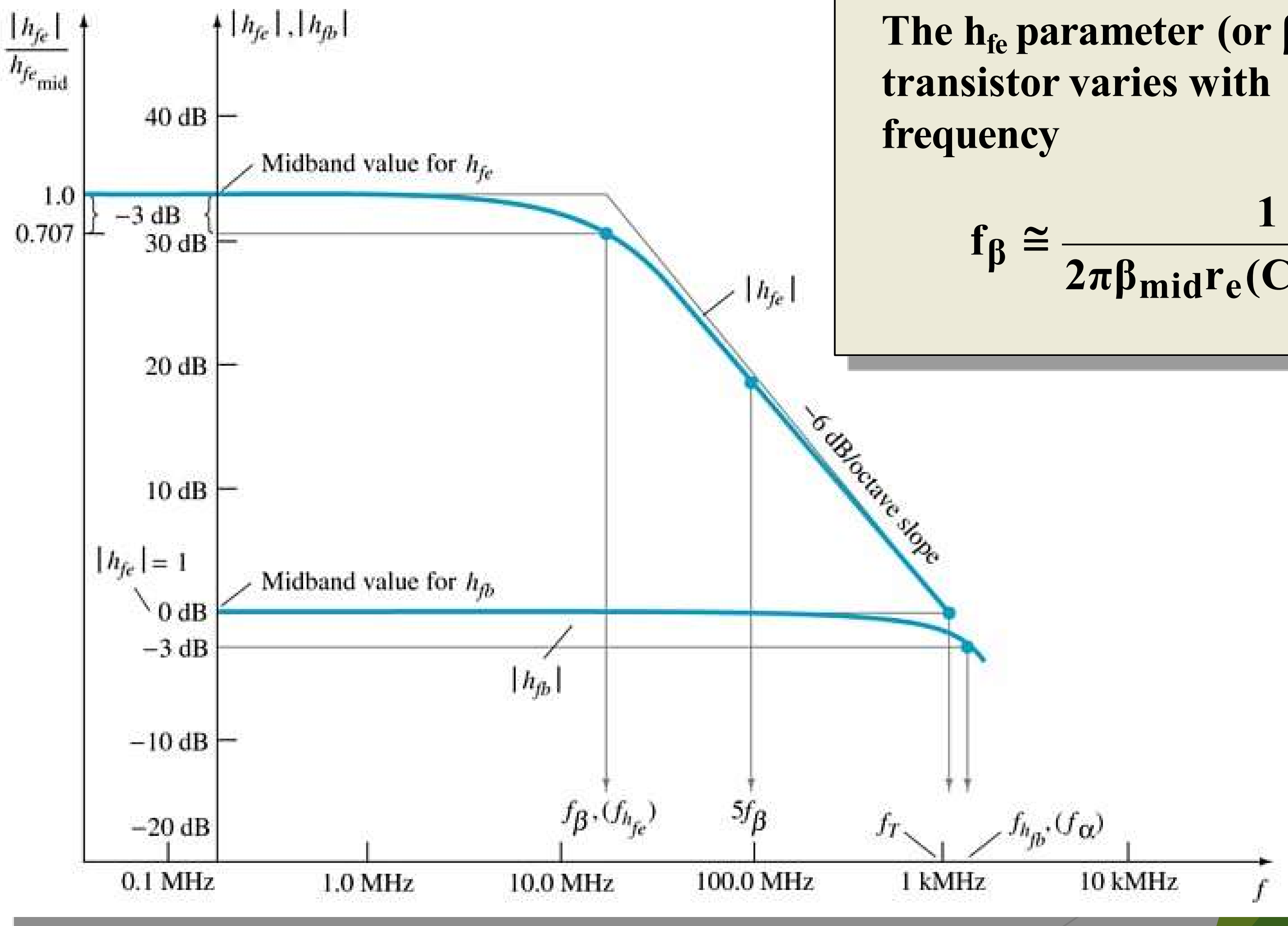
$$R_{Tho} = R_C \parallel R_L \parallel r_o$$

and

$$C_o = C_{Wo} + C_{ce} + C_{Mo}$$



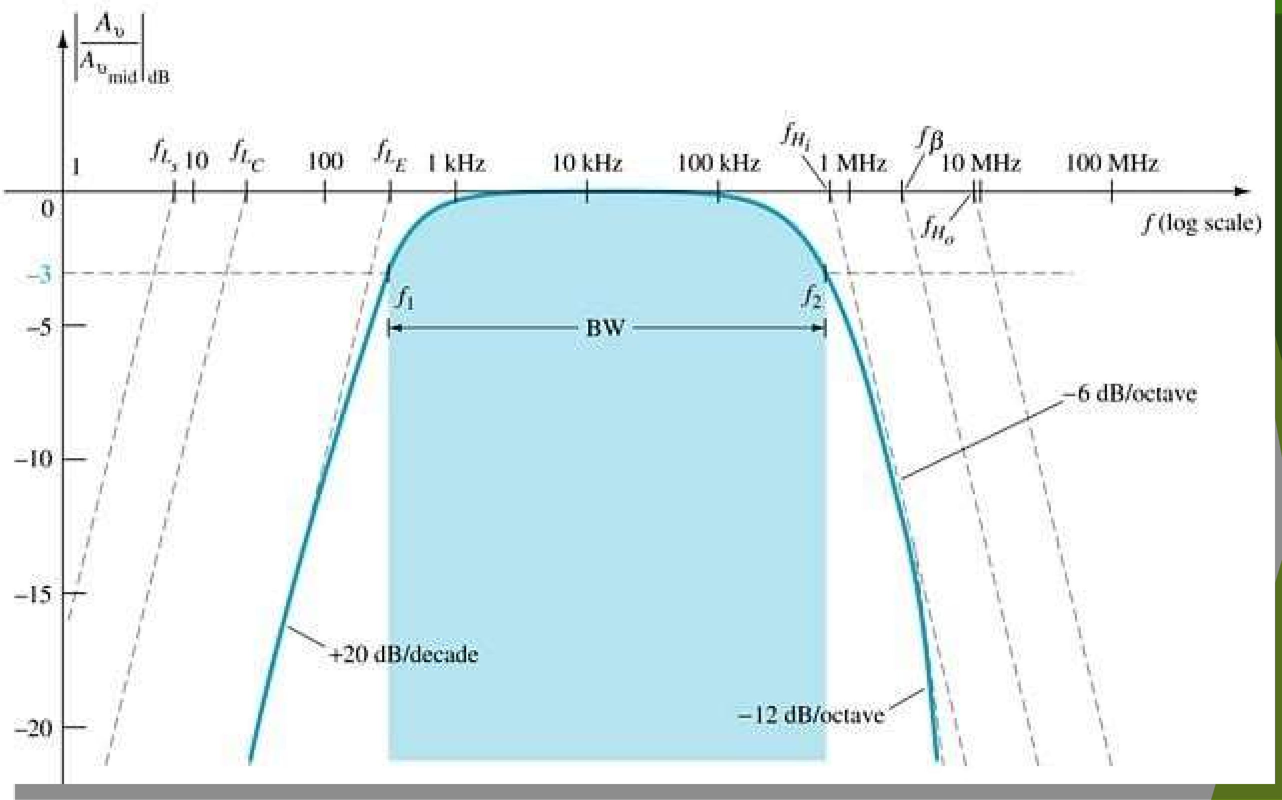
h_{fe} (or β) Variation



The h_{fe} parameter (or β) of a transistor varies with frequency

$$f_\beta \cong \frac{1}{2\pi\beta_{mid} r_e (C_{be} + C_{bc})}$$

BJT Amplifier Frequency Response

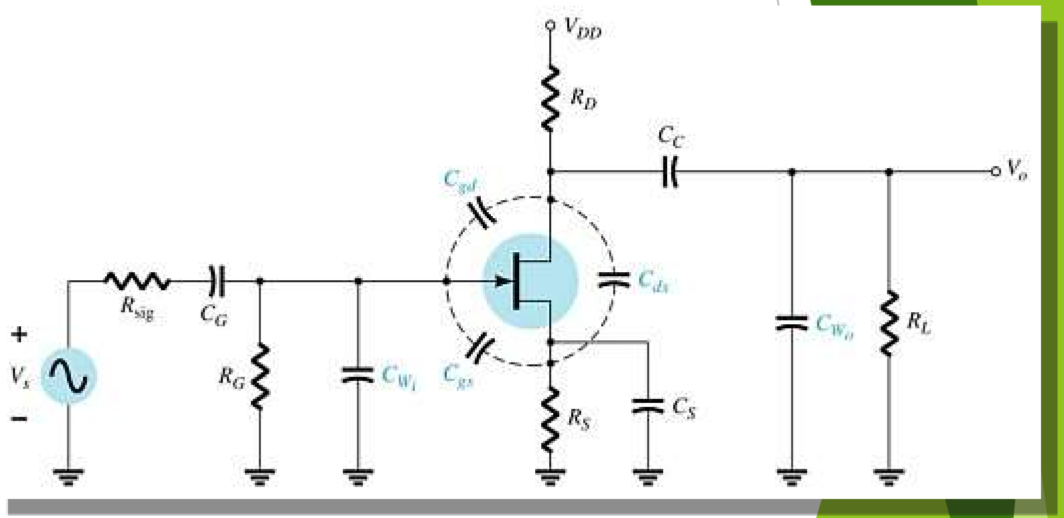


Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

FET Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- **Junction capacitances C_{gs}, C_{gd}, C_{ds}**
- **Wiring capacitances C_{wi}, C_{wo}**
- **Coupling capacitors C_G, C_C**
- **Bypass capacitor C_S**



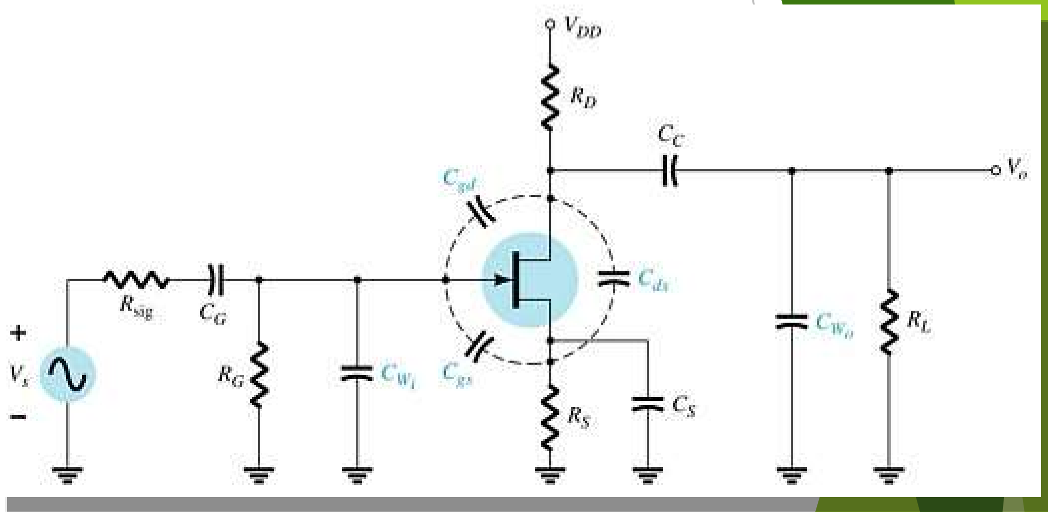
Input Network (f_{Hi}) High-Frequency Cutoff

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

$$C_i = C_{Wi} + C_{gs} + C_{Mi}$$

$$C_{Mi} = (1 - A_v)C_{gd}$$

$$R_{Thi} = R_{sig} \parallel R_G$$



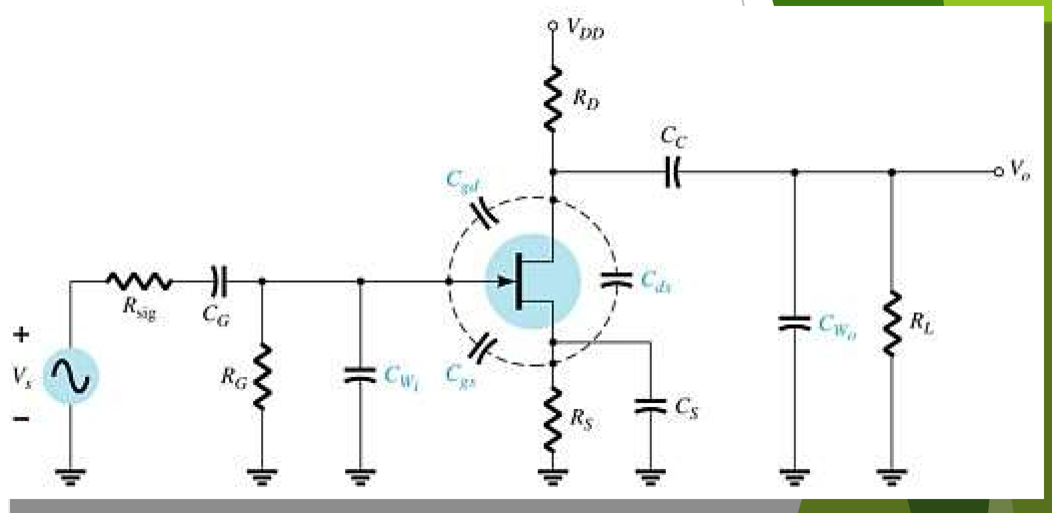
Output Network (f_{Ho}) High-Frequency Cutoff

$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

$$C_o = C_{Wo} + C_{ds} + C_{Mo}$$

$$C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$$

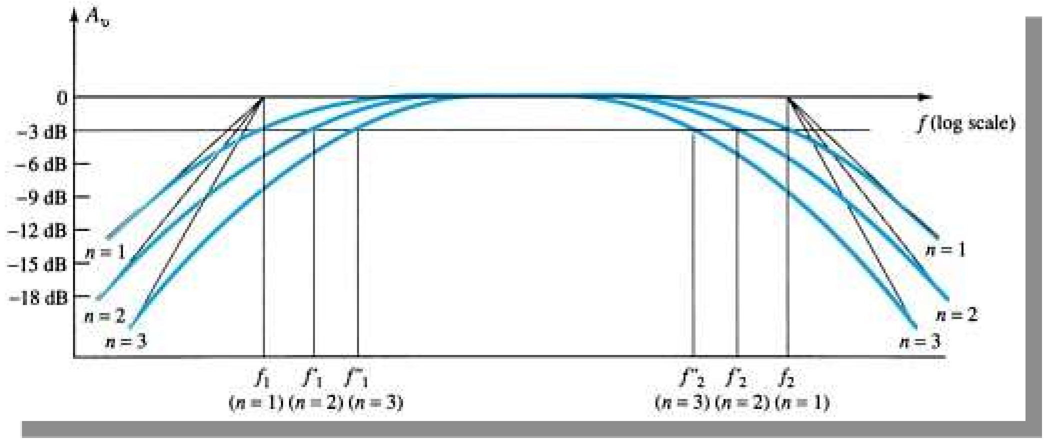
$$R_{Tho} = R_D \parallel R_L \parallel r_d$$



Multistage Frequency Effects

Each stage will have its own frequency response, but the output of one stage will be affected by capacitances in the subsequent stage. This is especially so when determining the high frequency response. For example, the output capacitance (C_o) will be affected by the input Miller Capacitance (C_{Mi}) of the next stage.

Multistage Amplifier Frequency Response



Once the cutoff frequencies have been determined for each stage (taking into account the shared capacitances), they can be plotted.

Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

Square wave Testing:

- Experimentally, the sense for the frequency response can be determined by applying a square wave signal to the amplifier and noting the output response.

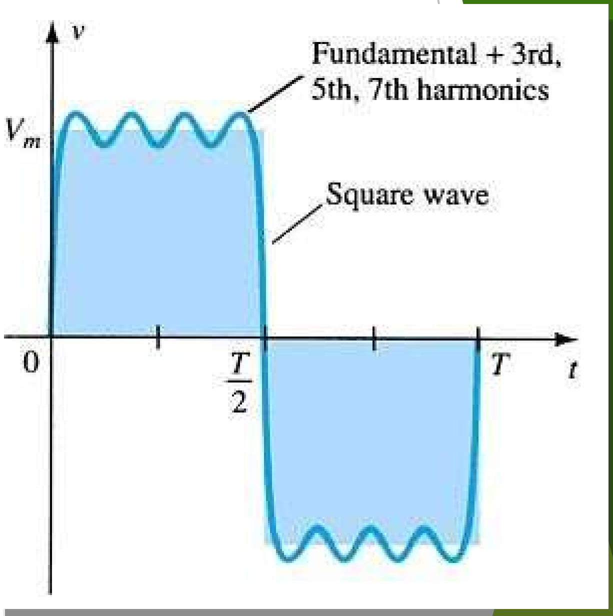
- The reason for choosing a square-wave signal for the testing process is best described by examining the Fourier series expansion of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies.

- The summation of the terms of the series will result in the original waveform. In other words, even though a waveform may not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies and magnitudes.

- Since the ninth harmonic has a magnitude greater than 10% of the fundamental term, the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function.

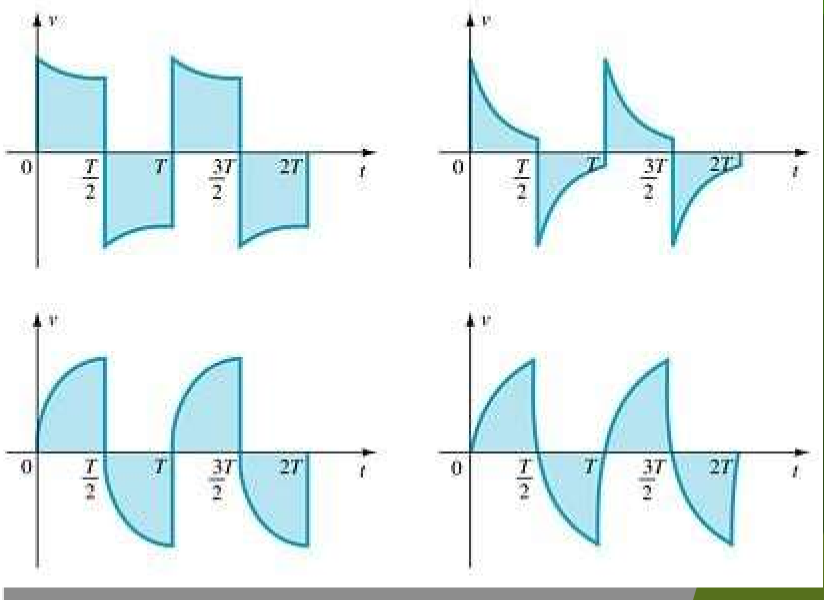
In order to determine the frequency response of an amplifier by experimentation, you must apply a wide range of frequencies to the amplifier.

One way to accomplish this is to apply a square wave. A square wave consists of multiple frequencies (by Fourier analysis: it consists of odd harmonics).



Square Wave Response Waveforms

If the output of the amplifier is not a perfect square wave then the amplifier is 'cutting' off certain frequency components of the square wave.



UNIT-III(a): Multivibrators

MULTIVIBRATOR

- **A MULTIVIBRATOR is an electronic circuit that generates square, rectangular, pulse waveforms, also called nonlinear oscillators or function generators.**
- **Multivibrator is basically a two amplifier circuits arranged with regenerative feedback.**

There are three types of Multivibrator:

- **Astable Multivibrator: Circuit is not stable in either state—it continuously**
- **Monostable Multivibrator: One of the state is stable but the other is not. (Application in Timer)**
- **Bistable Multivibrator: Circuit is stable in both the state and will remain in either state indefinitely. The circuit can be flipped from one state to the other by an external event or trigger. (Application in Flip flop)**

Multivibrators

A multivibrator is used to implement simple **two-state systems** such as oscillators, timers and flip-flops.

Three types:

–**Astable** – neither state is stable.

Applications: oscillator, etc.

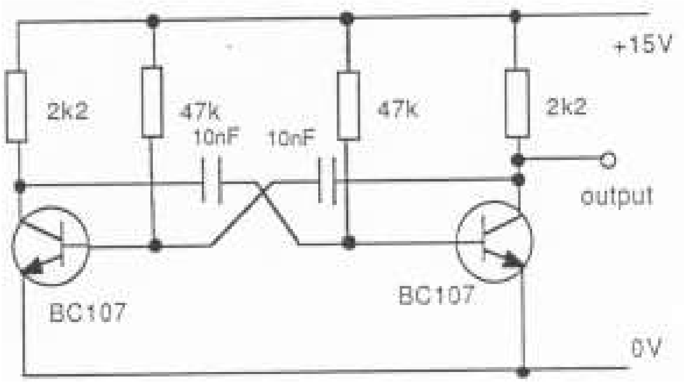
– **Monostable** - one of the states is stable, but the other is not;

Applications: timer, etc.

–**Bistable** – it remains in either state indefinitely.

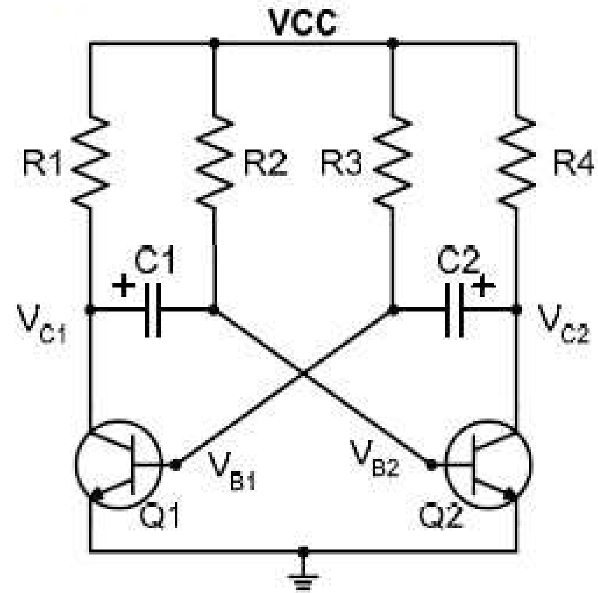
Applications: flip-flop, etc.

Astable Multivibrator



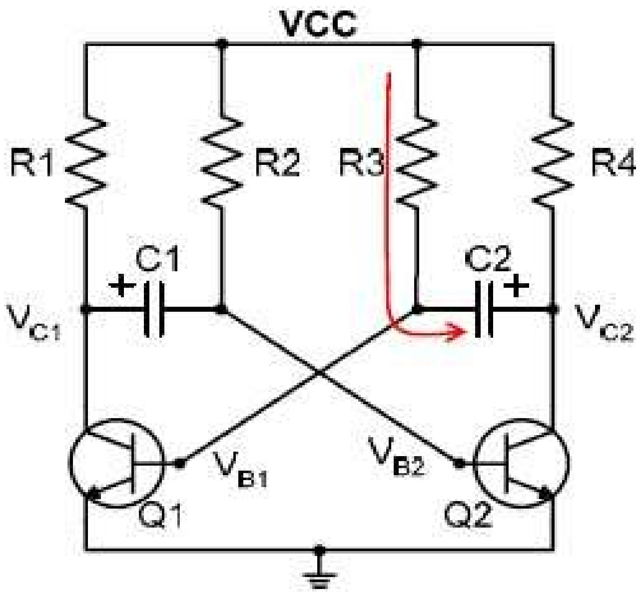
Circuit in Experiment A4

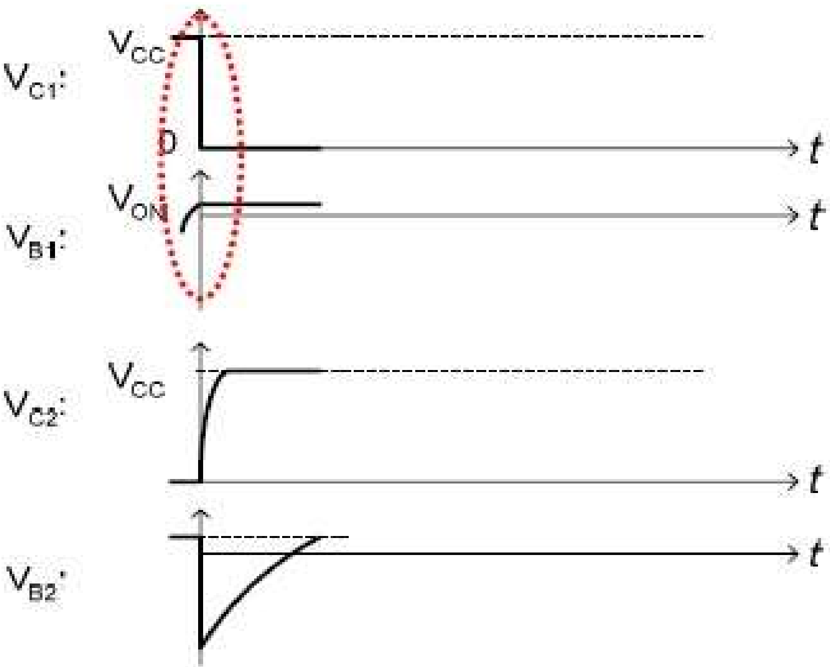
Redrawn



- Consists of two amplifying devices cross-coupled by resistors and capacitors.
- Typically, $R_2 = R_3$, $R_1 = R_4$, $C_1 = C_2$ and $R_2 >> R_1$.
- The circuit has two states
  - State 1: V_{C1} LOW, V_{C1} HIGH, Q_1 ON (saturation) and Q_2 OFF.
  - State 2: V_{C1} HIGH, V_{C2} LOW, Q_1 OFF and Q_2 ON (saturation).
- It continuously oscillates from one state to the other.

Basic Mode of Operation

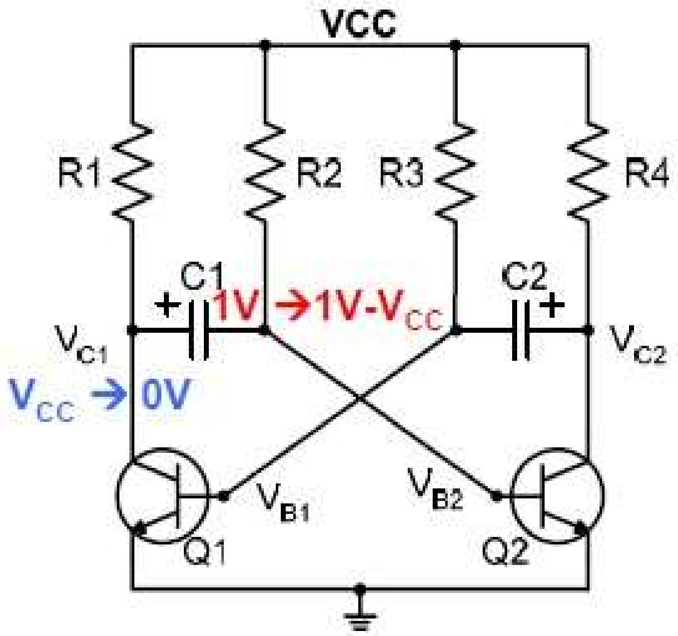


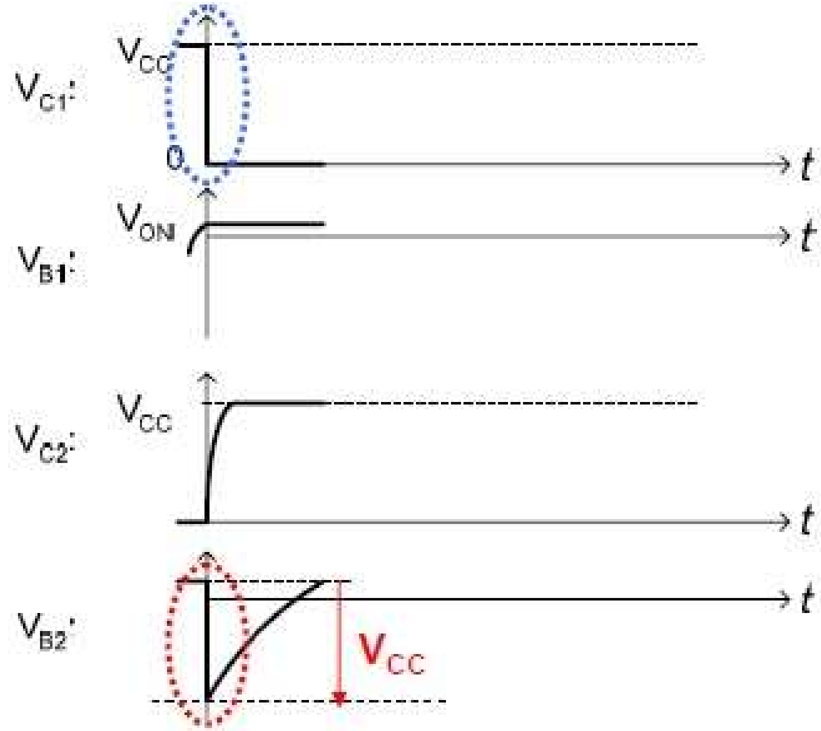


State 1:

- V_{B1} charges up through R_3 from below ground towards V_{CC}.
- When V_{B1} reaches V_{ON} (of $V_{BE,} \approx 1V$), Q_1 turns on and pulls V_{C1} from V_{CC} to $V_{CESat} \approx 0V$.
- Due to forward-bias of the BE junction of Q_1, V_{B1} remains at 1V.

Basic Mode of Operation

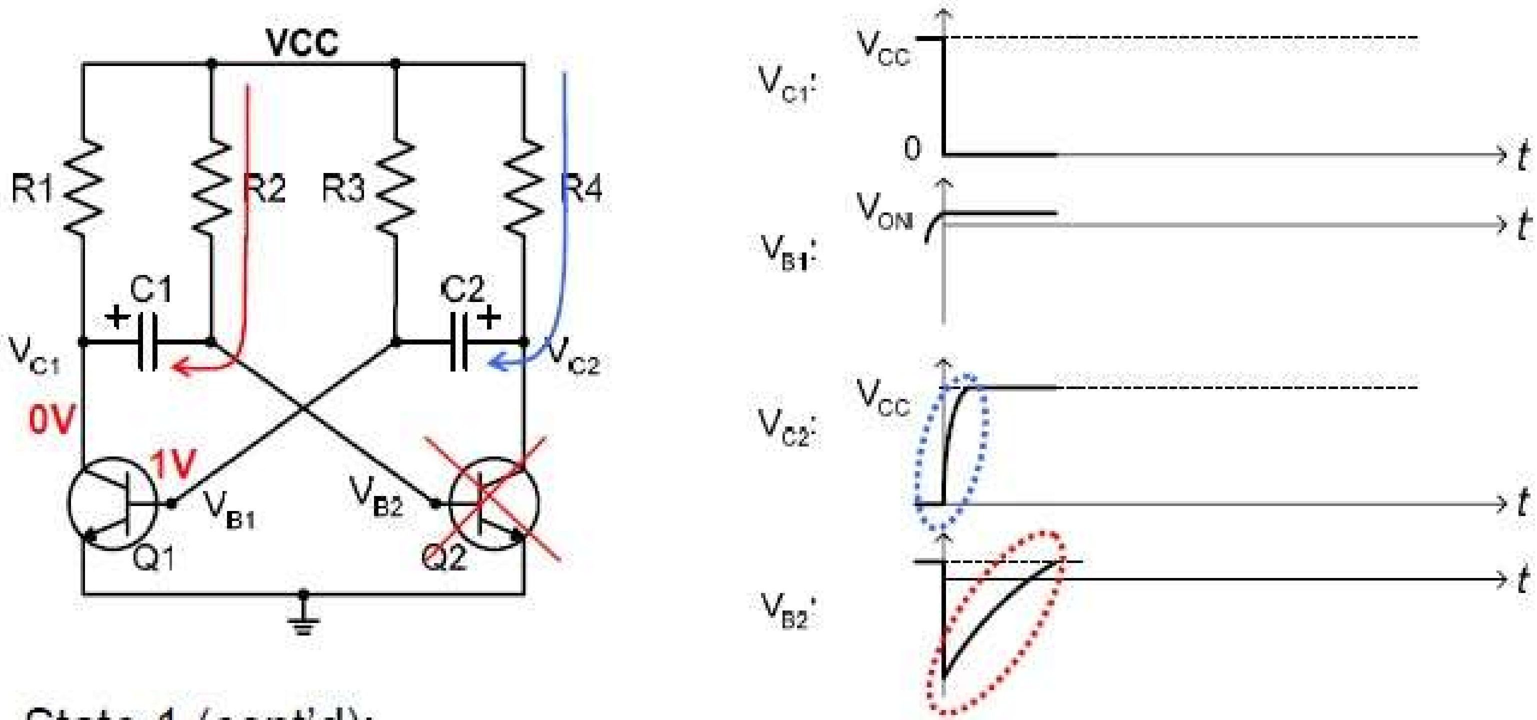




State 1 (cont'd):

- As C_1's voltage cannot change instantaneously, V_{B2} drops by V_{CC}.

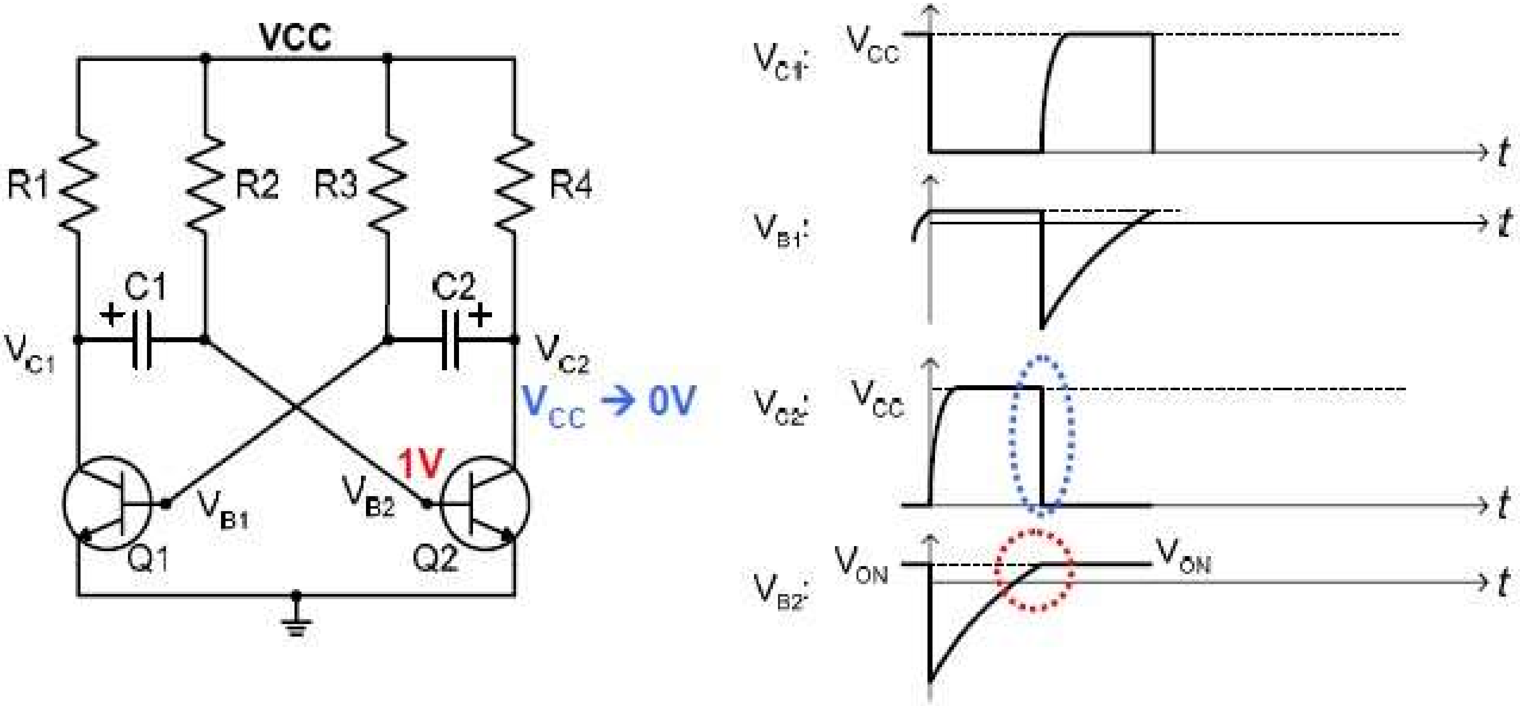
Basic Mode of Operation



State 1 (cont'd):

- Q_2 turns off and V_{C2} charges up through R_4 to V_{CC} (speed set by the time constant R_4C_2).
- V_{B2} charges up through R_2 towards V_{CC} (speed set by R_2C_1, which is slower than the charging up speed of V_{C2}).

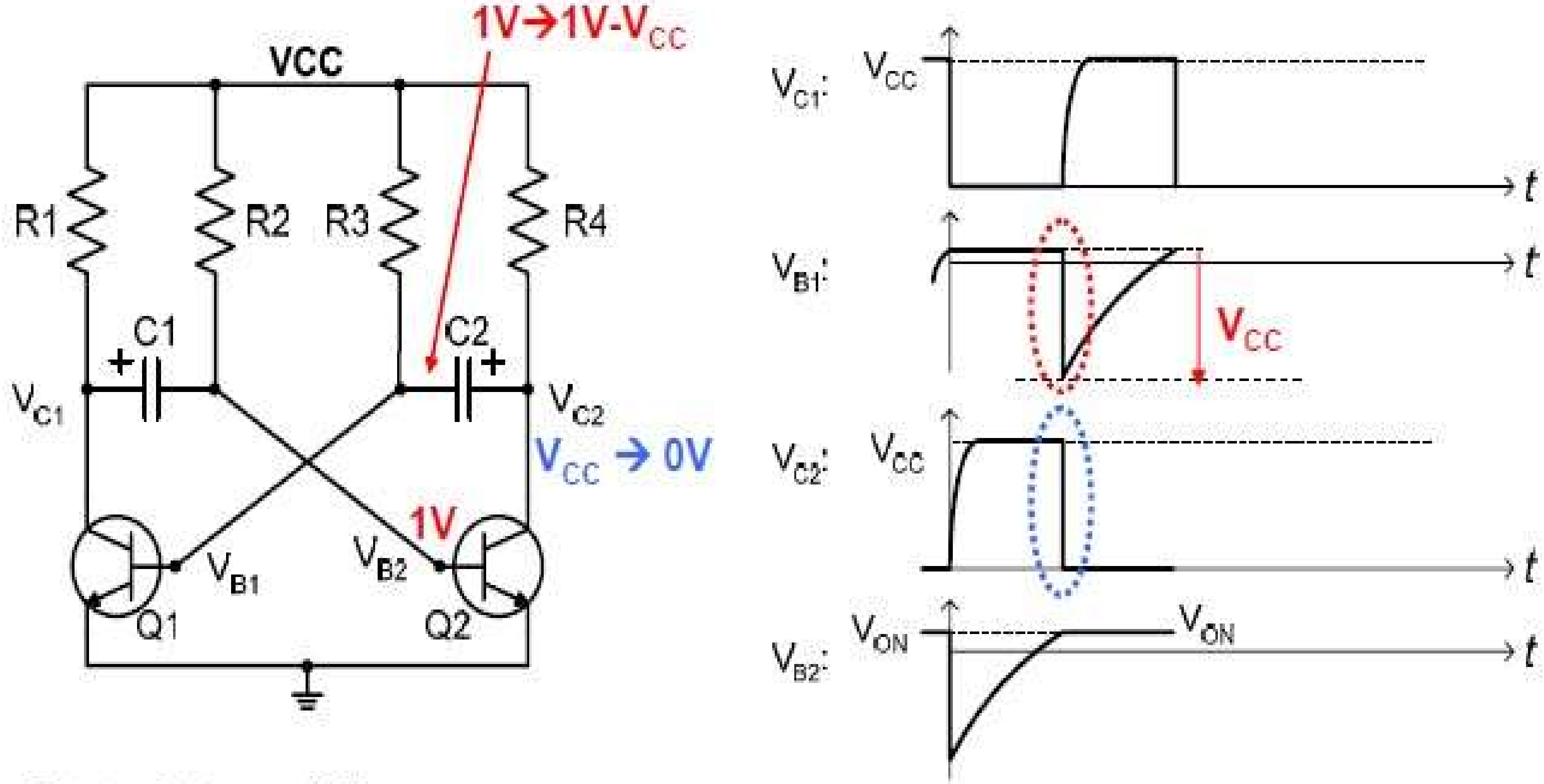
Basic Mode of Operation



State 2:

- When V_{B2} reaches V_{ON}, Q_2 turns on and pulls V_{C2} from V_{CC} to 0V.
- V_{B2} remains at V_{ON}.

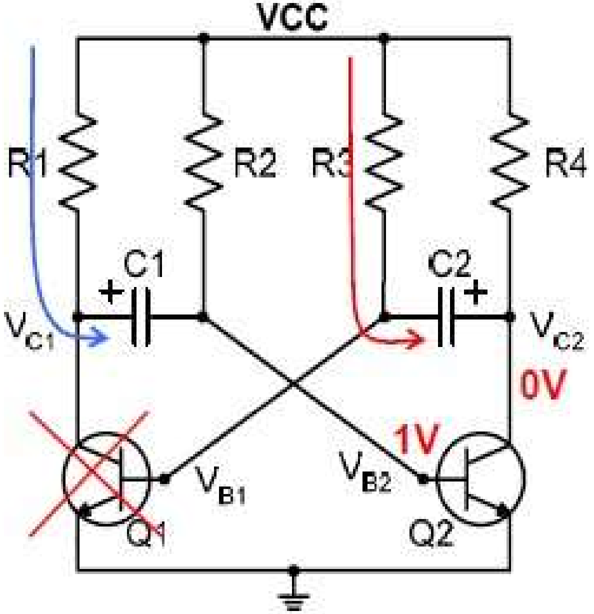
Basic Mode of Operation

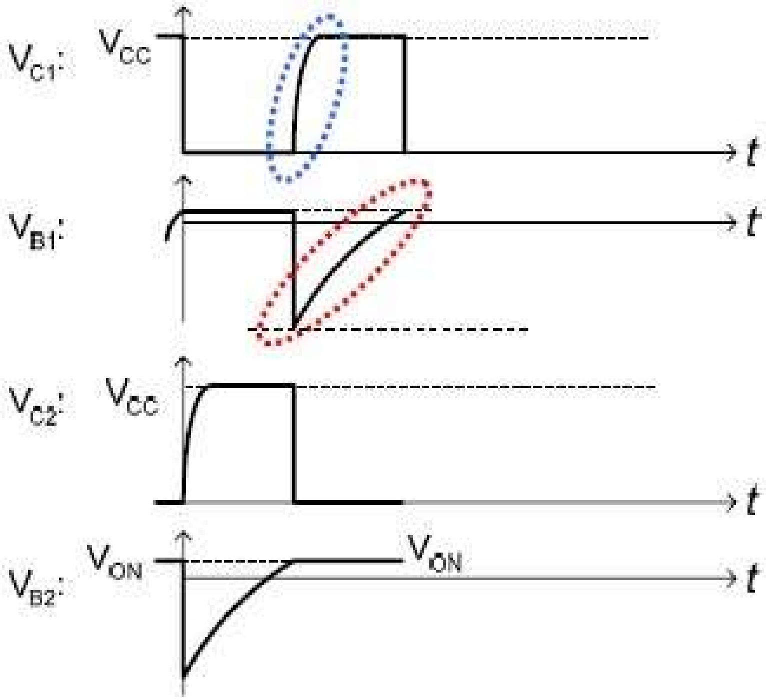


State 2 (cont'd):

- As C_2's voltage cannot change instantaneously, V_{B1} drops by V_{CC}.

Basic Mode of Operation

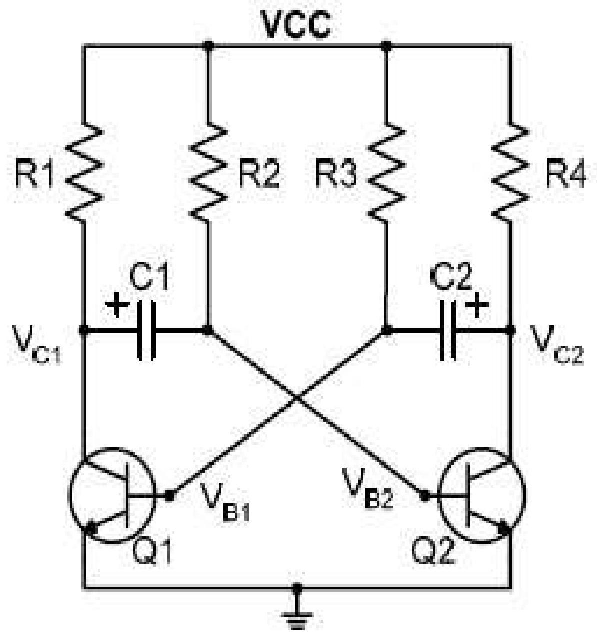


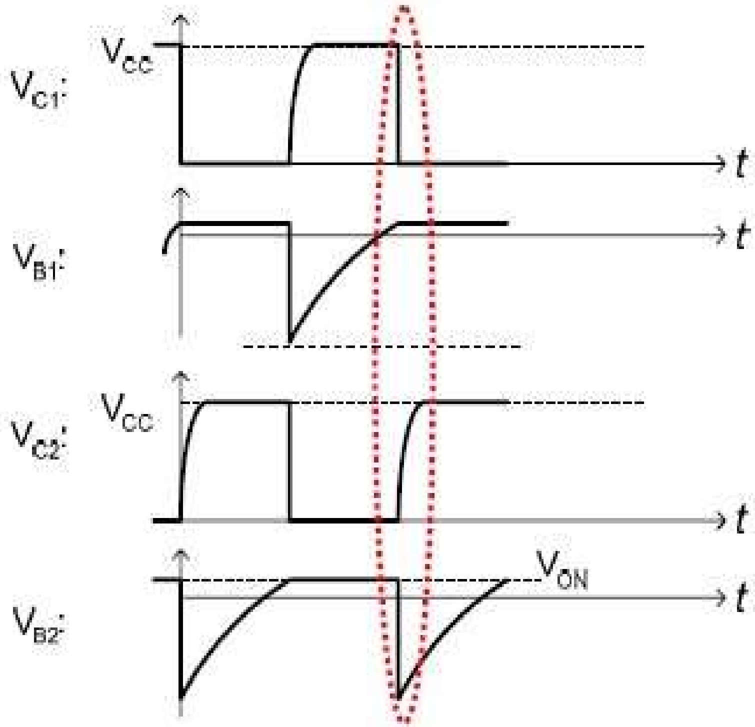


State 2 (cont'd):

- Q_1 turns off and V_{C1} charges up through R_1 to V_{CC}, at a rate set by R_1C_1.
- V_{B2} charges up through R_3 towards V_{CC}, at a rate set by R_3C_2, which is slower.

Basic Mode of Operation



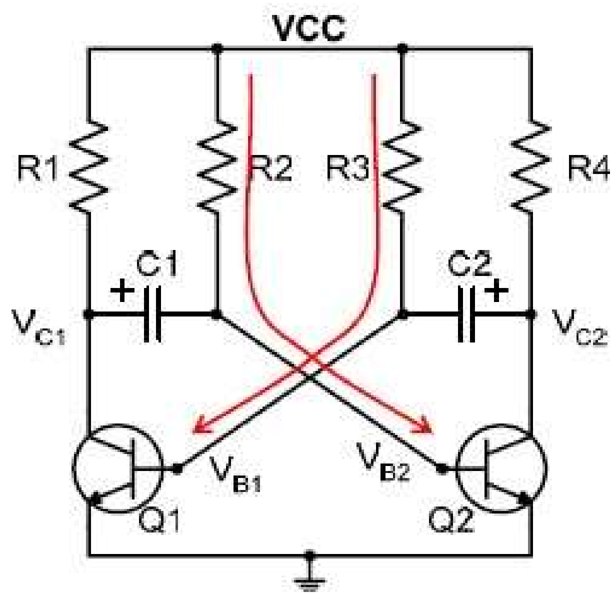


Back to state 1:

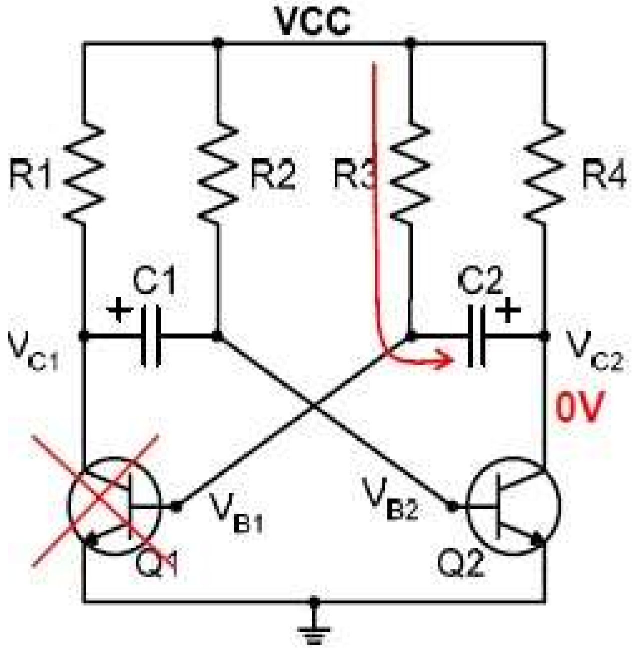
- When V_{B1} reaches Von, the circuit enters state 1 again, and the process repeats.

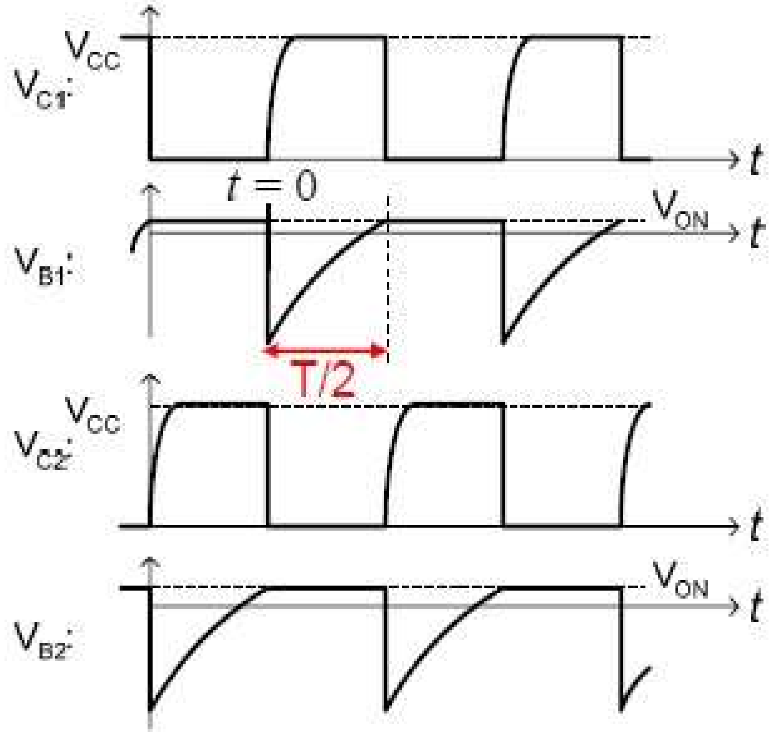
Initial Power-Up

- When the circuit is first powered up, neither transistor is ON.
- Parasitic capacitors between B and E of Q_1 and Q_2 are charged up towards V_{CC} through R_2 and R_3. Both V_{B1} and V_{B2} rise.
- Inevitable slight asymmetries will mean that one of the transistors is first to switch on. This will quickly put the circuit into one of the above states, and oscillation will ensue.



Multivibrator Frequency





$$v_{B1} = (V_{ON} - V_{CC}) + (2V_{CC} - V_{on})(1 - e^{-t/R_3C_2})$$

$$\approx -V_{CC} + 2V_{CC}(1 - e^{-t/R_3C_2}) \qquad \text{for } V_{ON} \ll V_{CC}$$

At t = T/2, $v_{B1}=V_{ON}$: $$V_{ON} = -V_{CC} + 2V_{CC}(1 - e^{-T/2R_3C_2})$$

Multivibrator Frequency

$$V_{ON} = -V_{CC} + 2V_{CC}(1 - e^{-T/2R_3C_2})$$

$$\therefore V_{CC} \approx 2V_{CC}(1 - e^{-T/2R_3C_2}) \quad \text{for } V_{ON} << V_{CC}$$

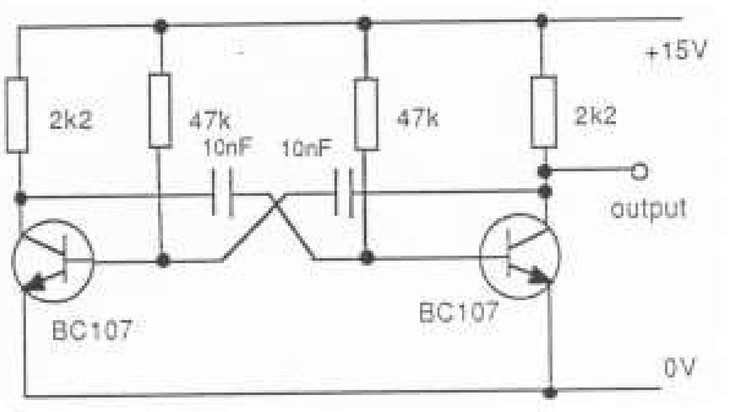
$$\therefore 1 = 2(1 - e^{-T/2R_3C_2})$$

$$\therefore e^{-T/2R_3C_2} = 0.5$$

$$\therefore -\frac{T}{2R_3C_2} = -\ln 2$$

$$\boxed{\therefore T = 2(\ln 2)R_3C_2}$$

or $$\boxed{f = \frac{1}{2(\ln 2)R_3C_2}}$$



For the above component values, f =1.53kHz.

Switching time & Frequency for Astable Multivibrators

- Time period of wave depends only upon the discharge of capacitors C_1 and C_2.
- Consider V_{B2} during discharge of C_2: $V_{B2} = V_{CC} - i_{C1}R_2$
- Since the capacitor C_1 charged up to V_{CC}, the initial discharge current will be

$$i_{C1} = \frac{V_{CC} + V_{CC}}{R_2}$$

Current decays exponentially with a time constant of R_2C_1

$$V_{B2} = V_{CC} - 2V_{CC}(e^{-t/R_2C_1})$$

Transistor will switch when V_{B2} = 0V (actually 0.7V for Si which is small compare to V_{CC})

$$\boxed{0 = V_{CC} - 2V_{CC}(e^{-t/R_2C_1})} \quad \boxed{2e^{-t/R_2C_1} = 1} \quad \boxed{t = T_2 = R_2C_1 \ln(2)}$$

where T2 is the off time for transistor Q_2

Switching time & Frequency for Astable Multivibrators

- Similarly off time for transistor Q_1 can be obtained.

$$\boxed{t = T_1 = R_3 C_2 \ln(2)}$$

- Total time period T:

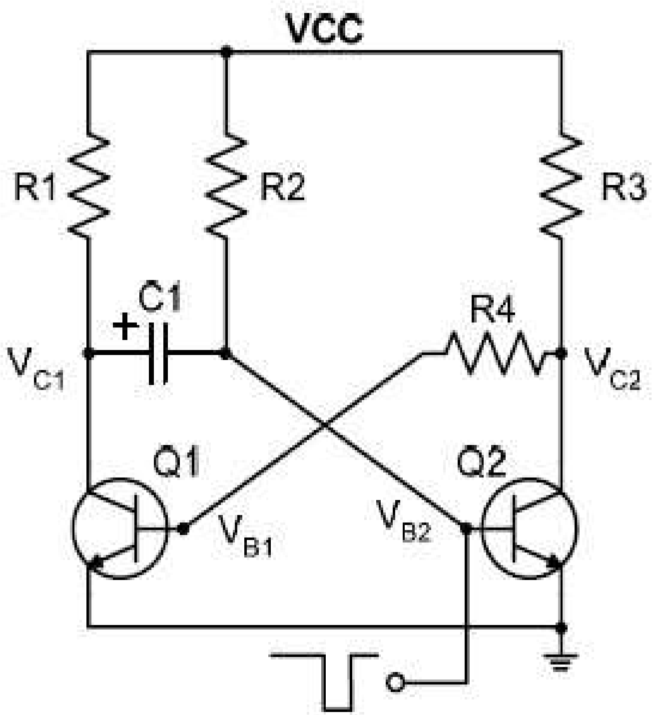
$$\boxed{T = T_1 + T_2 = [R_3 C_2 + R_2 C_1]\ln(2) = 0.694(R_3 C_2 + R_2 C_1)}$$

- If R2 = R3 = R, C1 = C2 = C then $\boxed{T = 1.4RC}$

- Frequency of oscillation is given by

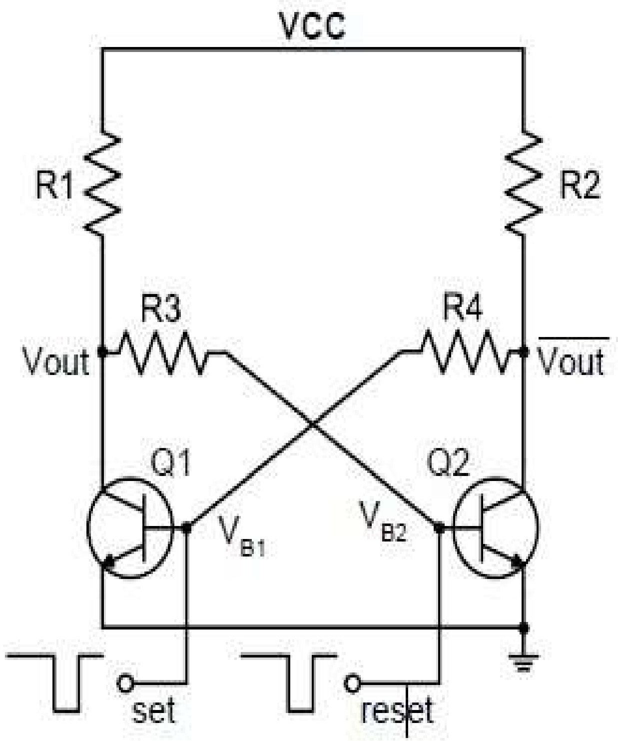
$$\boxed{f = \frac{1}{T} = \frac{0.7}{RC}}$$

Mono-stable Multivibrator



- Capacitive path between V_{C2} and V_{B1} removed.
- Stable for one state (state 2 here)
  - Q_1 OFF and Q_2 ON
  - V_{C1} High, V_{C2} Low
- When V_{B2} is momentarily pulled to ground by an external signal
  - V_{C2} rises to V_{CC}
  - Q_1 turns on
  - V_{C1} pulled down to 0V
  - Enter state 1 temporarily
- When the external signal goes high
  - V_{B2} charges up to V_{CC} through R_2
  - After a certain time T, V_{B2}=V_{ON}, Q_2 turns on
  - V_{C2} pulled to 0V, Q_1 turns off
  - Enters state 2 and remains there
- Can be used as a timer

Bi-stable Multivibrator



- Both capacitors removed
- Stable for either state 1 or 2
- Can be forced to either state by Set or Reset signals
- If Set is low,
  - Q_1 turns off
  - V_{C1} (V_{out}) and V_{B2} rises towards V_{CC}
  - Q_2 turns on
  - V_{C2} ($/V_{out}$) pulled to 0V
  - V_{B1} is latched to 0V
  - Circuit remains in state 2 until Reset is low
- If Reset is low
  - Similar operation
  - Circuit remains in state 1 until Set is low
- Behave as an RS flip-flop

UNIT-3(b)

CLIPPERS AND CLAMPERS

UNIT-3.B

CLIPPERS AND CLAMPERS

Non-Linear Wave Shaping

Definition: The process where by the form of a signal is changed by transmission through a non-linear network is called Non-linear Wave Shaping.

Types:

i. Clippers.

ii. Clampers.

Clippers and Clampers

- Diodes can be used in <u>wave shaping</u> circuits.
- Either:
  - Limit or "clip" signal portions.

    Clippers
  - Shift the dc voltage level of a signal.

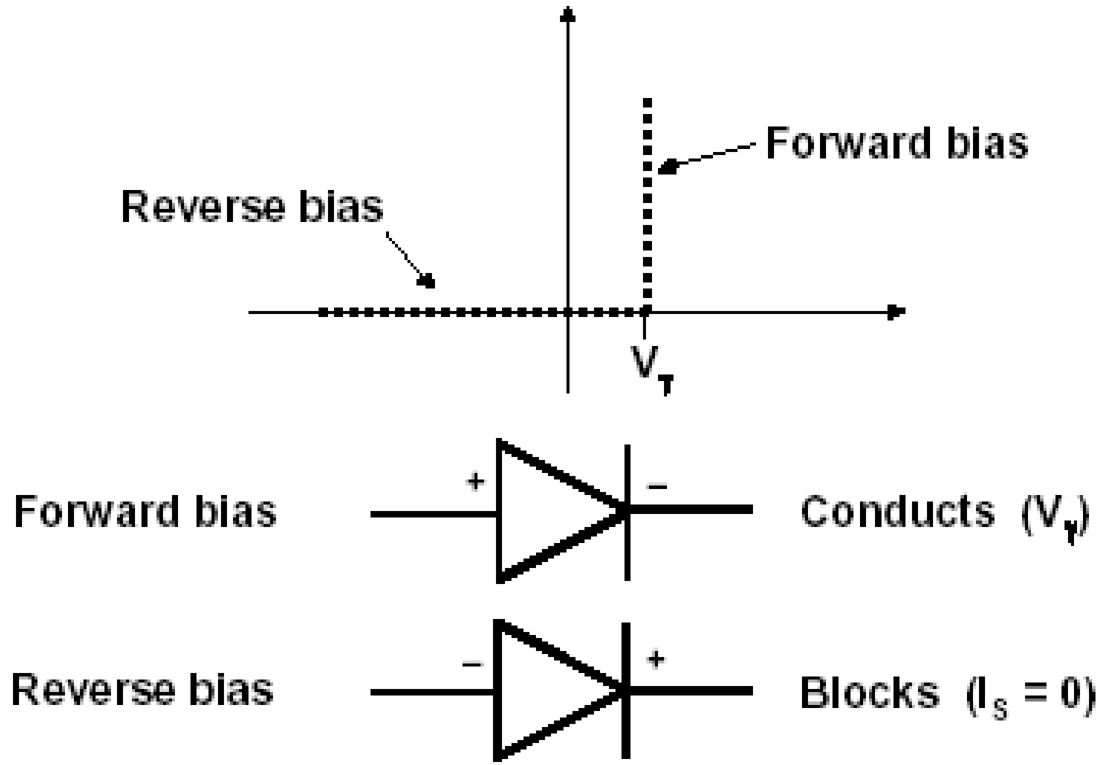
    Clampers

Clippers

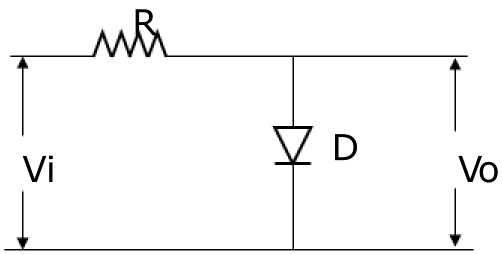
- Eliminate signal portions that are above or below a specified level.
- Application:

  Limit input voltage to an electronic circuit to prevent component damage.

Let's again consider piecewise linear diode model



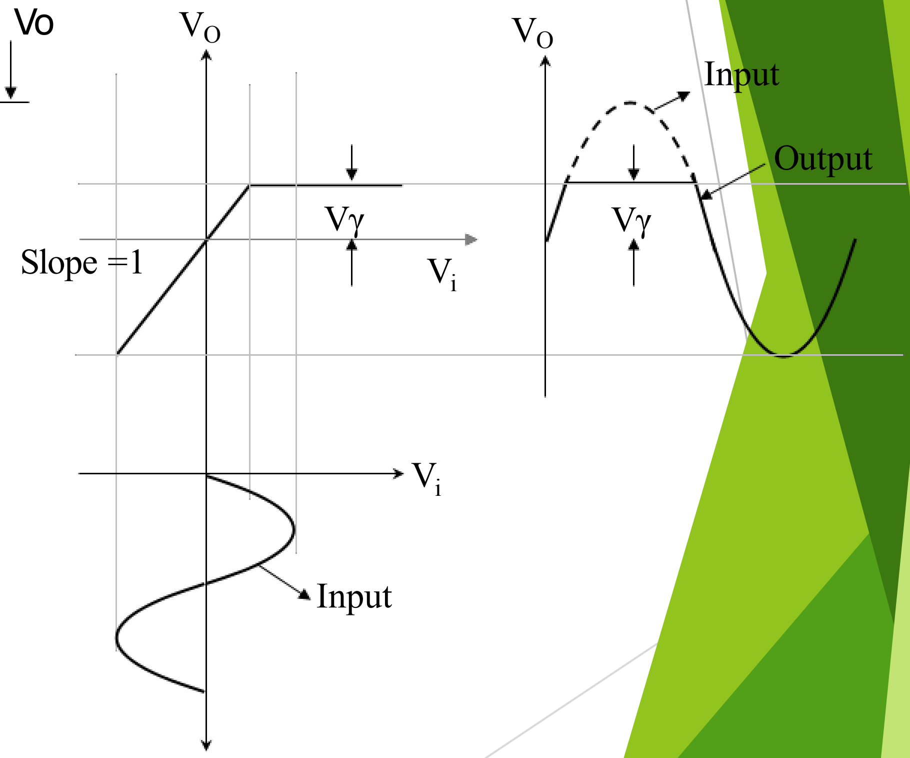
Positive Shunt clipping with zero reference voltage



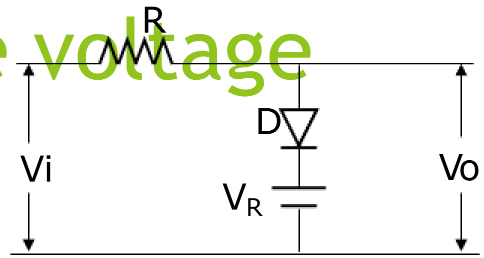
Transfer characteristics equations:

$V_O = 0$ for $V_i > 0$
$V_O = V_i$ for $V_i < 0$
[Ideal]

$V_O = V\gamma$ for $V_i > V\gamma$ D – ON
$V_O = V_i$ for $V_i < V\gamma$ D – OFF



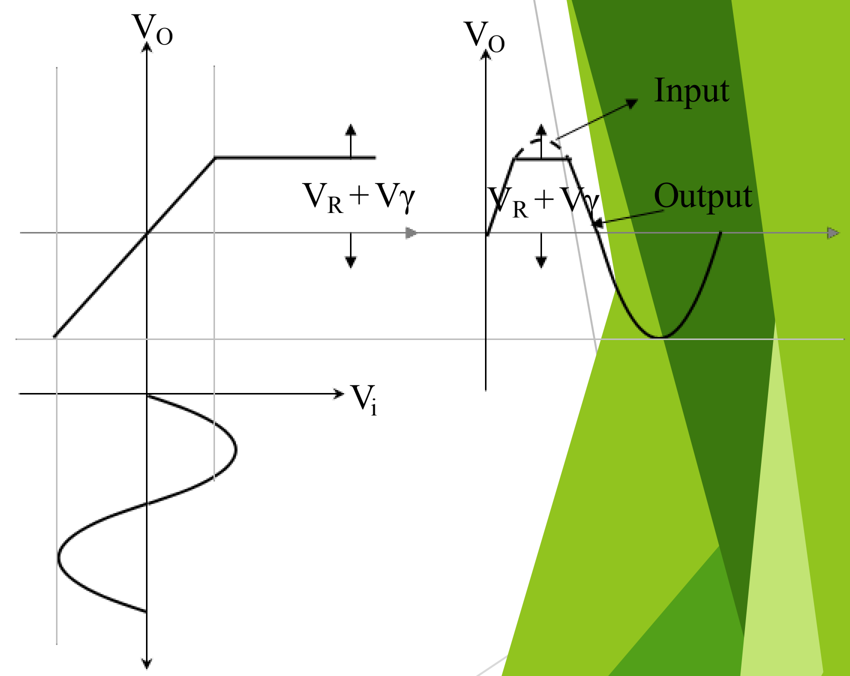
Positive Shunt clipping with positive reference voltage



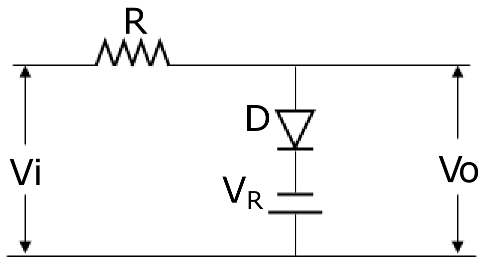
Transfer characteristics equations:

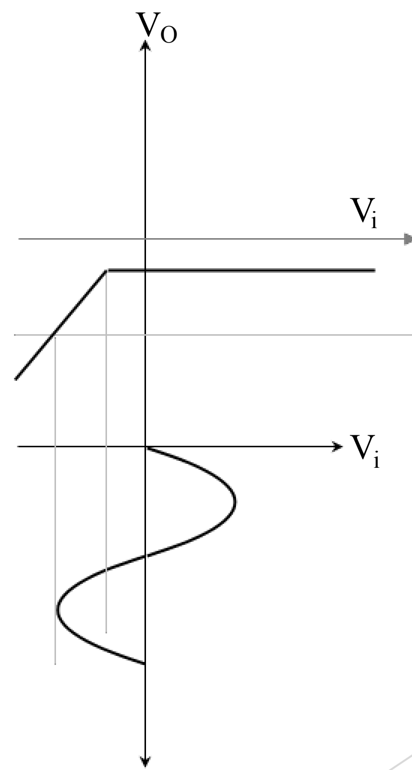
$V_i < V_R + V\gamma$ D – OFF $V_O = V_i$

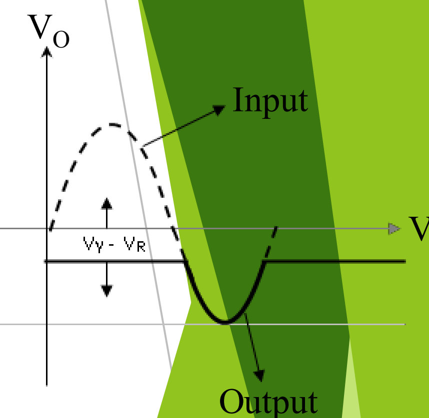
$V_i > V_R + V\gamma$ D – ON $V_O = V_R + V\gamma$



Positive Shunt clipping with negative refere voltage





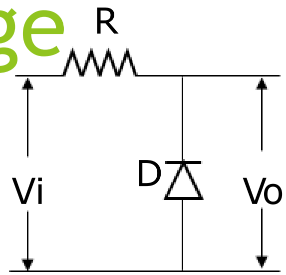


Transfer characteristics equation:

$V_i > V\gamma - V_R$ D – ON $V_O = V\gamma - V_R$

$V_i < V\gamma - V_R$ D – OFF $V_O = V_i$

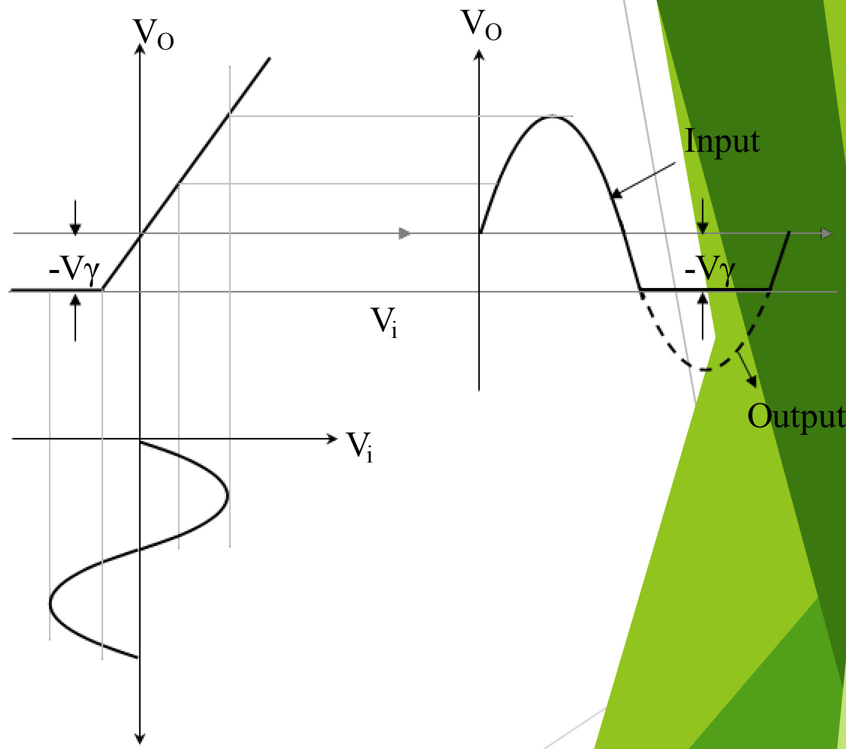
Negative Shunt clipping with zero referen voltage



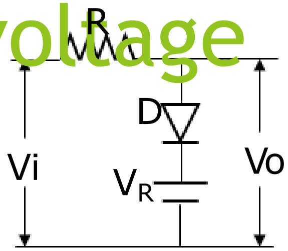
Transfer characteristic equations:

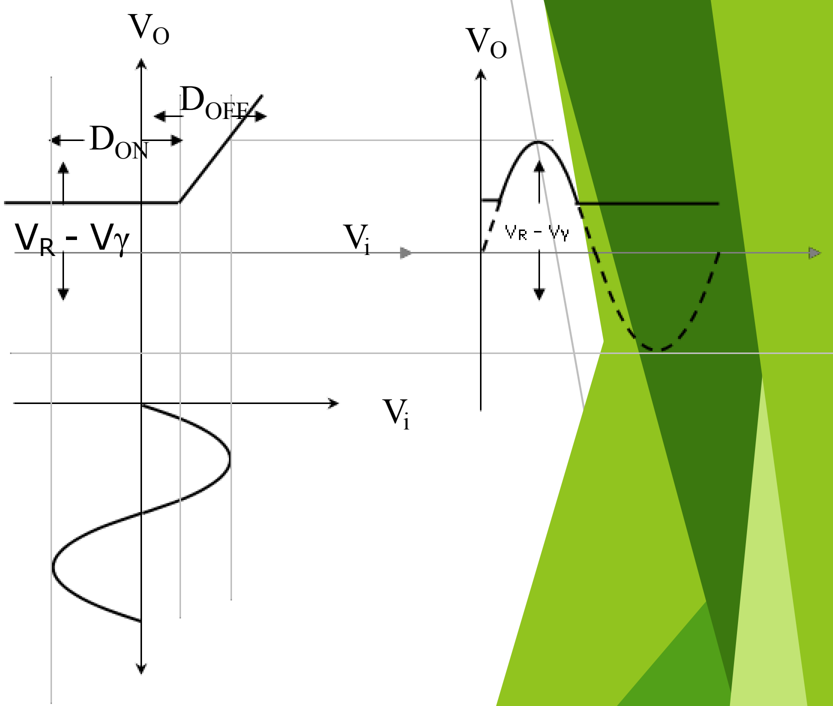
$V_i > -V\gamma$ D – OFF $V_O = V\gamma$

$V_i < -V\gamma$ D – ON $V_O = -V\gamma$



Negative Shunt clipping with positive reference voltage



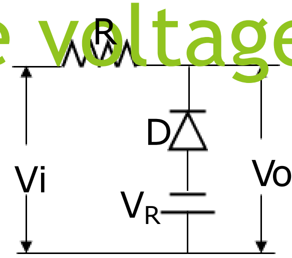


Transfer characteristics equations:

$V_i < V_R - V\gamma$ D – ON $\quad V_O = V_R - V\gamma$

$V_i > V_R - V\gamma$ D – OFF $\quad V_O = V_i$

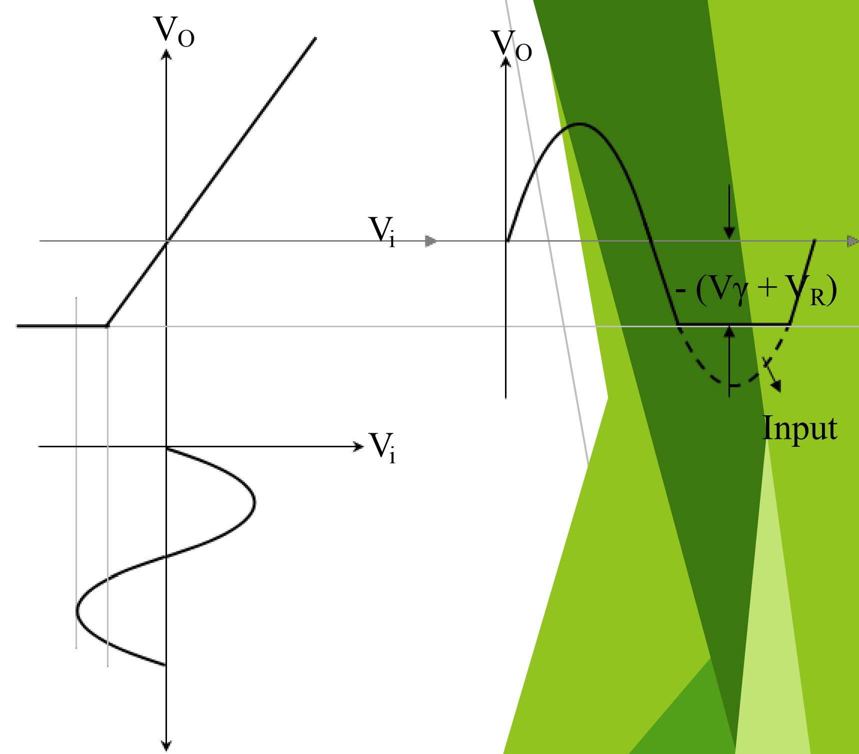
Negative Shunt clipping with negative reference voltage



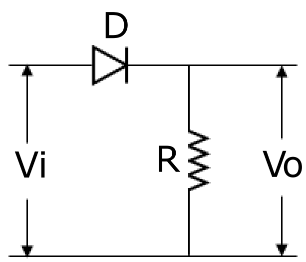
Transfer characteristic equations:

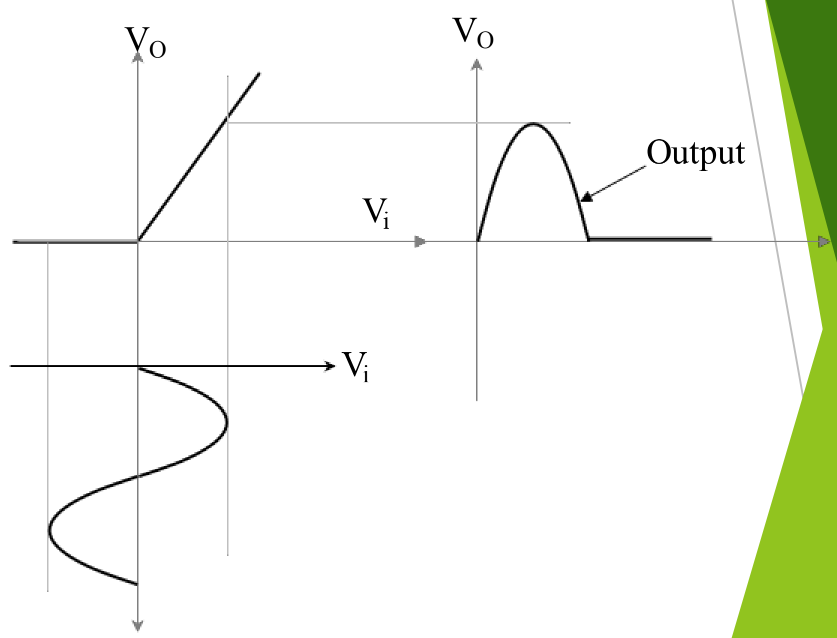
$V_i < -(V\gamma + V_R)$ D – ON $V_O = -(V\gamma + V_R)$

$V_i < -(V\gamma + V_R)$ D – OFF $V_O = V_i$



Negative Series clipper with zero reference

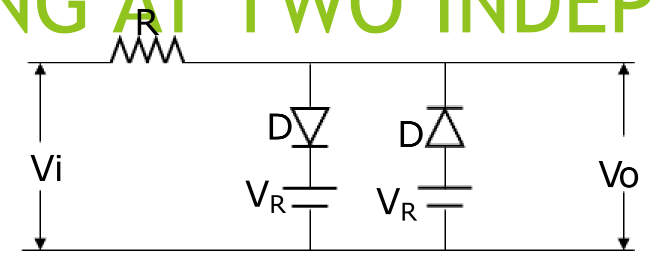




Transfer characteristic equations:

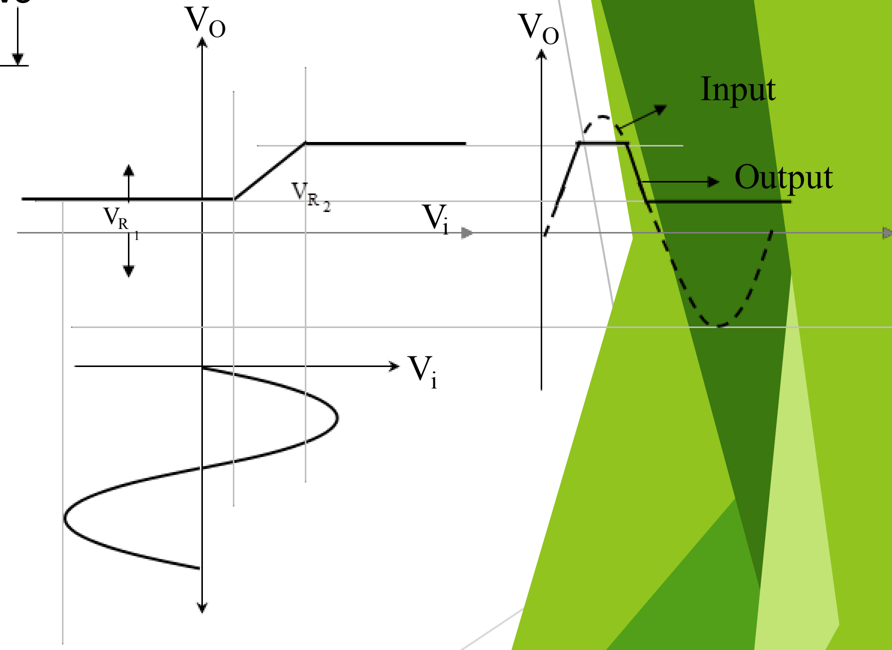
$V_i < 0$	D – OFF	$V_O = 0$	Ideal Diode
$V_i > 0$	D – ON	$V_O = V_i$	
$V_i < V_\gamma$	D – OFF	$V_O = 0$	Practical Diode
$V_i > V_\gamma$	D – ON	$V_O = V_i - V_\gamma$	

CLIPPING AT TWO INDEPENDENT LEVELS



Transfer characteristic equations:

Input (V_i)	Diode State	Output (V_o)
$V_i \leq V_{R_1}$	D_1 – ON, D_2 – OFF	$V_o = V_{R_1}$
$V_{R_1} < V_i < V_{R_2}$	D_1 – OFF, D_2 – OFF	$V_o = V_i$
$V_i \geq V_{R_2}$	D_1 – OFF, D_2 – ON	$V_o = V_{R_2}$



CLAMPING CIRCUIT

- The need to establish the extremity of the positive (or) negative signal excursion at some reference level. When the signal is passed through a capacitive coupling network such a signal has lost its d.c. component. The clamping circuit introduces the d.c. components at the outside, for this reason the coupling circuits are referred to as d.c. restore (or) d.c. reinserter.

- Def : "A clamping circuit is one that takes an input waveform and provides an output i.e., a faithful replica of its shape, but has one edge clamped to the zero voltage reference point.

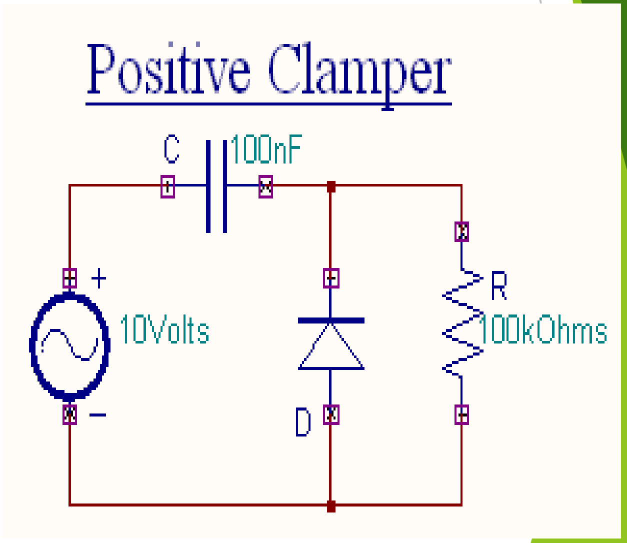
There are two types of clamping circuits.

- 1) Negative clamping circuit.
- 2) Positive clamping circuit.

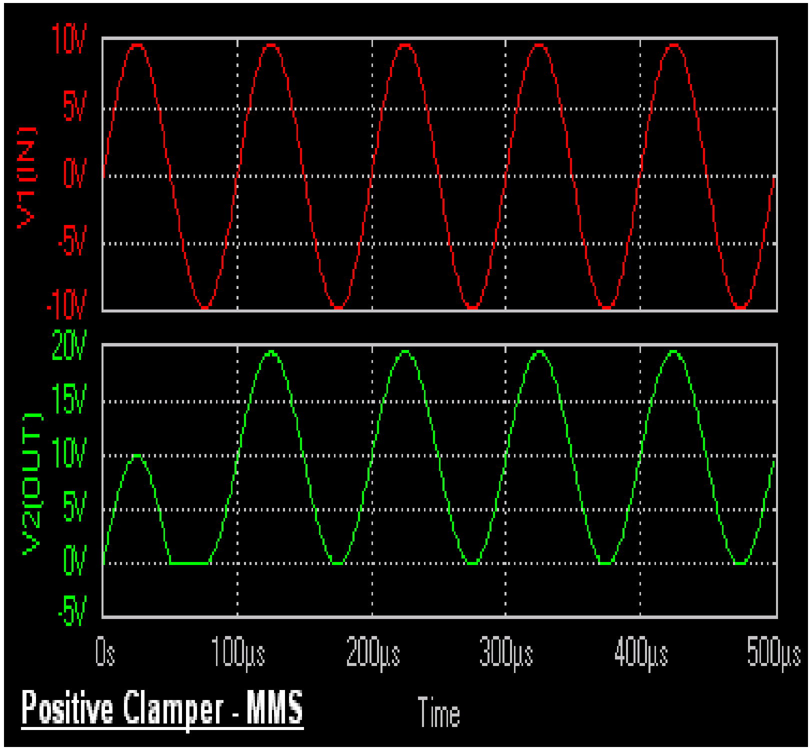
Diode :- Clamper

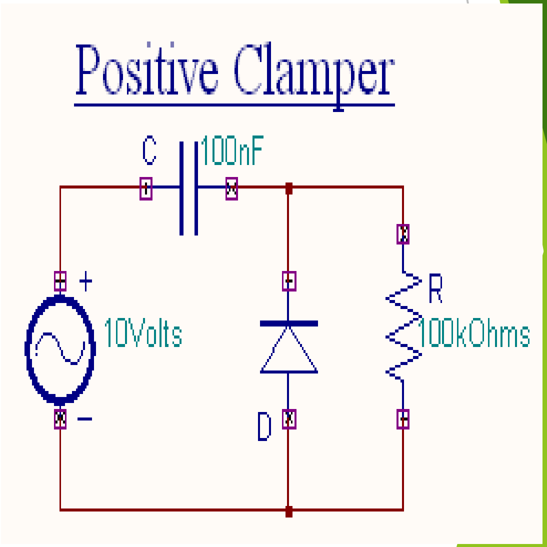
Positive Clamper

The circuit for a positive clamper is shown in the figure. During the negative half cycle of the input signal, the diode conducts and acts like a short circuit. The output voltage $V_o \Rightarrow 0$ volts . The capacitor is charged to the peak value of input voltage V_m. and it behaves like a battery. During the positive half of the input signal, the diode does not conduct and acts as an open circuit. Hence the output voltage $V_o \Rightarrow V_m + V_m$ This gives a positively clamped voltage.



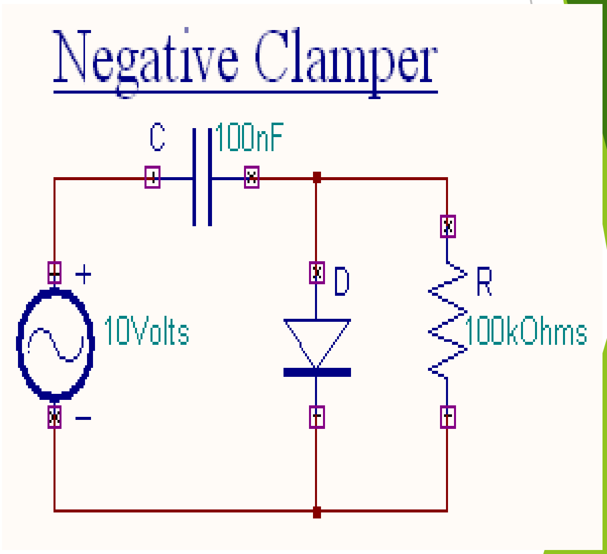
$V_o \Rightarrow V_m + V_m = 2\ V_m$


10V
5V
0V
-5V
-10V
V1(IN)
20V
15V
10V
5V
0V
-5V
V2(OUT)
0s
100μs
200μs
300μs
400μs
500μs
Positive Clamper - MMS
Time

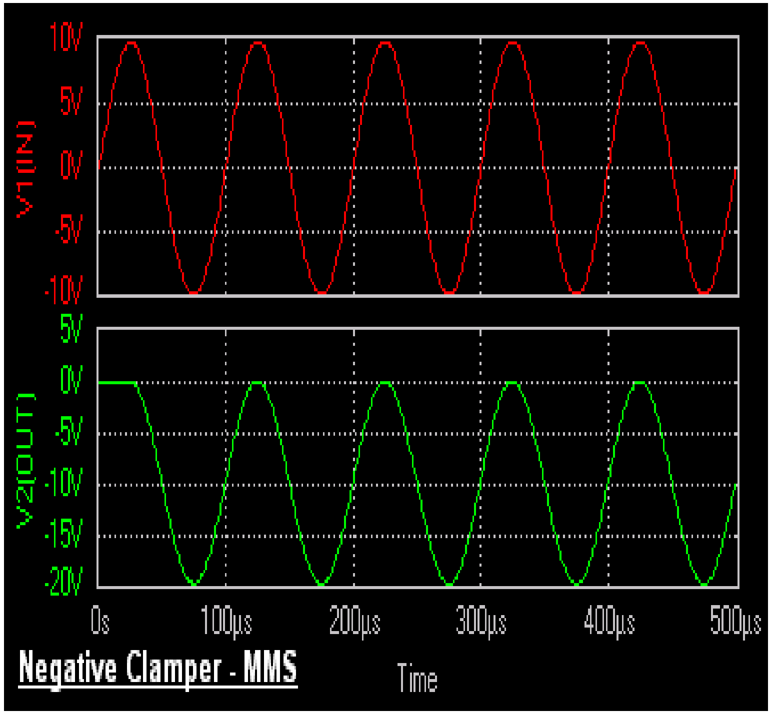

Positive Clamper
C
100nF
+
10Volts
−
D
R
100kOhms

Negative Clamper

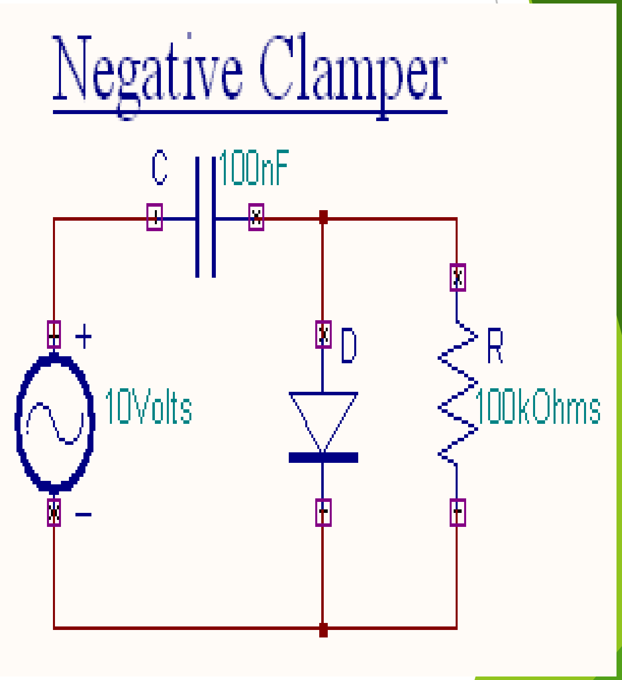
During the positive half cycle the diode conducts and acts like a short circuit. The capacitor charges to peak value of input voltage V_m. During this interval the output Vo which is taken across the short circuit will be zero During the negative half cycle, the diode is open. The output voltage can be found by applying KVL.



$$-V_m - V_m - V_o = 0 \qquad V_o = -2V_m$$

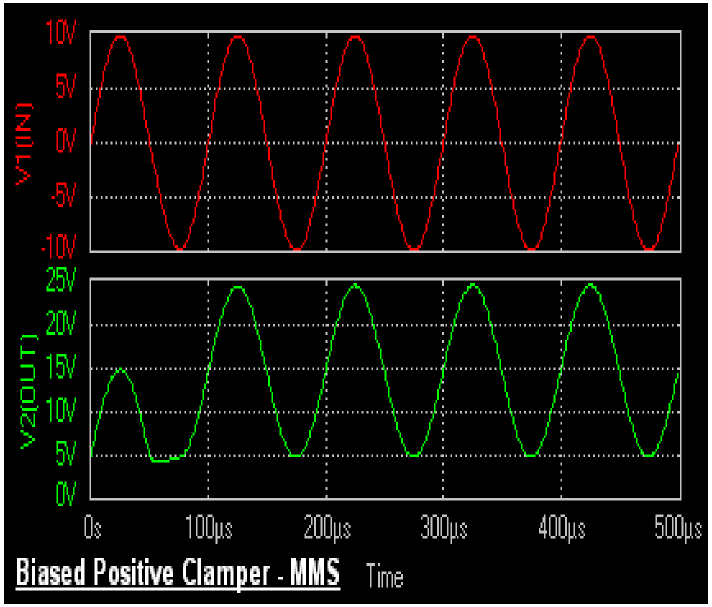


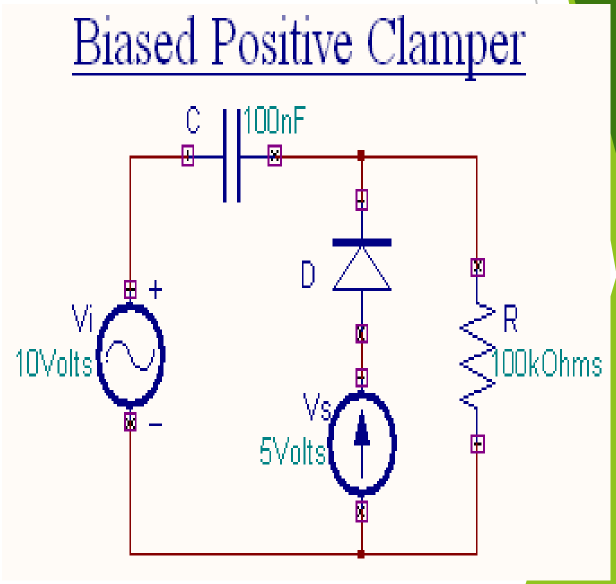
10V
5V
0V
-5V
-10V
V1(IN)
5V
0V
-5V
-10V
-15V
-20V
V2(OUT)
0s
100µs
200µs
300µs
400µs
500µs
Negative Clamper - MMS
Time



Negative Clamper
C
100nF
+
10Volts
−
D
R
100kOhms

Biased Clamper





CLAMPING CIRCUIT THEOREM

- Therefore the charge acquired by the capacitor during the forward interval

$$\therefore \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$

Consider a square wave input is applied to a clamping circuit under steady state condition

If V_f (t) is the output waveform in the forward direction, then from below figure the capacitor charging current is

$$i_f = \frac{V_f}{R_f}$$

Therefore the charge acquired by the capacitor during the forward interval

$$\int_0^{T_1} i_f \, dt = \frac{1}{R_f} \int_0^{T_1} V_f \, dt = \frac{A_f}{R_f} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

- Similarly if V_f (t) is the output voltage in the reverse direction, then the current which discharges by the capacitor is

$$i_r = \frac{V_r}{R}$$

$$\int_{T_1}^{T_2} i_r \, dt = \frac{1}{R}\int_{T_2}^{T_2} V_r \, dt = \frac{A_r}{R} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

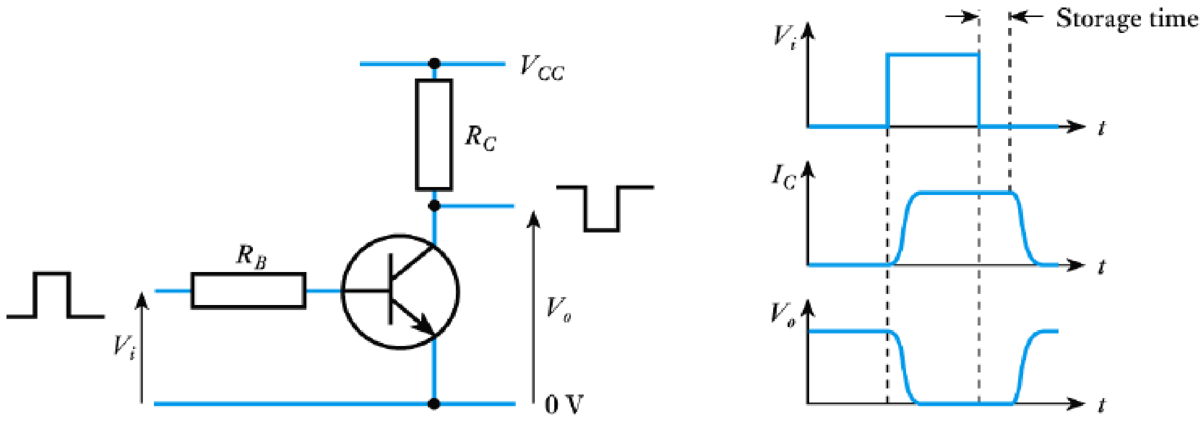
In the steady-state the net charge acquired by the capacitor must be zero.

Therefore from equation (1) & (2) $\frac{A_f}{R_f} = \frac{A_r}{R}$ this equation says that for any input waveform the ratio of the area under the output voltage curve in the forward direction to the reverse direction is equal to the ratio .

$$\frac{R_f}{R}$$

- **Transistors as switches**
  - both FETs and bipolar transistors make good switches
  - neither form produce *ideal* switches and their characteristics are slightly different
  - both forms of device take a finite time to switch and this produces a slight delay in the operation of the gate
  - this is termed the **propagation delay** of the circuit

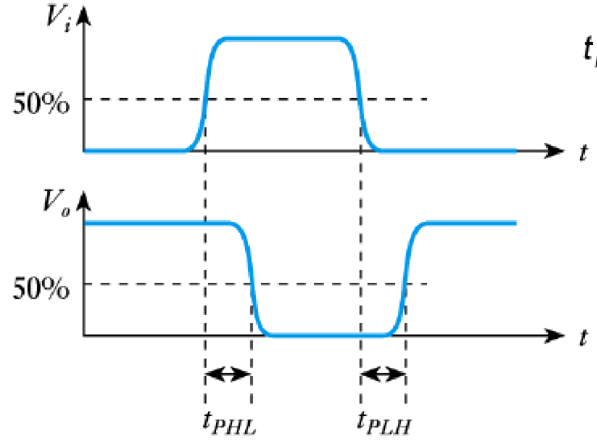
- The bipolar transistor as a logical switch



(a) Circuit (b) Waveforms

- when the input voltage to a bipolar transistor is high the transistor turns ON and the output voltage is driven down to its **saturation voltage** which is about 0.1 V
- however, saturation of the transistor results in the storage of excess charge in the base region
- this increases the time taken to turn OFF the device – an effect known as **storage time**
- this makes the device faster to turn ON than OFF
- some switching circuits increase speed by preventing the transistors from entering saturation

- **Timing considerations**
  - all gates have a certain **propagation delay time**, t_{PD}
  - this is the average of the two switching times



$$t_{PD} = \frac{1}{2}(t_{PHL} + t_{PLH})$$

Unit-4(a)

Large Signal Amplifiers

Power Amplifier (Class A)

- Induction of Power Amplifier
- Power and Efficiency
- Amplifier Classification
- Basic Class A Amplifier
- Transformer Coupled Class A Amplifier
- Push pull amplifier
- Complementary Symmetry circuits
- Phase inverters

- Power amplifiers are used to deliver a relatively **high amount of power**, usually **to** a **low resistance load.**
- Typical load values range from 300W (for transmission antennas) to 8W (for audio speaker).
- Although these load values do not cover every possibility, they do illustrate the fact that power amplifiers **usually drive low-resistance loads**.
- Typical output power rating of a power amplifier will be **1W or higher**.
- **Ideal** power amplifier will deliver **100%** of the power it draws from the supply to load. In **practice**, this can never occur.
- The reason for this is the fact that the components in the amplifier will all **dissipate** some of the power that is being drawn form the supply.

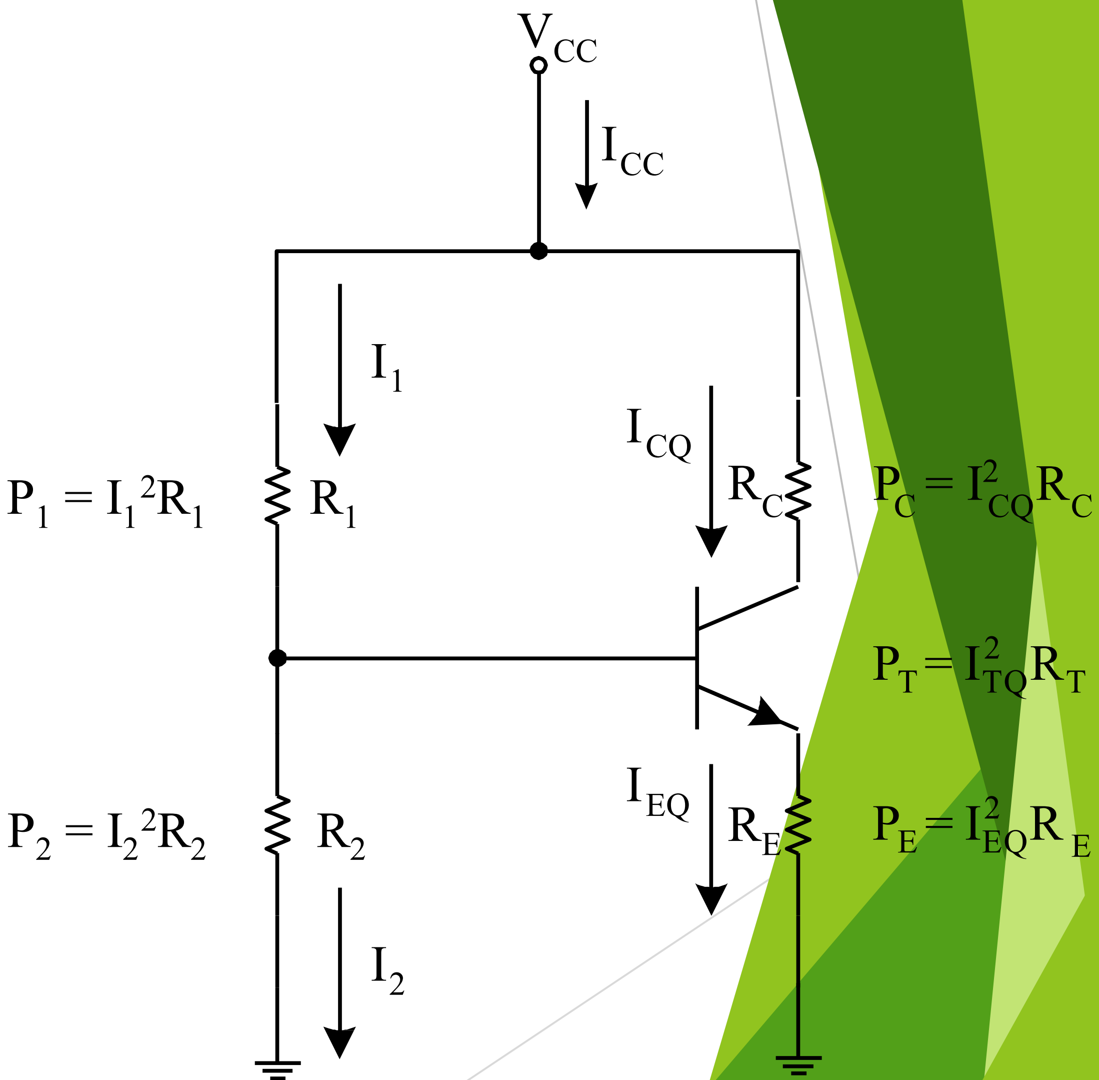
Amplifier Power Dissipation

The **total** amount of power being dissipated by the amplifier, $\boldsymbol{P_{tot}}$, is

$$P_{tot} = P_1 + P_2 + P_C + P_T + P_E$$

The difference between this total value and the total power being drawn from the supply is the power that actually goes to the **load – i.e. output power**.

⇒ **Amplifier Efficiency** $\boldsymbol{\eta}$



Amplifier Efficiency η

- A **figure of merit** for the power amplifier is its efficiency, η.
- **Efficiency (η)** of an amplifier is defined as the ratio of ac output power (power delivered to load) to dc input power .
- By formula :

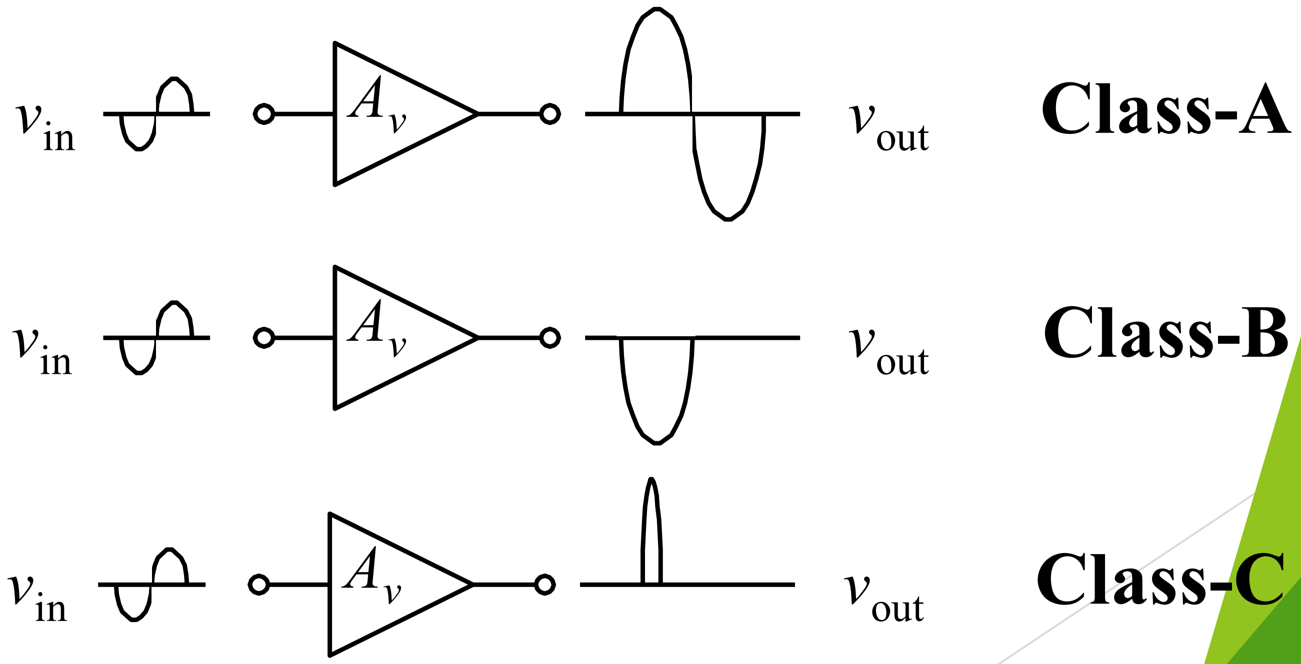
$$\eta = \frac{ac \quad output \quad power}{dc \quad input \quad power} \times 100\% = \frac{P_o(ac)}{P_i(dc)} \times 100\%$$

- As we will see, certain amplifier configurations have much higher efficiency ratings than others.
- This is primary consideration when deciding which type of power amplifier to use for a specific application.

- $\Rightarrow$ **Amplifier Classifications**

Amplifier Classifications

- Power amplifiers are classified according to the percent of time that collector current is **nonzero**.
- The amount the **output** signal varies over **one cycle** of operation for a **full cycle** of **input** signal.

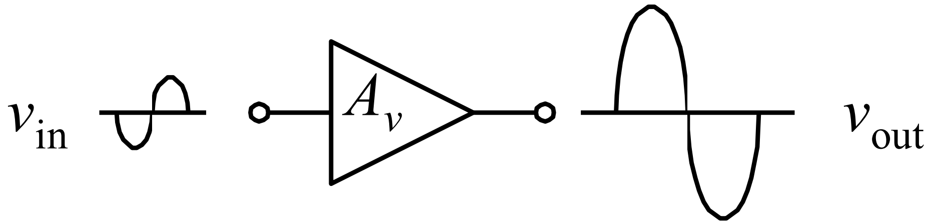


Efficiency Ratings

- The **maximum theoretical efficiency** ratings of class-A, B, and C amplifiers are:

Amplifier	Maximum Theoretical Efficiency, η_{max}
Class A	25%
Class B	78.5%
Class C	99%

Class A Amplifier

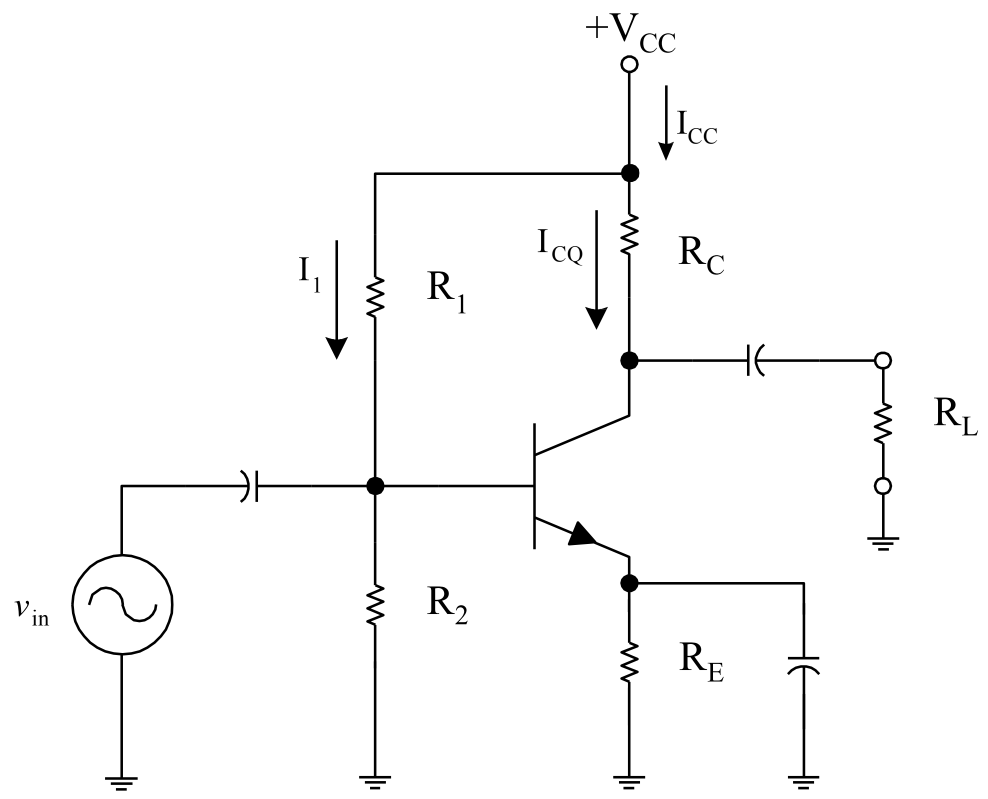


- v_{output} waveform $\rightarrow$ **same shape** $\rightarrow$ v_{input} waveform **+ π phase shift.**

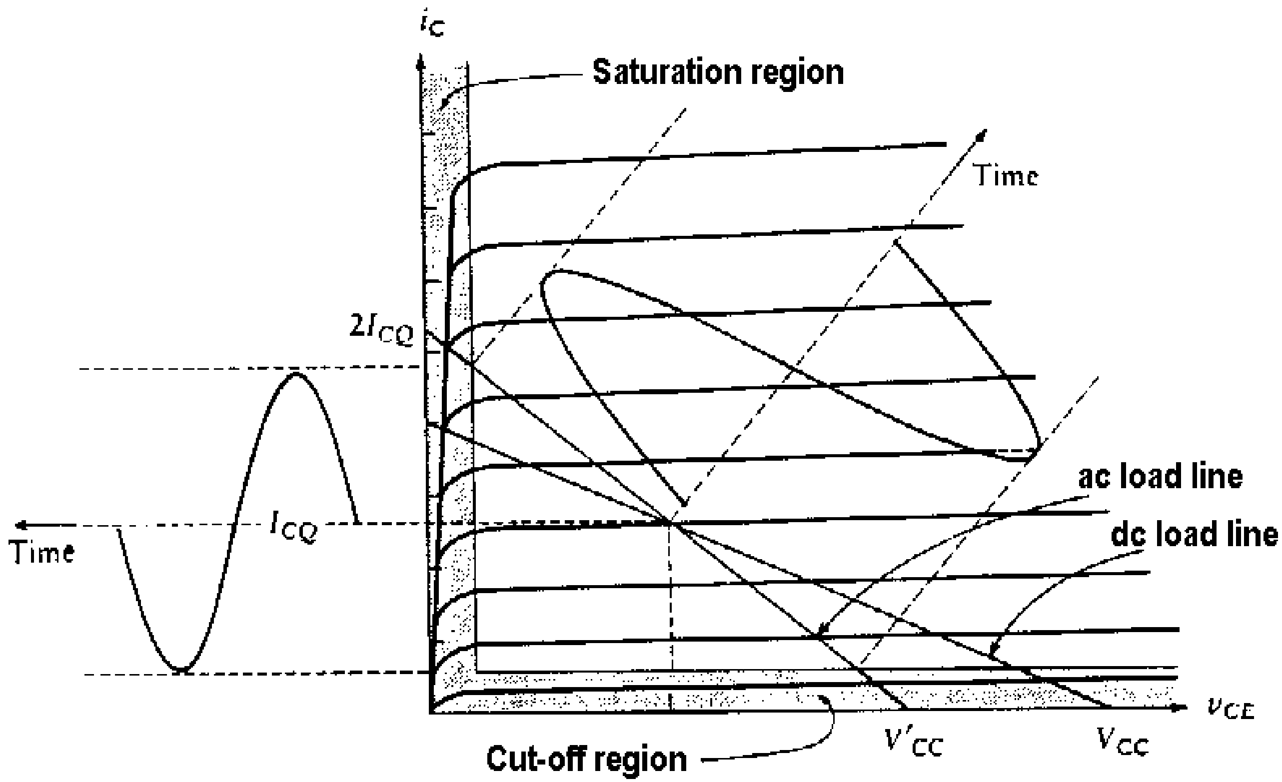
- The collector current is **nonzero** 100% of the time.
  $\rightarrow$ **inefficient**, since even with zero input signal, I_{CQ} is nonzero
  (i.e. transistor dissipates power in the rest, or quiescent, condition)

Basic Operation

Common-emitter (voltage-divider) configuration (RC-coupled amplifier)



Typical Characteristic Curves for Class-A Operation



Typical Characteristic

- Previous figure shows an example of a sinusoidal input and the resulting collector current at the output.
- The current, I_{CQ} , is usually set to be in the **center** of the ac load line. Why?

(DC and AC analyses $\rightarrow$ discussed in previous sessions)

DC Input Power

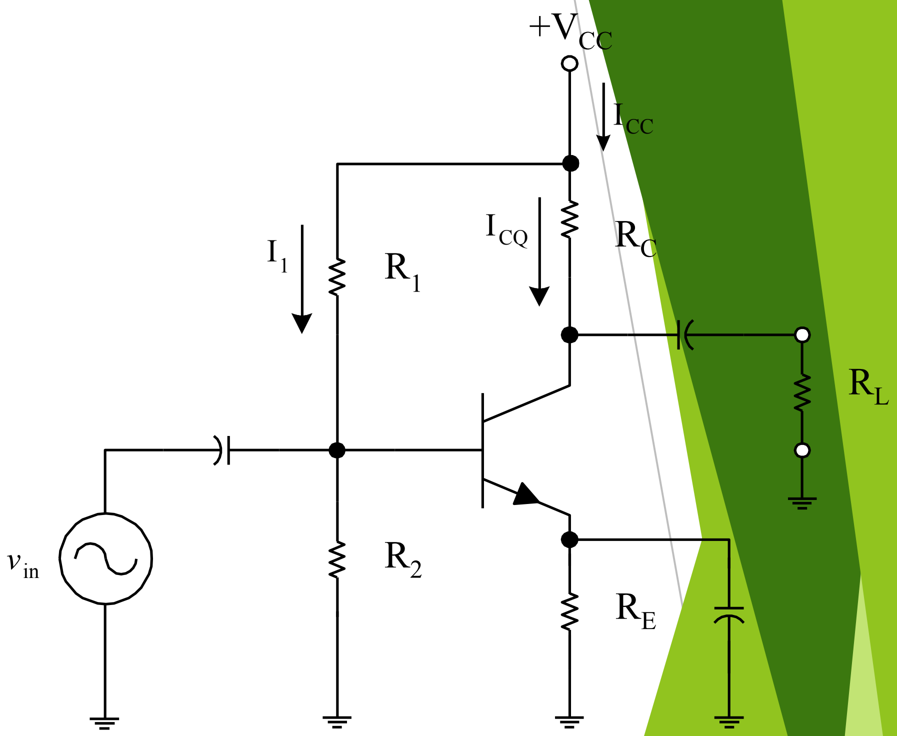
amplifier draws from the power supply :

$$P_i(dc) = V_{CC} I_{CC}$$

$$I_{CC} = I_{CQ} + I_1$$

$$I_{CC} \approx I_{CQ} \qquad (I_{CQ} >> I_1)$$

$$P_i(dc) = V_{CC} I_{CQ}$$

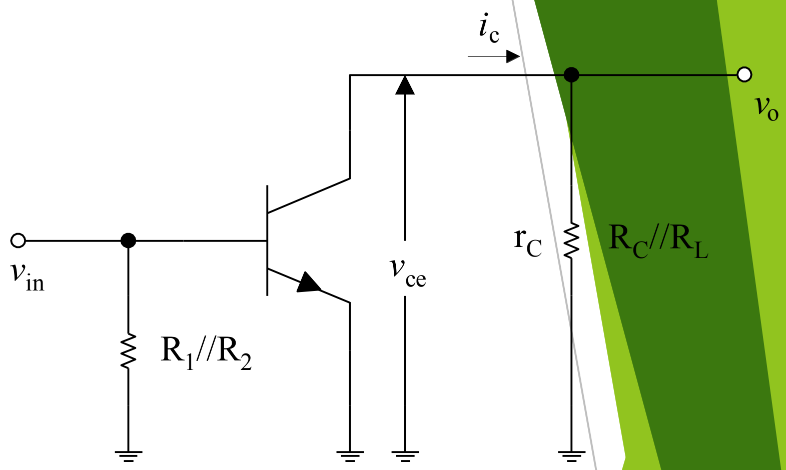


Note that this equation is valid for most amplifier power analyses. We can rewrite for the above equation for the **ideal** amplifier as

$$P_i(dc) = 2V_{CEQ} I_{CQ}$$

AC Output Power

$$P_o(ac) = i_{c(rms)} v_{o(rms)} = \frac{v^2_{o(rms)}}{R_L}$$

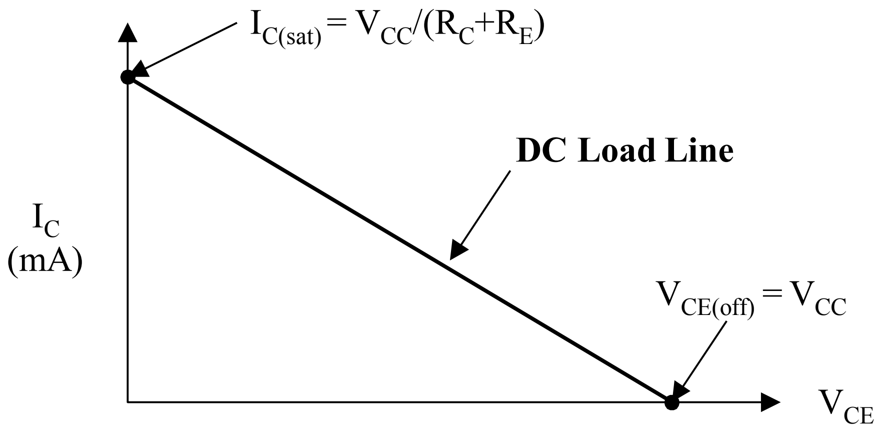


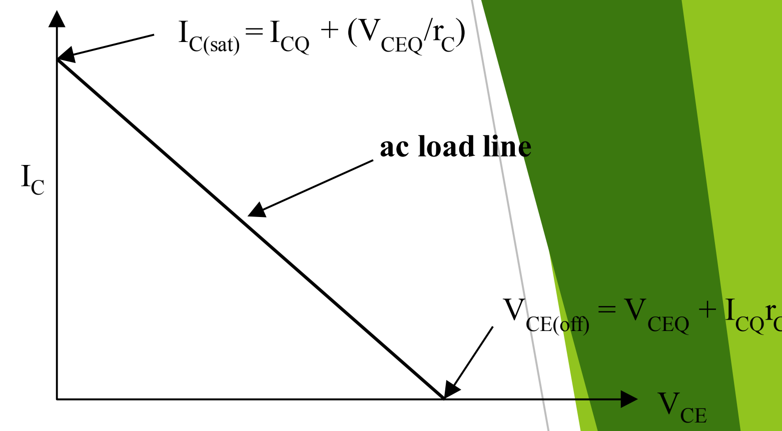
Above equations can be used to calculate the **maximum** possible value of ac load power. HOW??

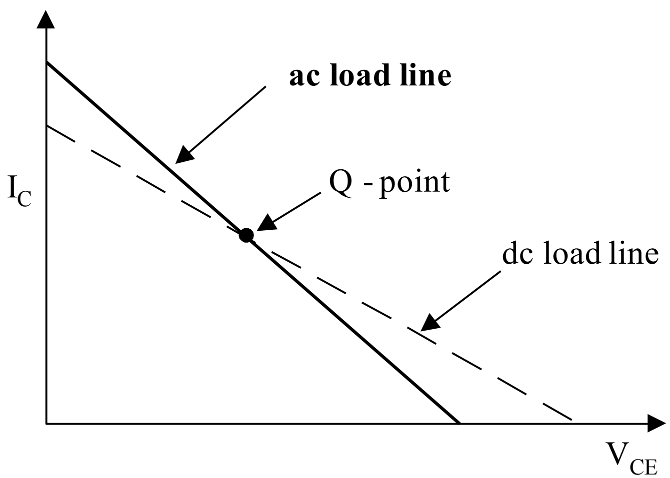
Disadvantage of using class-A amplifiers is the fact that their efficiency ratings are so low, $\boldsymbol{\eta_{max} \approx 25\%}$.

Why?? A majority of the power that is drawn from the supply by a class-A amplifier is used up by the amplifier itself.

$\rightarrow$ **Class-B Amplifier**



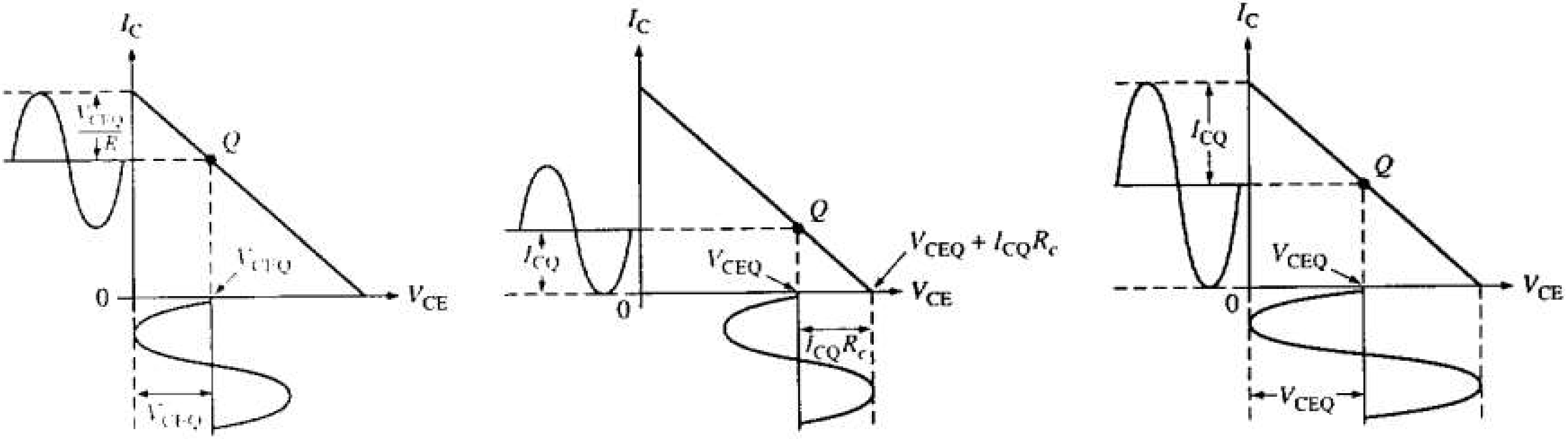




$$P_o(ac) = \left(\frac{V_{CEQ}}{\sqrt{2}}\right)\left(\frac{I_{CQ}}{\sqrt{2}}\right) = \frac{1}{2}V_{CEQ}I_{CQ} = \frac{V_{PP}^2}{8R_L}$$

$$\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% = \frac{\frac{1}{2}V_{CEQ}I_{CQ}}{2V_{CEQ}I_{CQ}} \times 100\% = 25\%$$

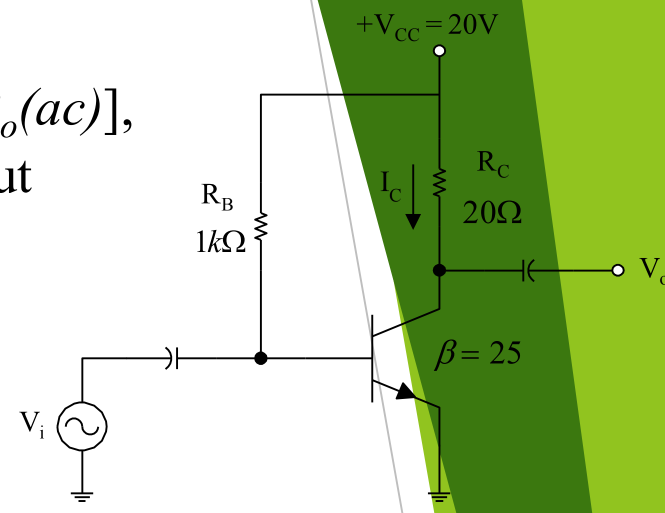
Limitation



(a) Limited by saturation (b) Limited by cutoff (c) Centered Q-point

Example

Calculate the input power [$P_i(dc)$], output power [$P_o(ac)$], and efficiency [η] of the amplifier circuit for an input voltage that results in a base current of 10mA peak.



$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20V - 0.7V}{1k\Omega} = 19.3mA$$

$$I_{CQ} = \beta I_B = 25(19.3mA) = 482.5mA \cong 0.48A$$

$$V_{CEQ} = V_{CC} - I_C R_C = 20V - (0.48A)(20\Omega) = 10.4V$$

$$I_{c(sat)} = \frac{V_{CC}}{R_C} = \frac{20V}{20\Omega} = 1000mA = 1A$$

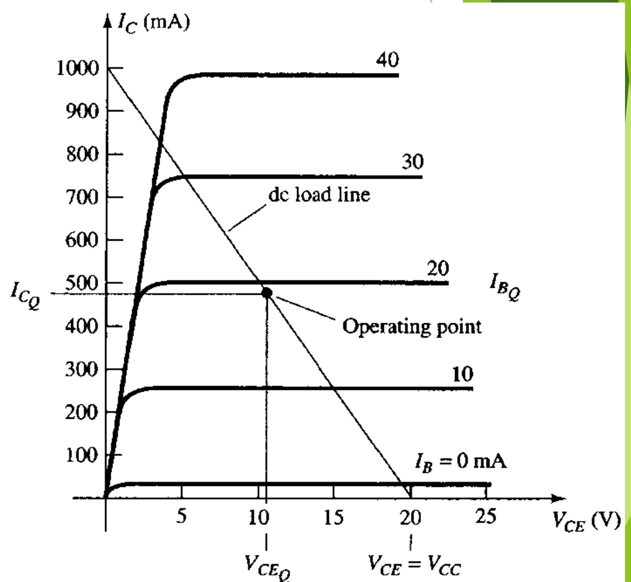
$$V_{CE(cutoff)} = V_{CC} = 20V$$

$$I_{C(peak)} = \beta I_{b(peak)} = 25(10mA\ peak) = 250mA\ peak$$

$$P_{o(ac)} = \frac{I^2_{C(peak)}}{2} R_C = \frac{\left(250\times10^{-3}A\right)^2}{2}(20\Omega) = 0.625W$$

$$P_{i(dc)} = V_{CC} I_{CQ} = (20V)(0.48A) = 9.6W$$

$$\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\% = 6.5\%$$



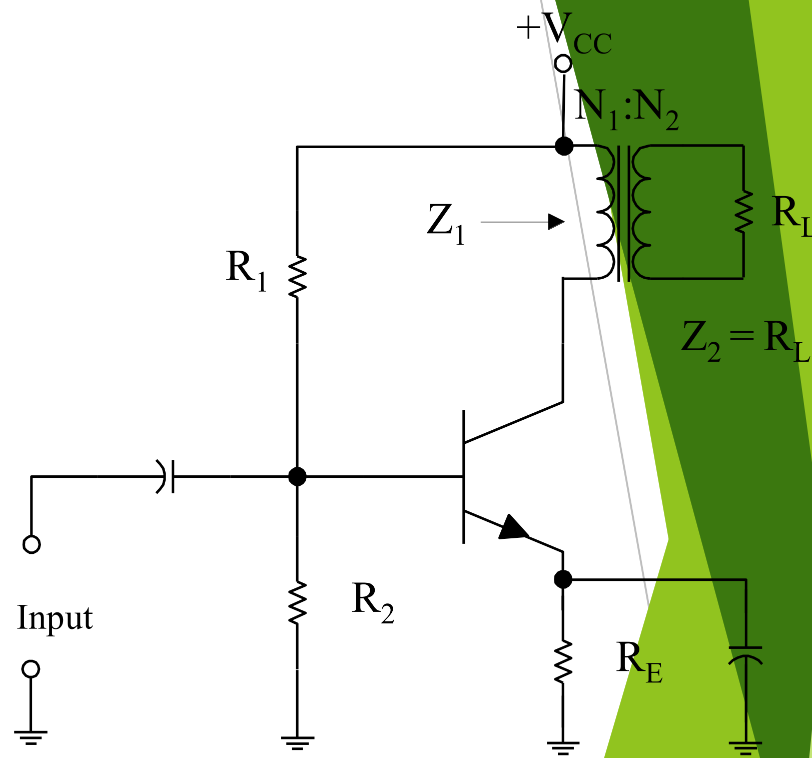
Transformer-Coupled Class-A Amplifier

A transformer-coupled class-A amplifier uses a transformer to couple the output signal from the amplifier to the load.

The relationship between the primary and secondary values of voltage, current and impedance are summarized

$$\frac{N_1}{N_2} = \frac{V_1}{V_2} = \frac{I_2}{I_1}$$

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{Z_1}{Z_2} = \frac{Z_1}{R_L}$$

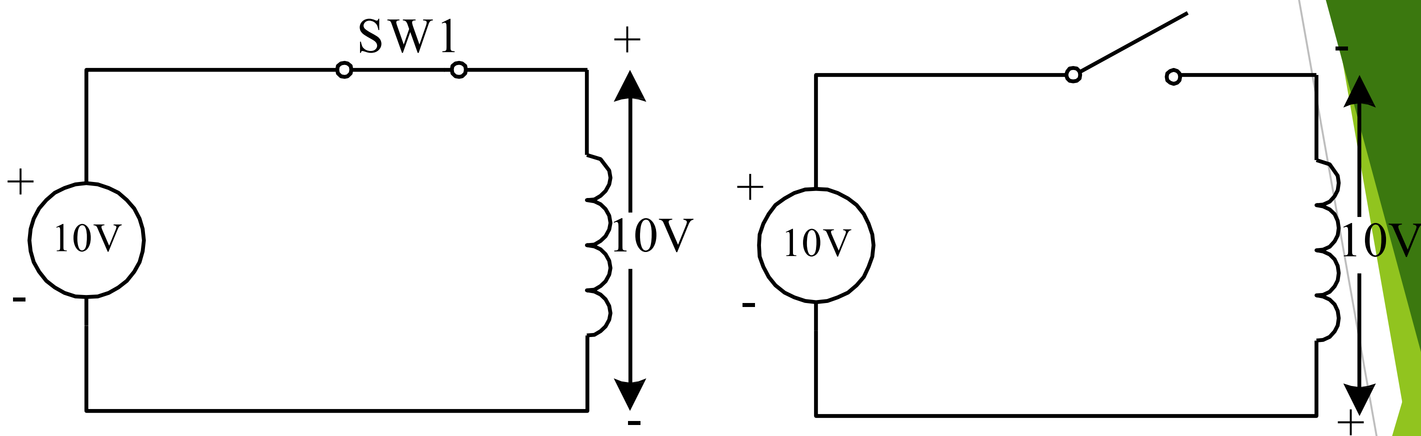


N_1, N_2 = the number of turns in the primary and secondary
V_1, V_2 = the primary and secondary voltages
I_1, I_2 = the primary and secondary currents
Z_1, Z_2 = the primary and seconadary impedance ($Z_2 = R_L$)

Transformer-Coupled Class-A Amplifier

- An **important** characteristic of the transformer is the ability to produce a **counter emf**, or **kick** emf.
- When an inductor experiences a rapid change in supply voltage, it will produce a voltage with a polarity that is opposite to the original voltage polarity.
- The counter emf is caused by the electromagnetic field that surrounds the inductor.

Counter emf

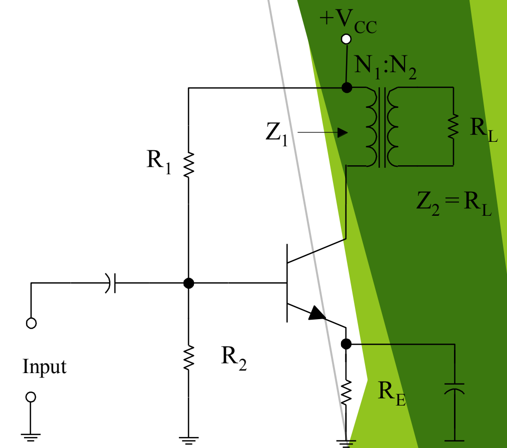


This counter emf will be present only for an instant.

As the field collapses into the inductor the voltage decreases in value until it eventually reaches 0V.

The dc biasing of a transformer-coupled class-A amplifier is very similar to any other class-A amplifier with **one important exception** :

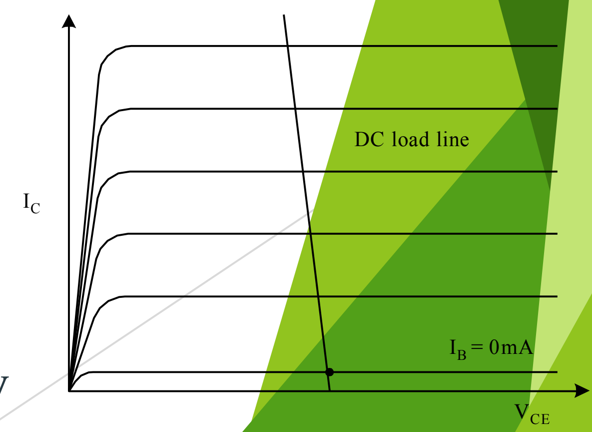
→ the value of V_{CEQ} is **designed** to be as close as possible to V_{CC}.



indicating that V_{CEQ} will be approximately equal to V_{CC} for all the values of I_C.

The nearly **vertical** load line of the transformer-coupled amplifier is caused by the **extremely low dc resistance** of the transformer primary.

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)}$$



The value of R_L is **ignored** in the dc analysis of the transformer-coupled class-A amplifier. The reason for this is the fact that transformer provides **dc isolation** between the primary and secondary. Since the load resistance is in the secondary of the transformer it **dose not** affect the dc analysis of the primary circuitry

Determine the maximum possible change in V_{CE}

- Since V_{CE} cannot change by an amount greater than $(V_{CEQ} - 0V)$, $v_{ce} = V_{CEQ}$.

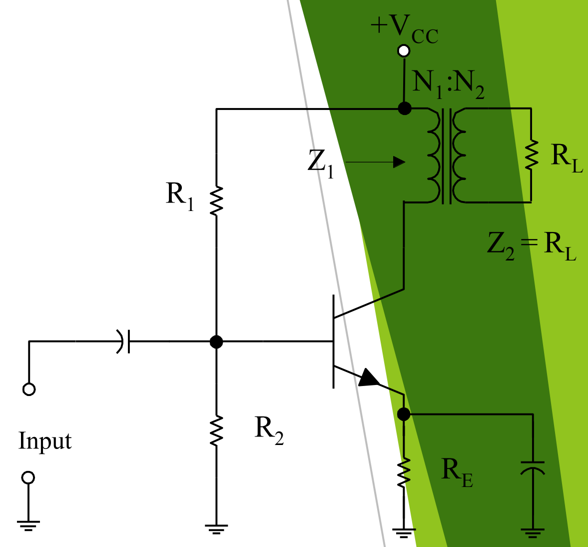
2. Determine the corresponding change in I_C

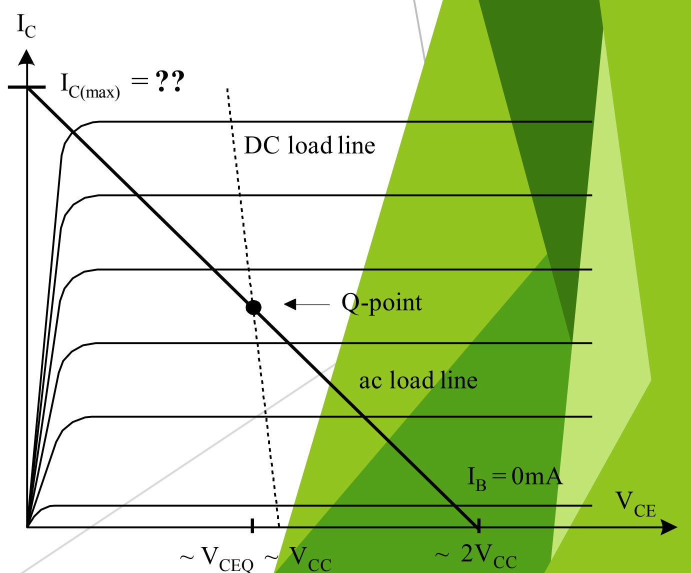
- Find the value of Z_1 for the transformer: $Z_1 = (N_1/N_2)^2 Z_2$ and $i_c = v_{ce} / Z_1$

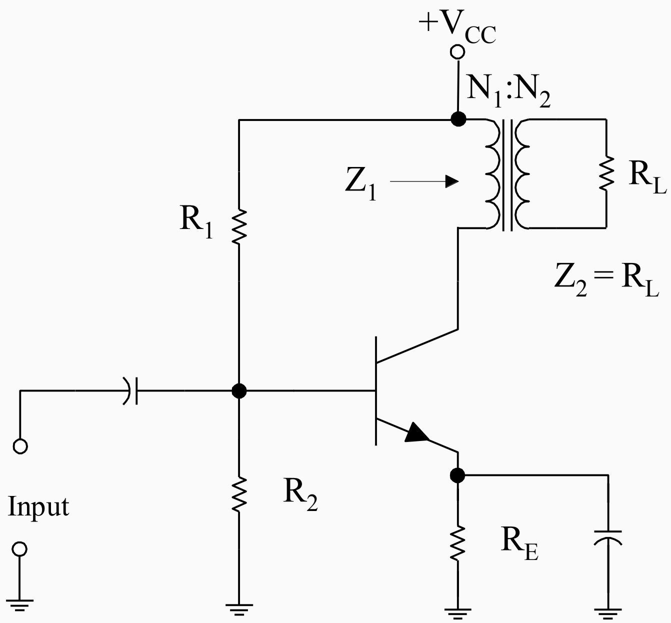
3. Plot a line that passes through the Q-point and the value of $I_{C(max)}$.

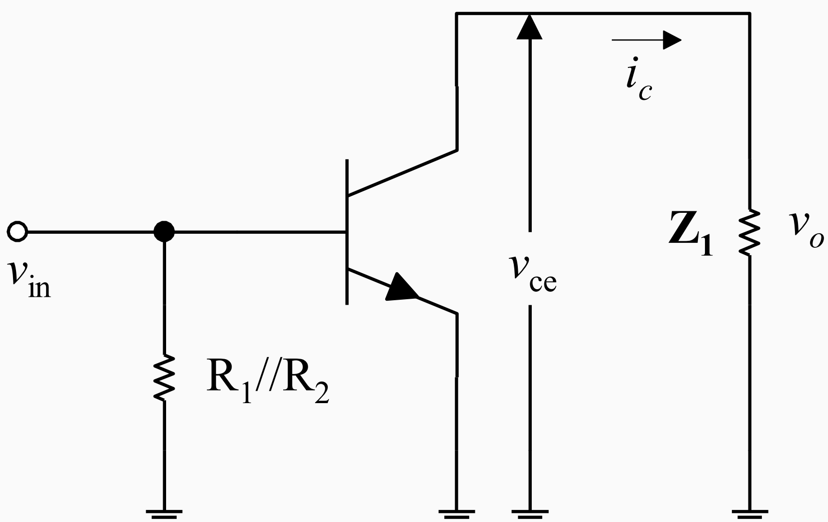
- $I_{C(max)} = I_{CQ} + i_c$

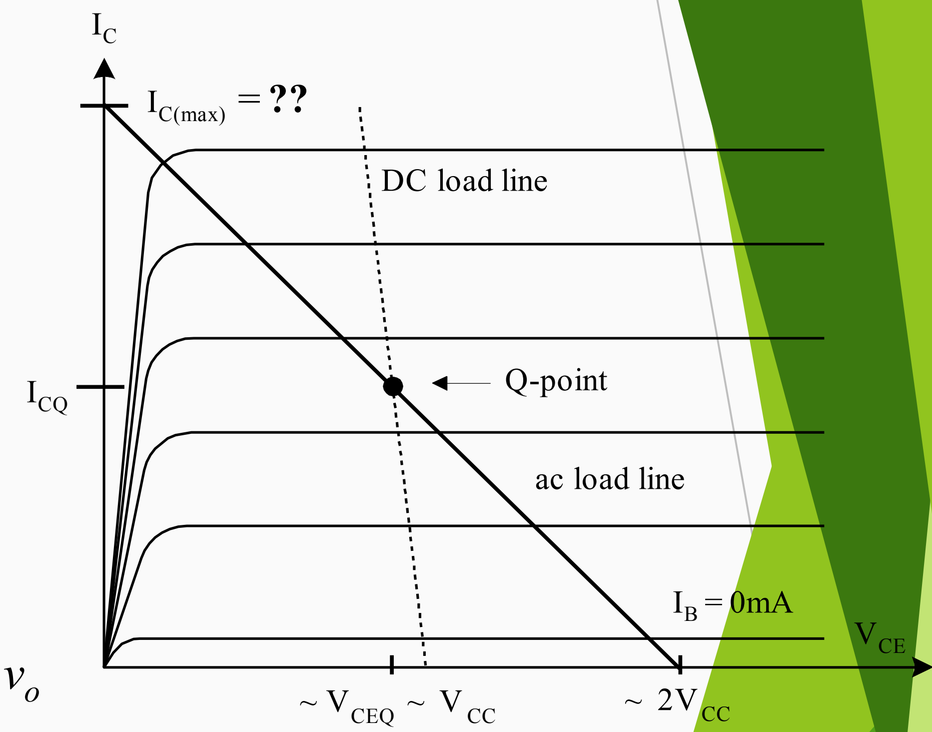
4. Locate the two points where the load line passes through the lies representing the minimum and maximum values of I_B. These two points are then used to find the maximum and minimum values of I_C and V_{CE}






+VCC
N1:N2
Z1
RL
R1
Z2 = RL
Input
R2
RE

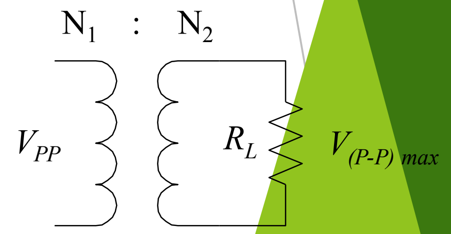

ic
vin
R1//R2
vce
Z1
vo


IC
IC(max) = ??
DC load line
ICQ
Q-point
ac load line
IB = 0mA
VCE
~ VCEQ ~ VCC
~ 2VCC

Maximum load power and efficiency

The Power Supply for the amplifier : $P_S = V_{CC} I_{CC}$

Maximum peak-to-peak voltage across the primary of the transformer is approximately equal to the difference between the values of $V_{CE(max)}$ and $V_{CE(min)}$: $V_{PP} = V_{CE(max)} - V_{CE(min)}$



Maximum possible peak-to-peak **load voltage** is found by

$$\boxed{V_{(P\text{-}P)max} = (N_2 / N_1) V_{PP}}$$

The **actual efficiency** rating of a transformer-coupled class-A amplifier will generally be **less than 40%**.

There are several reasons for the difference between the practical and theoretical efficiency ratings for the amplifier :

1. The derivation of the η = 50% value assumes that $V_{CEQ} = V_{CC}$. In practice, V_{CEQ} will always be some value that is less the V_{CC} .
2. The transformer is subject to various power losses. Among these losses are couple loss and hysteresis loss. These transformer power losses are not considered in the derivation of the η = 50% value.

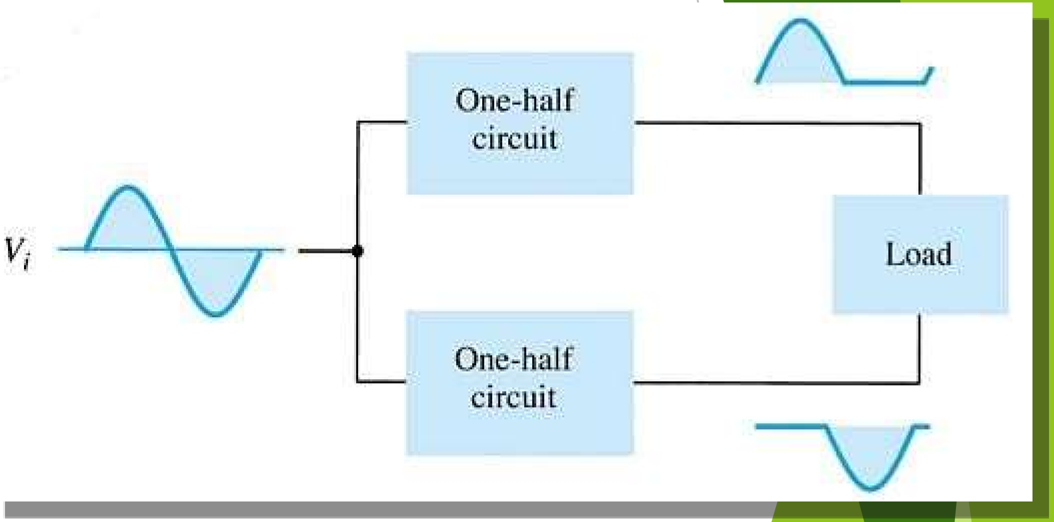
- One of the **primary advantages** of using the transformer-coupled class-A amplifier is the **increased efficiency** over the RC-coupled class-A circuit.
- **Another advantage** is the fact that the transformer-coupled amplifier is **easily converted into** a type of amplifier that is used extensively in communications :- the **tuned amplifier**.
- A tuned amplifier is a circuit that is designed to have a specific value of power gain over a **specific range of frequency**.

B Amplifier

In class B, the transistor is biased just off. The AC signal turns the transistor on.

The transistor only conducts when it is turned on by one-half of the AC cycle.

In order to get a full AC cycle out of a class B amplifier, you need two transistors:



- **An *npn* transistor that provides the negative half of the AC cycle**
- **A *pnp* transistor that provides the positive half.**

Class B Amplifier

- Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half cycle, the circuit is referred to as a push-pull circuit

Input DC power

- The power supplied to the load by an amplifier is drawn from the power supply
- The amount of this DC power is calculated using

$$P_{i(dc)} = V_{CC} I_{dc}$$

- The DC current drawn from the source is the average value of the current delivered to the load

Input DC power

- The current drawn from a single DC supply has the form of a full wave rectified signal, while that drawn from two power supplies has the form of half-wave rectified signal from each supply
- On either case the average value for the current is given by $I_{dc} = \frac{2}{\pi} \times I_p$
- The input power can be written as

$$P_{i(dc)} = \frac{2}{\pi} V_{CC} I_p$$

Output AC power

- The power delivered to the load can be calculated using the following equation

$$P_{o(ac)} = \frac{V_{L(p-p)}}{8R_L} = \frac{V_{L(p)}}{2R_L}$$

- The efficiency of the amplifier is given by

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

- Not that $I_p = \frac{V_{L(p)}}{R_L}$
- Therefore the efficiency can be re-expressed as

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4}\frac{V_L(\text{p})}{V_{CC}} \times 100\%$$

Output AC power

- The maximum efficiency can be obtained if

$$V_L(\mathrm{p}) = V_{CC}$$

- The value of this maximum efficiency will be

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power dissipated by the output transistors

- The power dissipated by the output transistors as heat is given by $P_{2Q} = P_i(\mathrm{dc}) - P_o(\mathrm{ac})$
- The power in each transistor is given by

$$P_Q = \frac{P_{2Q}}{2}$$

Example

__Example 1:__ For class B amplifier providing a 20-V peak signal to a 16-Ω speaker and a power supply of V_{CC}=*30 V*, determine the input power , output power and the efficiency

__Solution:__

The input power is given by $$P_{i(dc)} = \frac{2}{\pi} V_{CC} I_p$$

The peak collector load current can be found from

$$I_L(\mathrm{p}) = \frac{V_L(\mathrm{p})}{R_L} = \frac{20\ \mathrm{V}}{16\ \Omega} = 1.25\ \mathrm{A}$$

Example

__Solution:__

The input power is $P_{i(dc)} = \frac{2}{\pi}30(1.25) = 23.9\ W$

The output power is given by

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(20\text{ V})^2}{2(16\ \Omega)} = \mathbf{12.5\ W}$$

The efficiency is

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{12.5\text{ W}}{23.9\text{ W}} \times 100\% = \mathbf{52.3\%}$$

Maximum power dissipated by the output transistors

- The maximum power dissipated by the two transistors occurs when the output voltage across the load is given by

$$V_L(\text{p}) = 0.636V_{CC} \qquad \left(= \frac{2}{\pi}V_{CC}\right)$$

- The maximum power dissipation is given by

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

Example

<u>Example 2:</u> For class B amplifier using a supply of *V_{CC}=30 V and driving a load of 16-Ω*, determine the input power , output power and the efficiency

<u>Solution:</u>

The maximum output power is given by

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{2(16\ \Omega)} = \mathbf{28.125\ W}$$

The maximum input power drawn from the supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30\text{ V})^2}{\pi(16\ \Omega)} = \mathbf{35.81\ W}$$

Example

<u>*Solution:*</u>

The efficiency is given by

$$\text{maximum } \%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125\ \text{W}}{35.81\ \text{W}} \times 100\% = 78.54\%$$

The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30\ \text{V})^2}{\pi^2 16\ \Omega}\right] = \mathbf{5.7\ W}$$

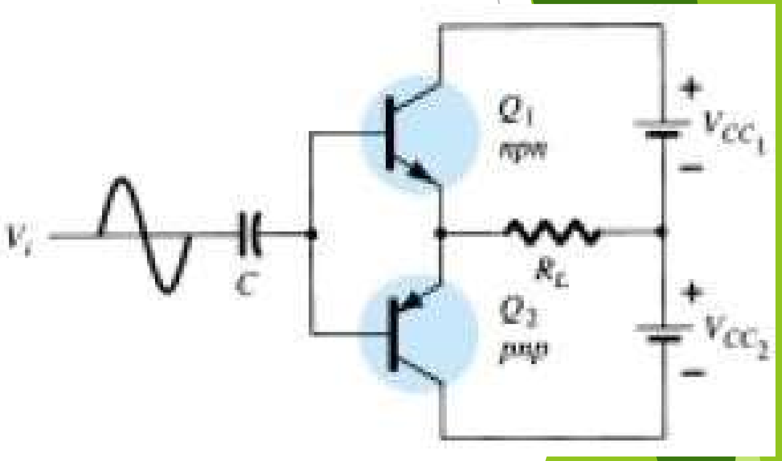
Class B Amplifier circuits

- A number of circuit arrangements can be used to realize class B amplifier
- We will consider in this course two arrangements in particular

1. The first arrangement uses a single input signal fed to the input of two complementary transistors (complementary symmetry circuits)
2. The second arrangement uses two out of phase input signals of equal amplitudes feeded to the input of two similar NPN or PNP transistors (quasi-complementary push-pull amplifier)

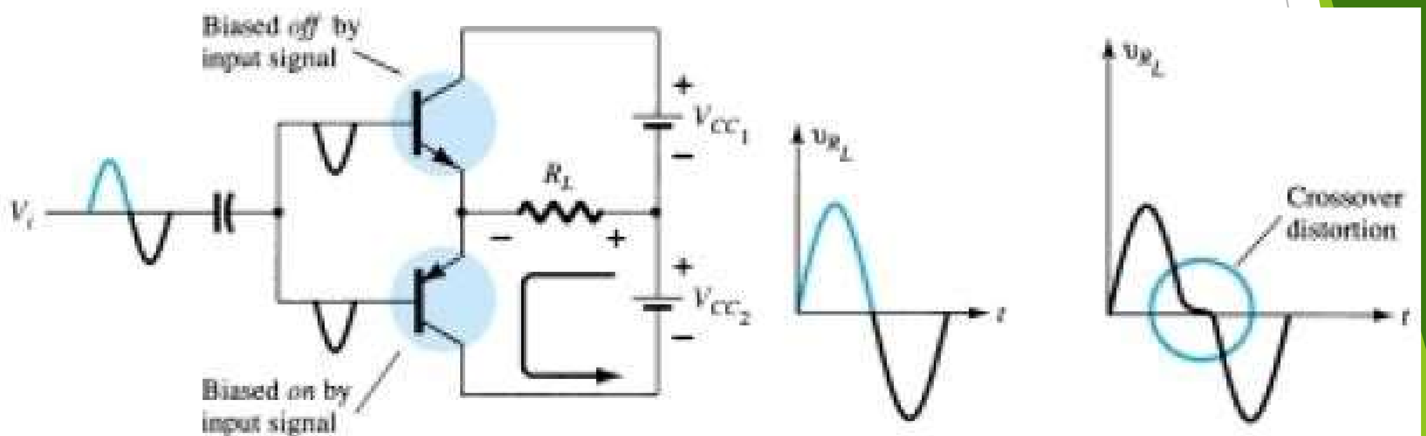
Complementary symmetry circuits first arrangement

- This circuit uses both npn and pnp transistor to construct class B amplifier as shown to the left
- One disadvantage of this circuit is the need for two separate voltage supplies



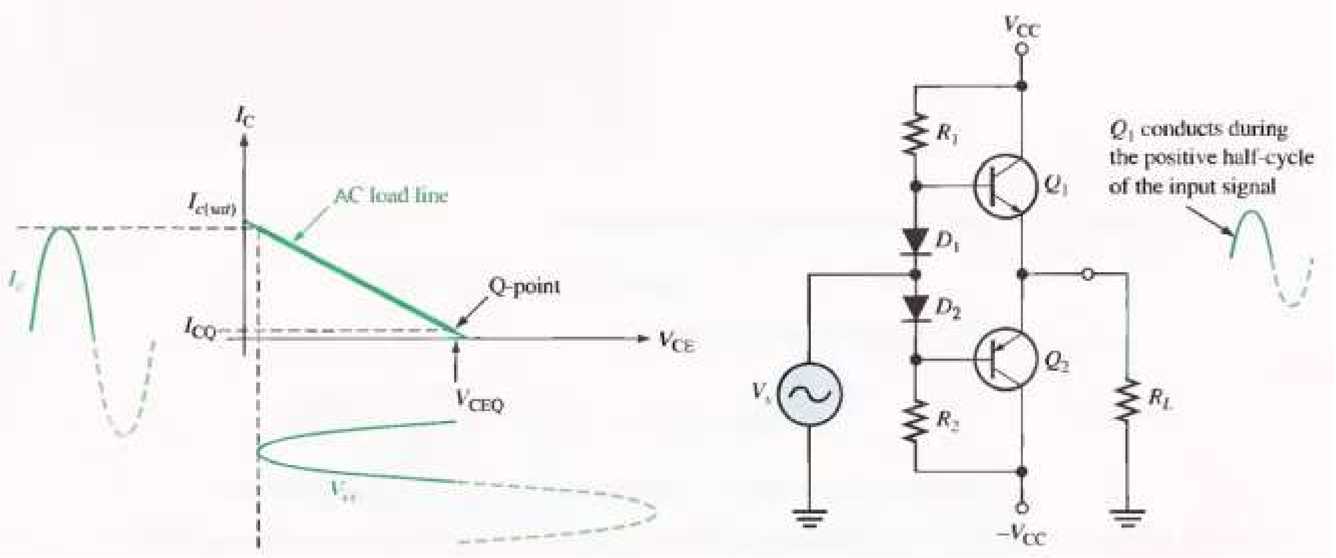
Complementary symmetry circuits

- another disadvantage of this circuit is the resulting cross over distortion



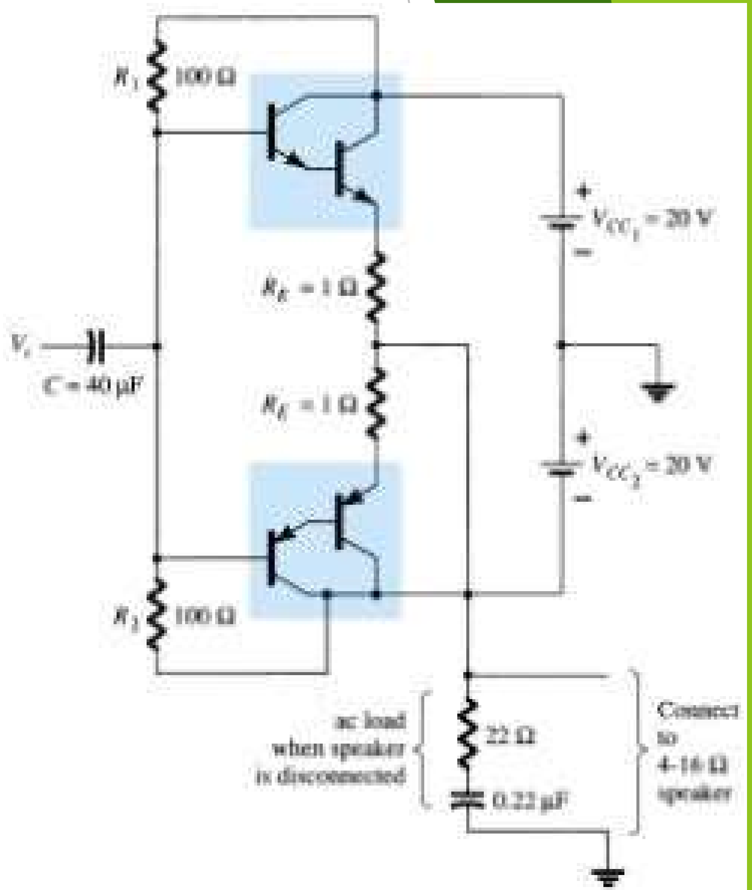
- Cross over distortion can be eliminated the by biasing the transistors in class AB operation where the transistors are biased to be on for slightly more than half a cycle

Class AB biasing to solve crossover distortion



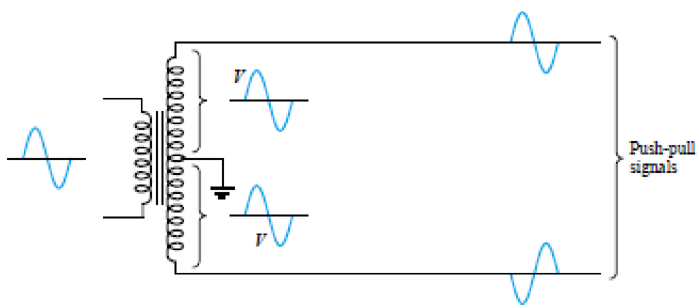
Complementary symmetry circuits

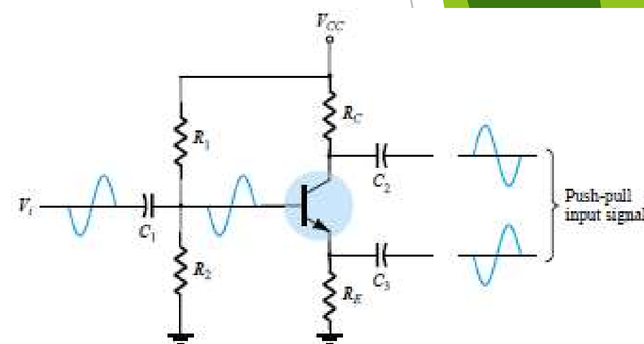
- A more practical version of a push-pull circuit using complementary transistors is shown to the right
- This circuit uses to complementary Darlington pair transistors to achieve larger current driving and lower output impedance

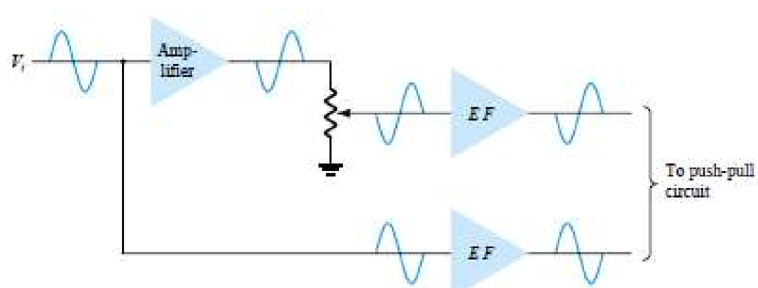


Second arrangement

- As stated previously the second arrangement which uses two equal input signals of opposite phase has to be preceded by a phase inverting network as shown below

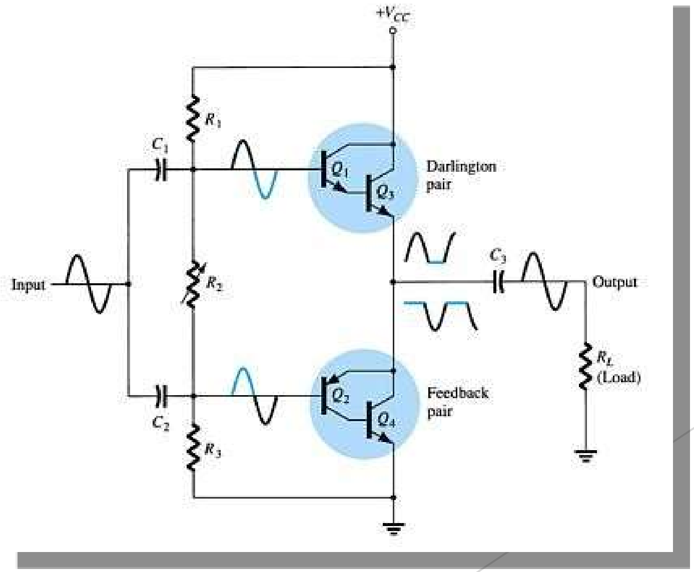






Quasi-complementary push pull amplifier second arrangement

- In practical power amplifier circuits it is preferable to uses npn for both transistors
- Since the push pull connection requires complementary devices, a pnp high power transistor must be used.
- This can be achieved by using the circuit shown



Example

__Example:__ For the circuit shown, calculate the input power, output power and the power handled by each transistor and the efficiency if the input signal is 12 V_{rms}

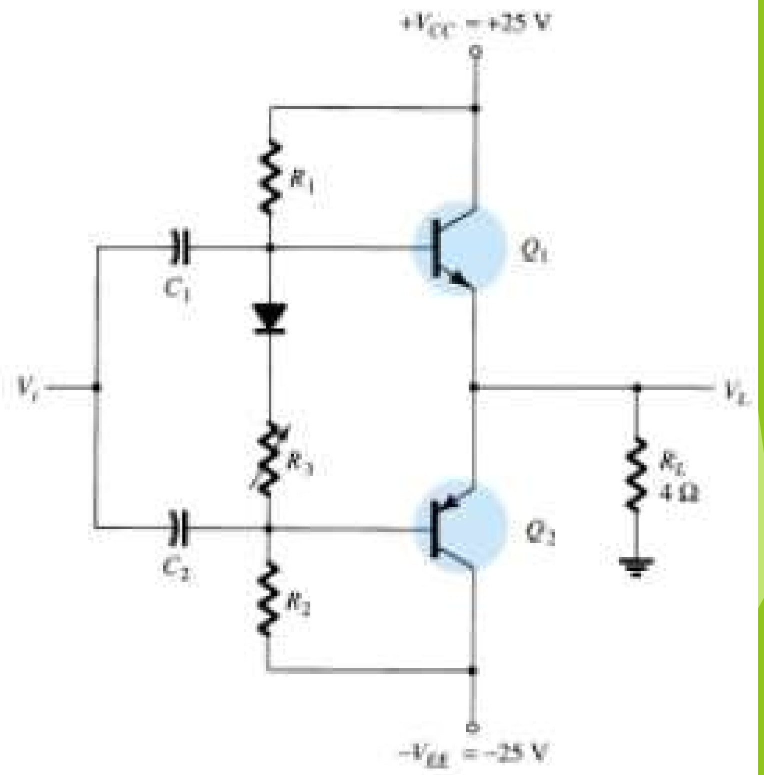
__Solution:__

The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\, V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

The output power is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = 36.125\text{ W}$$



Example

<u>*Solution:*</u>

The peak load current is $I_L(\text{p}) = \dfrac{V_L(\text{p})}{R_L} = \dfrac{17\ \text{V}}{4\ \Omega} = 4.25\ \text{A}$

The dc current can be found from the peak as

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2(4.25\ \text{A})}{\pi} = 2.71\ \text{A}$$

The input power is given by

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = (25\ \text{V})(2.71\ \text{A}) = \mathbf{67.75\ W}$$

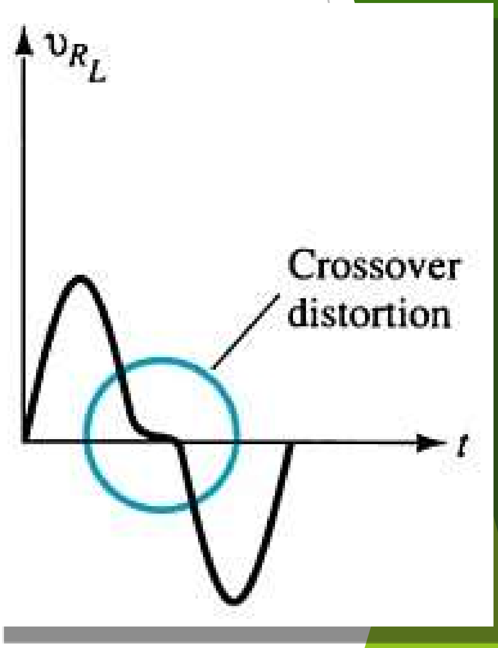
The power dissipated by each transistor is given by

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\ \text{W} - 36.125\ \text{W}}{2} = \mathbf{15.8\ W}$$

$$\%\ \eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125\ \text{W}}{67.75\ \text{W}} \times 100\% = \mathbf{53.3\%}$$

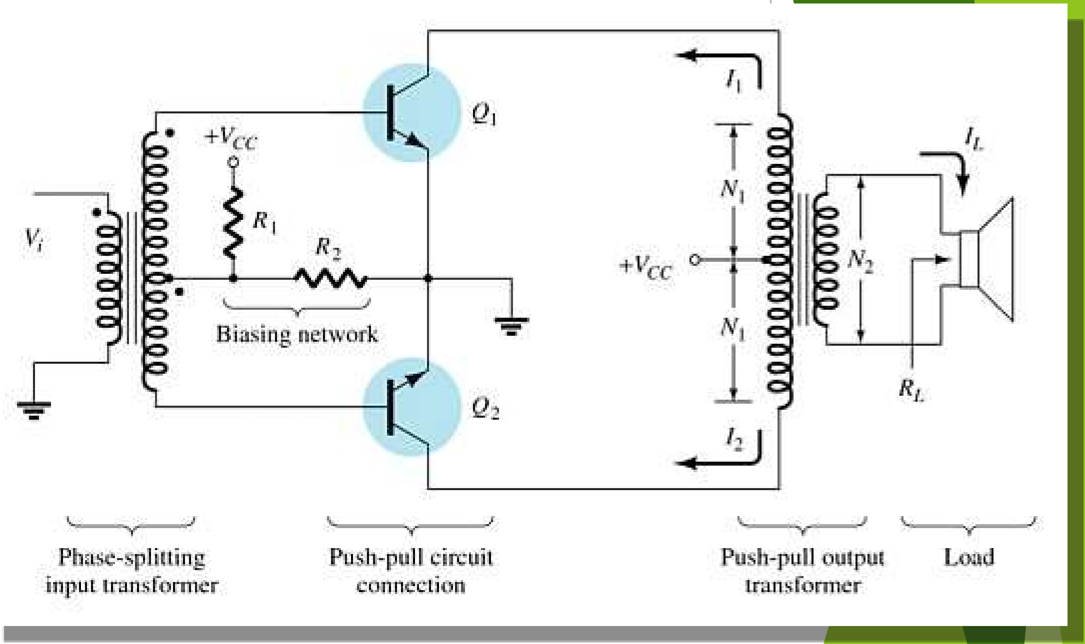
Crossover Distortion

If the transistors Q_1 and Q_2 do not turn on and off at exactly the same time, then there is a gap in the output voltage.



Class B Amplifier Push-Pull Operation

- During the positive half-cycle of the AC input, transistor Q_1 (*npn*) is conducting and Q_2 (*pnp*) is off.
- During the negative half-cycle of the AC input, transistor Q_2 (*pnp*) is conducting and Q_1 (*npn*) is off.



Each transistor produces one-half of an AC cycle. The transformer combines the two outputs to form a full AC cycle.

This circuit is less commonly used in modern circuits

Amplifier Distortion

If the output of an amplifier is not a complete AC sine wave, then it is distorting the output. The amplifier is non-linear.

This distortion can be analyzed using Fourier analysis. In Fourier analysis, any distorted periodic waveform can be broken down into frequency components. These components are harmonics of the fundamental frequency

Harmonics

Harmonics are integer multiples of a fundamental frequency.

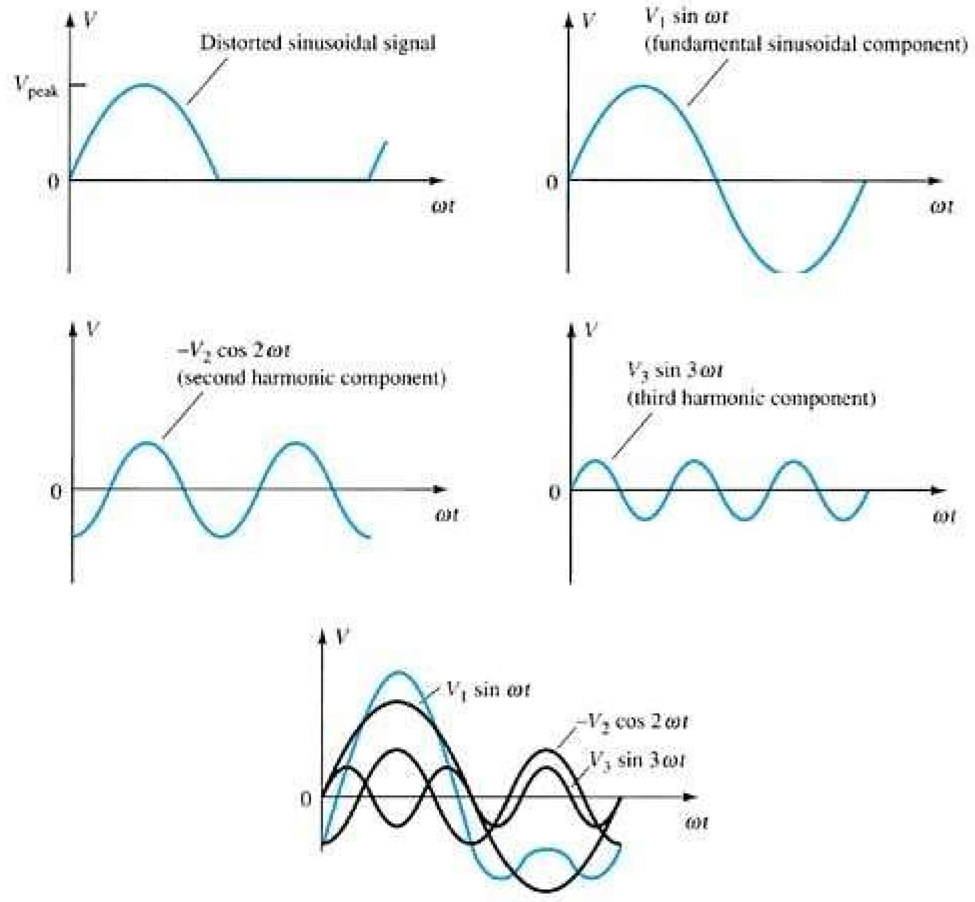
If the fundamental frequency is 5kHz:

1st harmonic	**1 x 5kHz**
2nd harmonic	**2 x 5kHz**
3rd harmonic	**3 x 5kHz**
4th harmonic	**4 x 5kHz**
etc.	

Note that the 1st and 3rd harmonics are called odd harmonics and the 2nd and 4th are called even harmonics

Harmonic Distortion

According to Fourier analysis, if a signal is not purely sinusoidal, then it contains harmonics.



Harmonic Distortion Calculations

Harmonic distortion (D) can be calculated:

$$\%\text{ nth harmonic distortion} = \%D_n = \left|\frac{A_n}{A_1}\right| \times 100$$

where

A_1 is the amplitude of the fundamental frequency

A_n is the amplitude of the highest harmonic

The total harmonic distortion (THD) is determined by:

$$\%\,\mathbf{THD} = \sqrt{D_2^2 + D_3^2 + D_3^2 + \square} \times 100$$

EXAMPLE 16.13

Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution

Using Eq. (16.30) yields

$$\% D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{10\%}$$

$$\% D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{4\%}$$

$$\% D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{2\%}$$

EXAMPLE 16.14

Calculate the total harmonic distortion for the amplitude components given in Example 16.13.

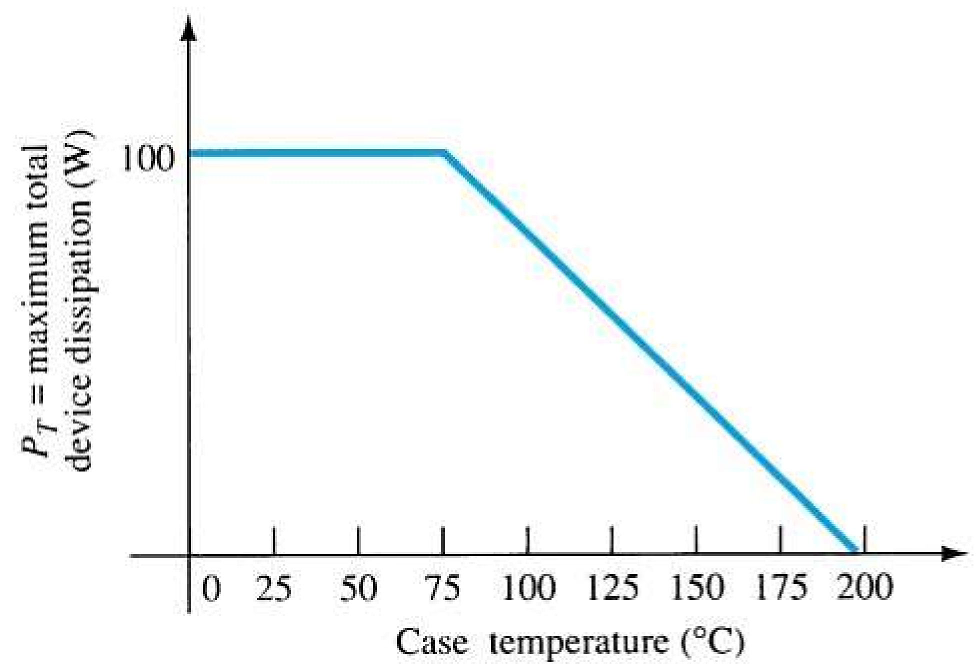
Solution

Using the computed values of $D_2 = 0.10$, $D_3 = 0.04$, and $D_4 = 0.02$ in Eq. (16.31),

$$\begin{aligned}\%\text{ THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= \mathbf{10.95\%}\end{aligned}$$

Power Transistor Derating Curve

Power transistors dissipate a lot of power in heat. This can be destructive to the amplifier as well as to surrounding components



Unit -4(b)

LINEAR WAVE SHAPING

Wave Shaping

<u>Definition</u>: It is the process of changing the shape of input signal with linear / non-linear circuits.

<u>Types</u>:

i. Linear Wave Shaping

ii. Non-linear Wave Shaping

Linear Wave Shaping

<u>Definition</u>: The process where by the form of a non-sinusoidal signal is changed by transmission through a linear network is called Linear Wave Shaping.

<u>Types</u>:

i. High Pass RC Circuit.

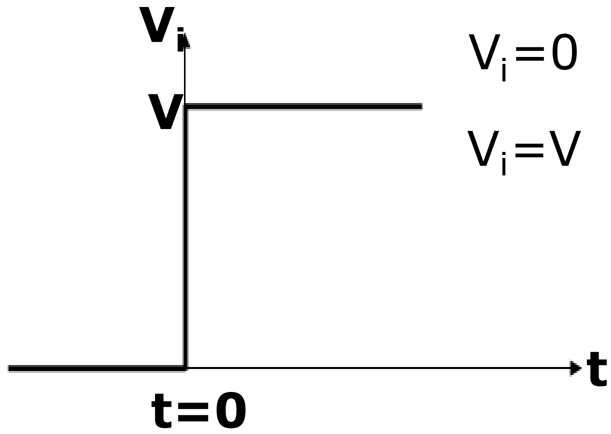
ii. Low Pass RC Circuit.

Non-sinusoidal wave forms

1) Step
2) Pulse
3) Square wave
4) Ramp
5) Exponential wave forms.

Step Waveform

A step voltage is one which maintains the value zero for all times t<0 and maintains the value V for all times t>0.

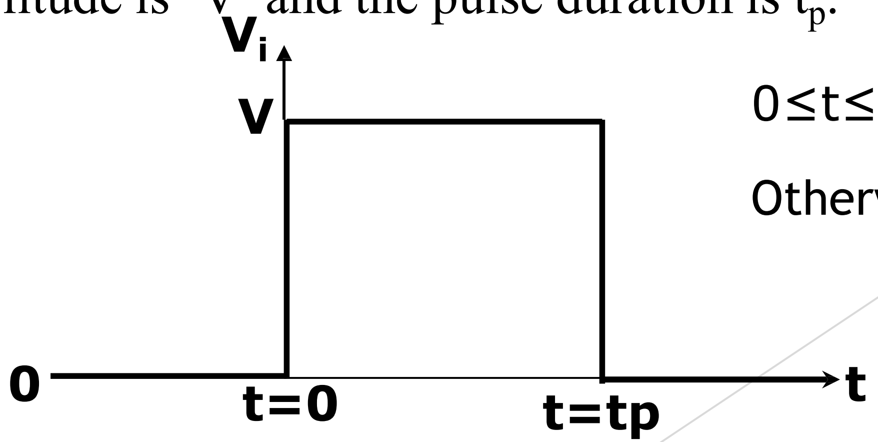


$V_i=0 \quad t<0$

$V_i=V \quad t>0$

Pulse

The pulse amplitude is 'V' and the pulse duration is t_p.

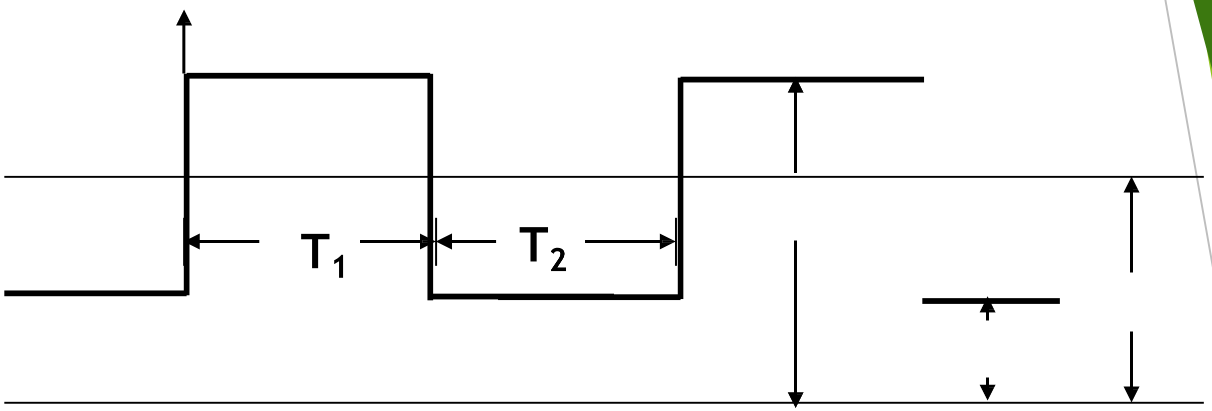


$0 \le t \le tp \quad V_i=V$

Otherwise $\quad V_i=0$

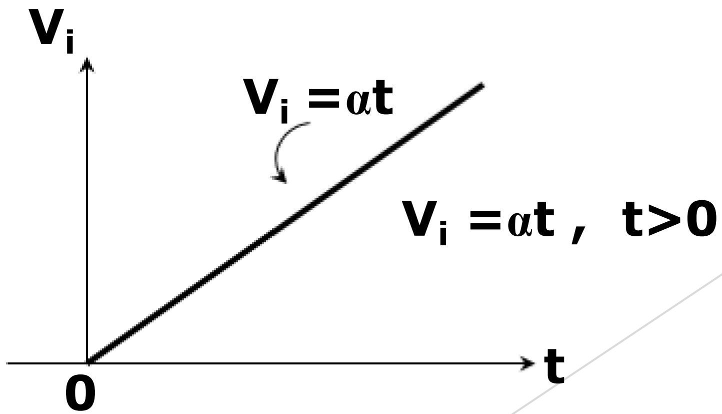
Square Wave

- A wave form which maintains itself at one constant level v^1 for a time T_1 and at other constant Level V^{11} for a time T_2 and which is repetitive with a period $T=T_1+T_2$ is called a square-wave.



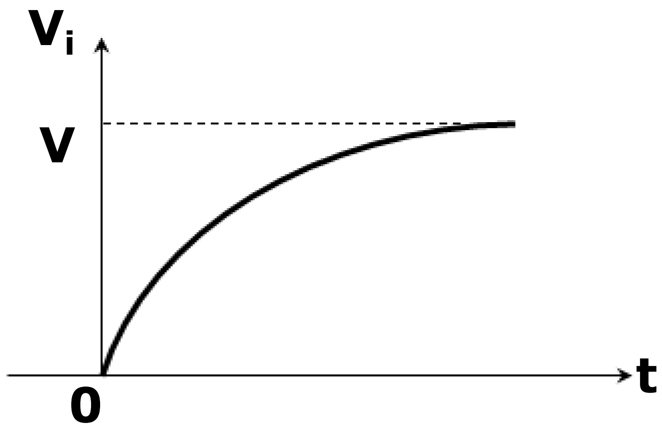
Ramp

A waveform which is zero for t<0 and which increases linearly with time for t>0.

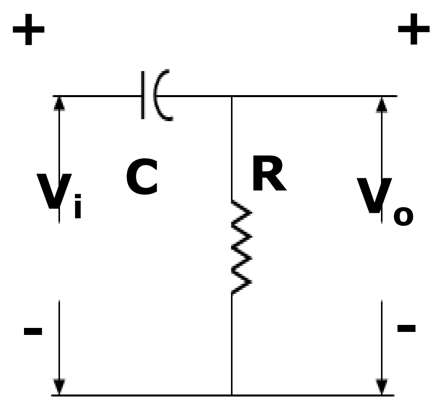


Exponential

- The exponential waveform input is given by where T is the time constant of the exponential input



High pass RC circuit



$$X_C = \frac{1}{2\pi f C}$$

If f=low, X_c becomes high

C act as open circuit, so the V_o=0.

If f=high, X_c becomes low

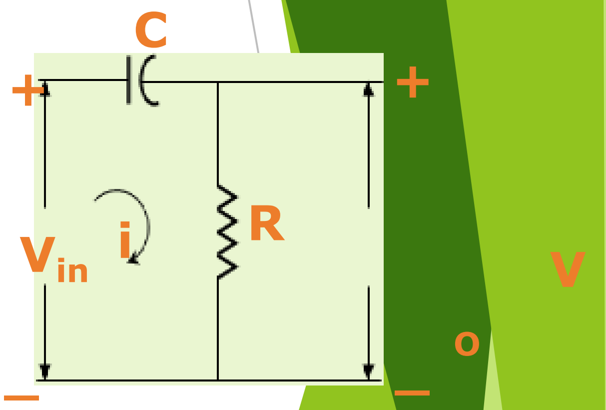
C acts as short circuit, so we get the output.

The higher frequency components in the input signal appear at the output with less attenuation due to this behavior the circuit is called "High Pass Filter".

Sinusoidal input

- For Sinusoidal input, the output increases in amplitude with increasing frequency.

$$V_o = iR$$



$$i = \frac{V_{in}}{R - jX_C} = \frac{V_{in}}{R - \frac{j}{2\pi f C}}$$

$$i = \frac{V_{in}}{R\left[1 - \frac{j}{2\pi f RC}\right]}$$

$$V_O = iR = \frac{V_{in} \times R}{R\left[1 - \frac{j}{2\pi f RC}\right]} = \frac{V_{in}}{1 - \frac{j}{2\pi f RC}}$$

$$V_o = \frac{V_{in}}{1 - j\frac{f_1}{f}} \quad \text{where } f_1 = \frac{1}{2\pi RC}$$

$$\frac{V_O}{V_{in}} = \frac{1}{1 + j\left(-\frac{f1}{f}\right)}$$

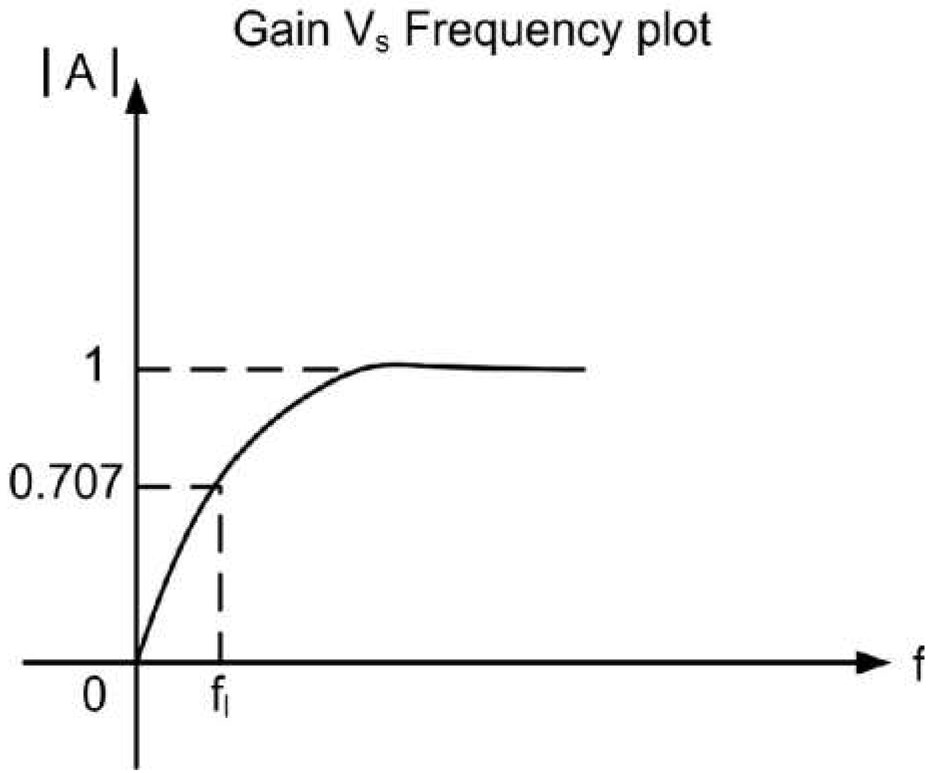
$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_1}{f}\right)^2}}$$

$$|A| = 0.707$$

$$\theta = -\tan^{-1}\left(\frac{-f_1}{f}\right) = \tan^{-1}\left(\frac{f_1}{f}\right)$$

At the frequency $f = f_1$

$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707$$



At $f = f_1$ the gain is 0.707 or this level corresponds to a signal reduction of 3 decibels(dB).

∴ f_1 is referred to as Lower 3-dB frequency.

Square wave input

- Percentage Tilt (Tilt) $\%$

Tilt is defined as the decay in the amplitude of the output voltage wave due to the input voltage maintaining constant level

$$P = \frac{V_1 - V^1{}_1}{V/2} X100$$

$$V_1' = V_1 . e^{-T_1/RC} \longrightarrow (1)$$

$$V_2' = V_2 . e^{-T_2/RC} \longrightarrow (2)$$

$$V_1' - V_2 = V \longrightarrow (3)$$

$$V_1 - V_2' = V \longrightarrow (4)$$

- A symmetrical square wave is one for which $T_1 = T_2 = T/2$ & because of symmetry $V_1 = -V_2$

By substituting these in above equation (3)

- $$V_1' = -V_2'$$

$$V = V_1' - V_2$$

$$V = V_1 . e^{-\frac{T}{2RC}} - V_2$$

$$V = V_1 . e^{-\frac{T}{2RC}} + V_1$$

$$V = V_1 (1 + e^{-\frac{T}{2RC}})$$

$$\boxed{V_1 = \frac{V}{1 + e^{-T/2RC}}} \longrightarrow \text{I}$$

Equation (1) $V_1' = V_1 . e^{-\frac{T}{2RC}}$

$$V_1' = \frac{V}{1 + e^{-T/2RC}} \times e^{-T/2RC} = \frac{V}{1 + e^{T/2RC}}$$

$$\boxed{V_1' = \frac{V}{1 + e^{T/2RC}}} \longrightarrow \text{II}$$

For $RC >> T/2$ the equation (I) & (II) becomes as

$$V_1 \cong \frac{V}{2}\left(1+\frac{T}{4RC}\right) \ \& \ V_1^1 \cong \frac{V}{2}\left(1-\frac{T}{4RC}\right)$$

The percentage tilt 'P' is defined by $P = \dfrac{V_1 - V_1^1}{V/2} \times 100$

$$P = \frac{\dfrac{V}{1+e^{-T/2RC}} - \dfrac{V}{1+e^{T/2RC}}}{V/2} \times 100$$

$$P = \left[\frac{1}{1+e^{-T/2RC}} - \frac{1}{1+e^{T/2RC}}\right] \times 200$$

$$P = \left[\frac{1}{1+e^{-T/2RC}} - \frac{e^{-T/2RC}}{1+e^{T/2RC}}\right] \times 200$$

$$P = \frac{1-e^{-T/2RC}}{1+e^{-T/2RC}} \times 200\%$$

High Pass RC circuit acts as differentiator:-

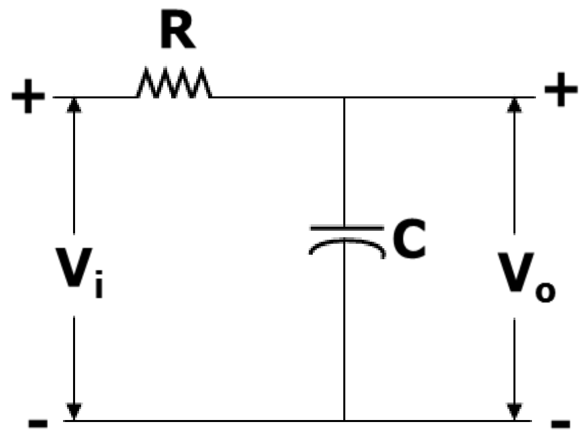
- The time constant of high pass RC circuit in very small in comparison within the time required for the input signal to make an appreciable change, the circuit is called a *"differentiator"*.
- Under this circumstances the voltage drop across R will be very small in comparison with the drop across C. Hence we may consider that the total input V_i appears across $\frac{dV_i}{dt}$ C, so that the current is determined entirely by the capacitance.
- Then the current is $i = C \frac{dV_i}{dt}$ and the output signal across R is

$$V_0 = iR$$

$$V_0 = RC$$

- hence the output is proportional to the derivative of the input.

Low Pass RC Circ



$$X_C = \frac{1}{2\Pi f C}$$

If f=low, X_c becomes high

C act as open circuit, so we get the output.

If f=high, X_c becomes low

C acts as short circuit, so V_o=0.

As the lower frequency signals appear at the output, it is called as "Low pass RC circuit".

Sinusoidal input

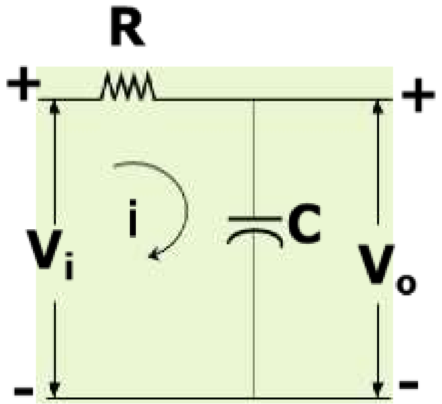
$$V_o = \frac{1}{CS} i$$

$$V_O = \frac{V_{in} \times \frac{X_C}{j}}{R + \frac{X_C}{j}}$$

where $X_C = \frac{1}{2\pi fC}$

$$V_O = \frac{V_{in} \times \frac{1}{j\,\omega C}}{R + \frac{1}{j\,\omega C}}$$

$$V_O = \frac{V_{in}}{j\omega RC + 1} = \frac{V_{in}}{1 + j2\pi fRC}$$



$$V_O = \frac{V_{in}}{1 + j\frac{f}{f_2}} \qquad \text{where} \quad f_2 = \frac{1}{2\pi RC}$$

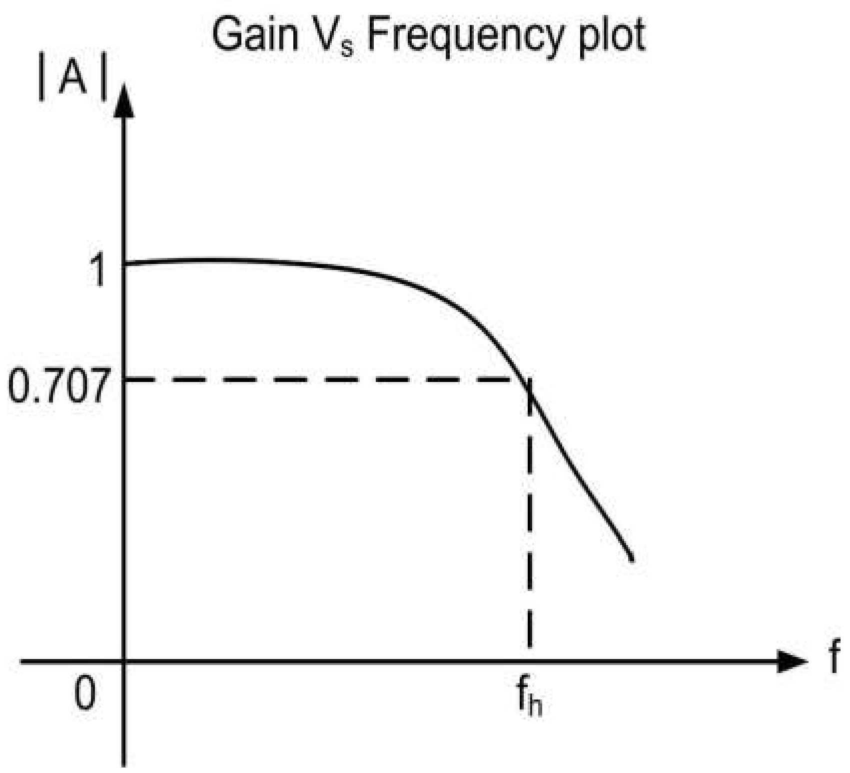
$$A = \frac{V_O}{V_{in}} = \frac{1}{1 + j\frac{f}{f_2}}$$

$$|A| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}} \qquad \text{and} \qquad \theta = -\tan^{-1}\left(\frac{f}{f_2}\right)$$

$$\text{At the frequency } f = f_2$$

$$\left|\frac{V_O}{V_{in}}\right| = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707$$

$$|A| = 0.707$$



At $f = f_2$ the gain is 0.707 or this level corresponds to a signal reduction of 3 decibels(dB).

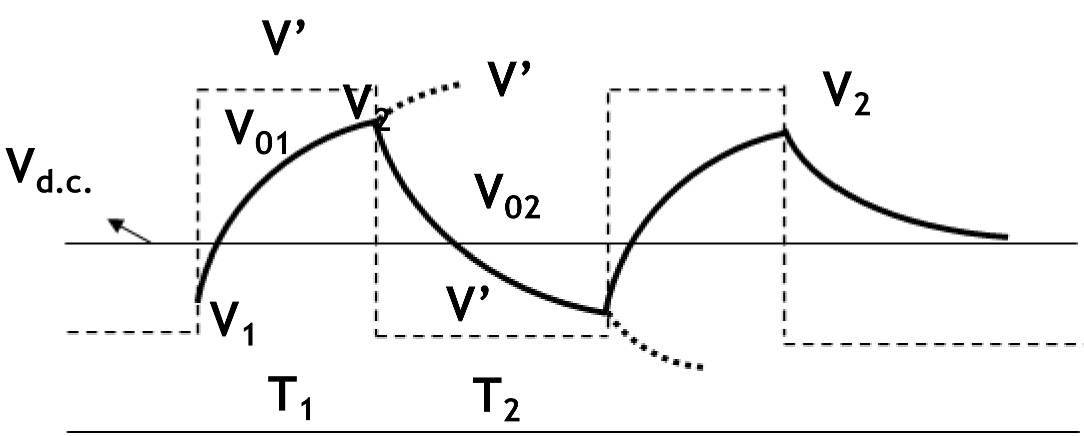
$\therefore$ f_2 or f_h is referred to as upper 3-dB frequency.

Square wave input

- Rise Time(t_r):

The time required for the voltage to rise from 10 % to 90 % of the final steady value is called "Rise Time".

$$t_r = 2.2RC$$



$$\Rightarrow V_O = V_f + (V_i - V_f)\, e^{\frac{-t}{RC}}$$

The output voltage V_{01} & V_{02} is given by

$$V_{01} = V^{1} + (V1 - V^{1})\,.\, e^{-T_1/RC} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ (1)$$

$$V_{02} = V^{11} + (V2 - V^{11})\,.\, e^{-T_2/RC} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ (2)$$

if we set $V_{01} = V_2$ at $t=T_1$

and $V_{02} = V_1$ at $t= T_1+T_2$

$$V_2 = V^{1} + (V1 - V^{1})\, e^{-T_1/RC}$$

$$V_1 = V^{11} + (V2 - V^{11})\, e^{-T_2/RC}$$

Since the average across R is zero then the d.c voltage at the output is same as that of the input. This average value is indicated as Vd.c.

Consider a symmetrical square wave with zero average value, so that

$$T_1 = T_2 = T/2$$

$$V^1 = -V^{11} = V/2 \quad \& \quad V_1 = -V_2$$

$$V_2 = \frac{V}{2} + \left(-V_2 - \frac{V}{2}\right) e^{-\frac{T}{2RC}}$$

$$V_2 = \left[1 + e^{-\frac{T}{2RC}}\right] = \frac{V}{2}\left[1 - e^{-\frac{T}{2RC}}\right]$$

$$V = \frac{V}{2}\left[\frac{1 - e^{-T/2RC}}{1 + e^{-T/2RC}}\right]$$

$$V_2 = \frac{V}{2}\left[\frac{e^{T/2RC} - 1}{e^{T/2RC} + 1}\right]$$

$$V_2 = \frac{V}{2} \cdot \frac{e^{2x} - 1}{e^{2x} + 1} \quad \text{where} \quad x = \frac{T}{4RC}$$

$$\boxed{V_2 = \frac{V}{2} \tanh x}$$

Low pass RC circuit acts as an integrator

- The time constant is very large in comparison with the time required for the input signal to make an appreciable change, the circuit is called an "Integrator".
- As RC>>T the voltage drop across C will be very small in comparison to the voltage drop across R and we may consider that the total input V_i appear and across R, then

$$V_i = iR$$

$$i = \frac{V_i}{R}$$

For low pass RC circuit the output voltage V_o is given by

$$V_O = \frac{1}{C}\int i\,dt$$

$$V_O = \frac{1}{C}\int \frac{V_i}{R}\,dt$$

$$V_O = \frac{1}{RC}\int V_i\,dt$$

Advantages of Integrator over differenti

- Integrators are almost invariably preferred over differentiators in analog computer applications for the following reasons.
- The gain of the integrator decreases with frequency where as the gain of the differentiator increases linearly with frequency. It is easier to stabilize the former than the latter with respect to spurious oscillations.
- As a result of its limited band width an integrator is less sensitive to noise voltages than a differentiator.
- If the input wave form changes very rapidly, the amplifier of a differentiator may over load.
- It is more convenient to introduce initial conditions in an integrator.

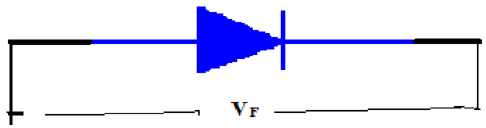
UNIT-V:
Switching Characteristics of Devices

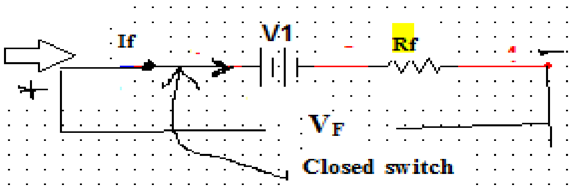
SWITCHING CHARACTERISTICS OF DEVICE

- **DIODE AS A SWITCH**
- The diode readily conducts when forward-biased and the bias voltage is greater than the cut-in voltage.
- There is no conduction through the device ,when it is reverse biased.
- The forward resistance of an ideal diode is zero, and the reverse resistance is infinitely large.
- A diode conducts when forward-biased and blocks conduction when reverse-biased, it can function as an electronic switch.
- When it is conducting , it is ON, and when it is not conducting it is OFF.

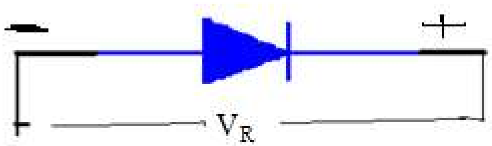
Diode as a Switch

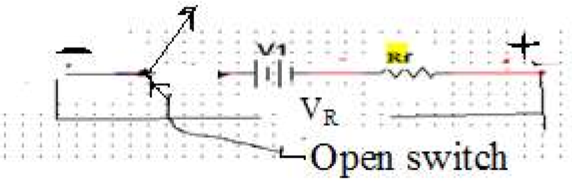
- If a forward bias voltage Vf >V1 is applied the diode readily conducts and a forward current If flows.   V1=Barrier potential
- Hence a forward-biased diode acts as a switch.



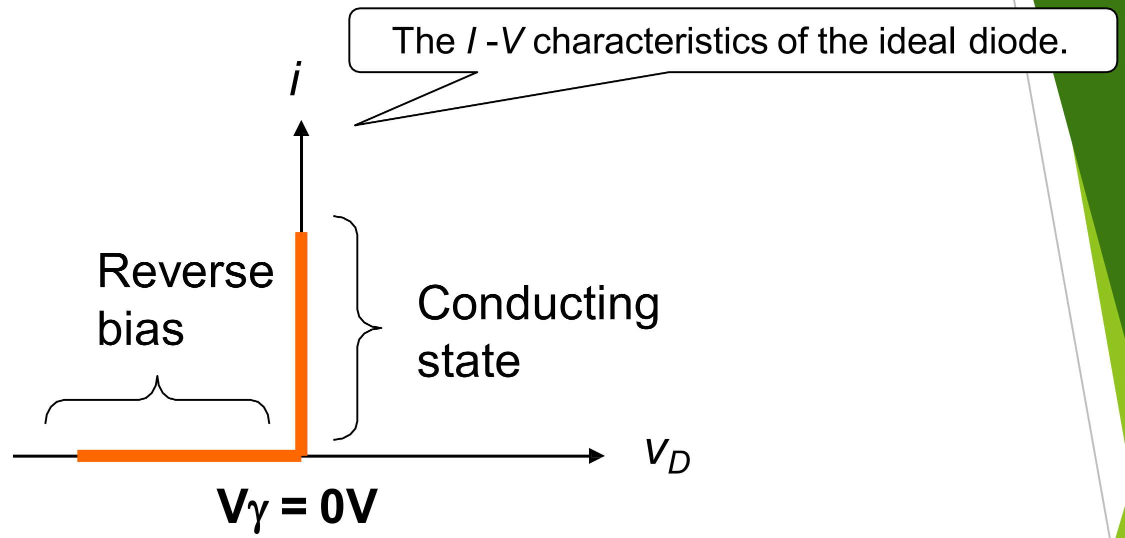


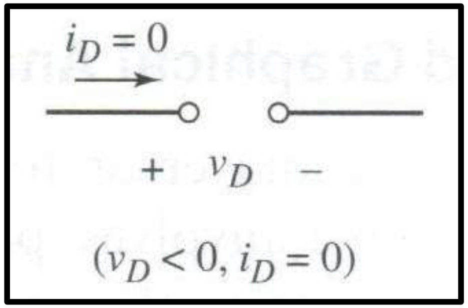
- When the reverse bias is applied to the diode, diode does not conduct.
- Hence the reverse biased diode analogous to open switch



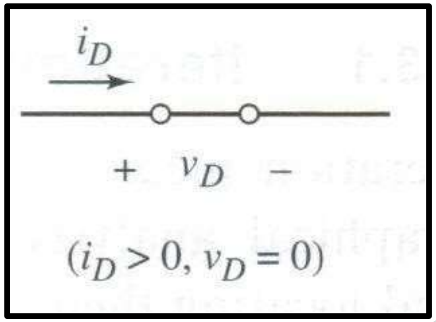


CIRCUIT REPRESENTATION OF DIODE





Reverse biased open circuit



Conducting state short circuit

Ideal diode Model

Useful for circuits with more than one diode

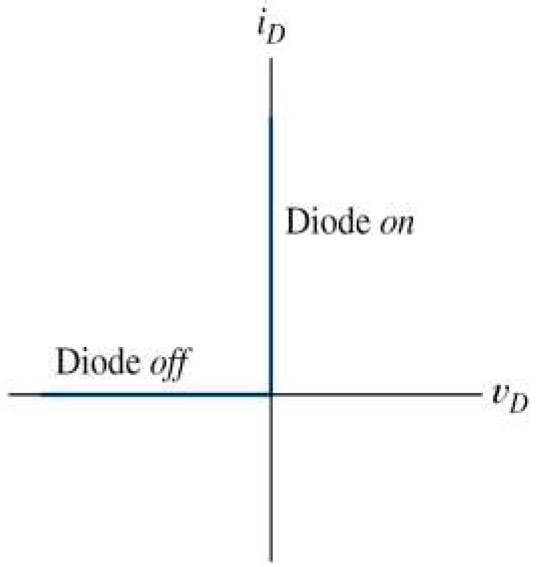


Figure 10.15 Ideal-diode volt–ampere characteristic.

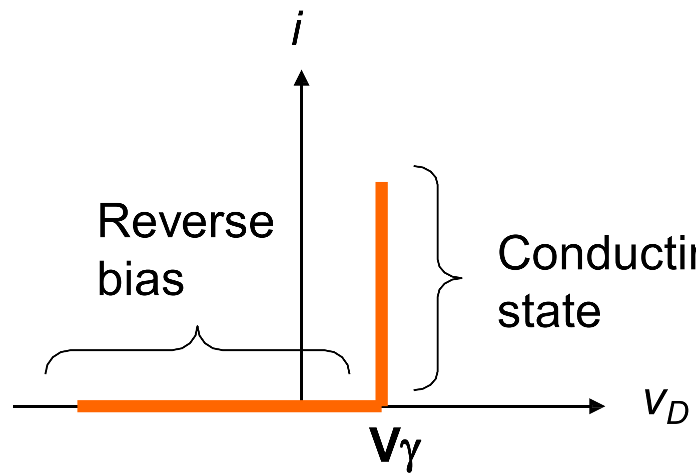
(1) Assume a state for each diode, either "on" or "off" -2^n combinations

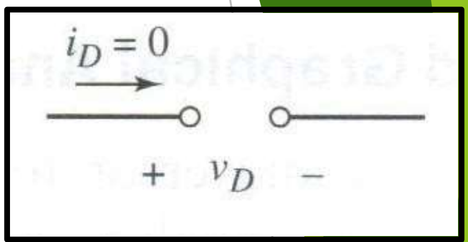
(2) Assume a short circuit for diode "on" and an open circuit for diode "off"

(3) Check to see if the result is consistent with the assumed state for each diode (current must flow in the forward direction for diode "on" and the voltage across the diodes assumed to be "off" must be positive at the cathode – reverse bias)

(4) If the results are consistent with the assumed states, the analysis is finished. Otherwise return to step (1) and choose a different combination of diode states.

CIRCUIT REPRESENTATION OF DIODE – Piecewise Linear Model

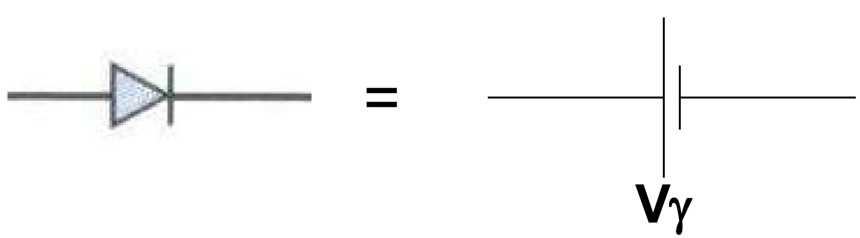




Reverse biased open circuit

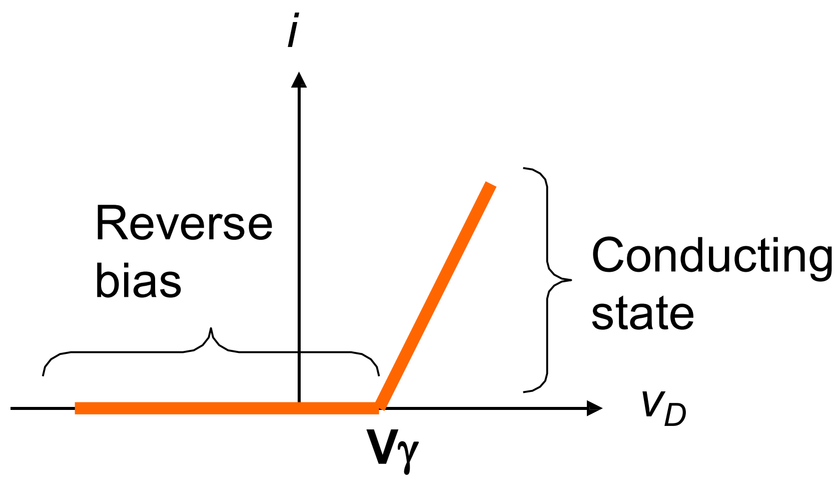
V_D = $V\gamma$ for diode to turn on.

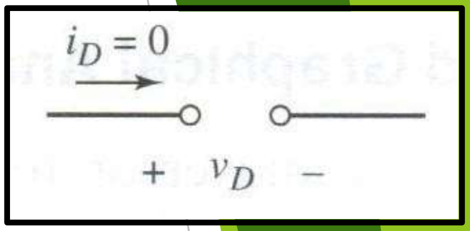
Hence during <u>conducting state:</u>



Represented as a battery of voltage = **$V\gamma$**

CIRCUIT REPRESENTATION OF DIODE – Piecewise Linear Model

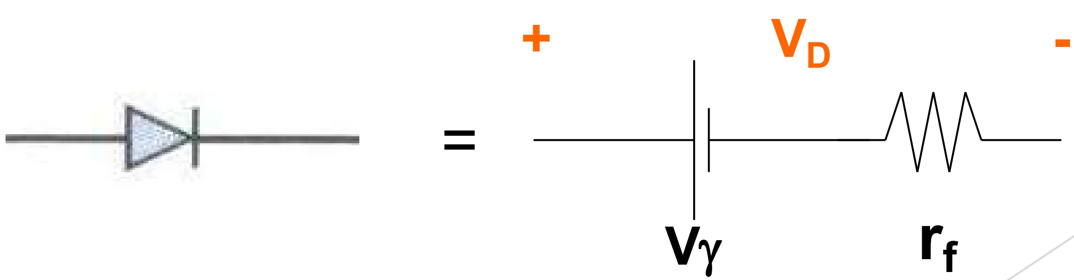




Reverse biased open circuit

$V_D \geq V\gamma$ for diode to turn on.

Hence during <u>conducting state:</u>

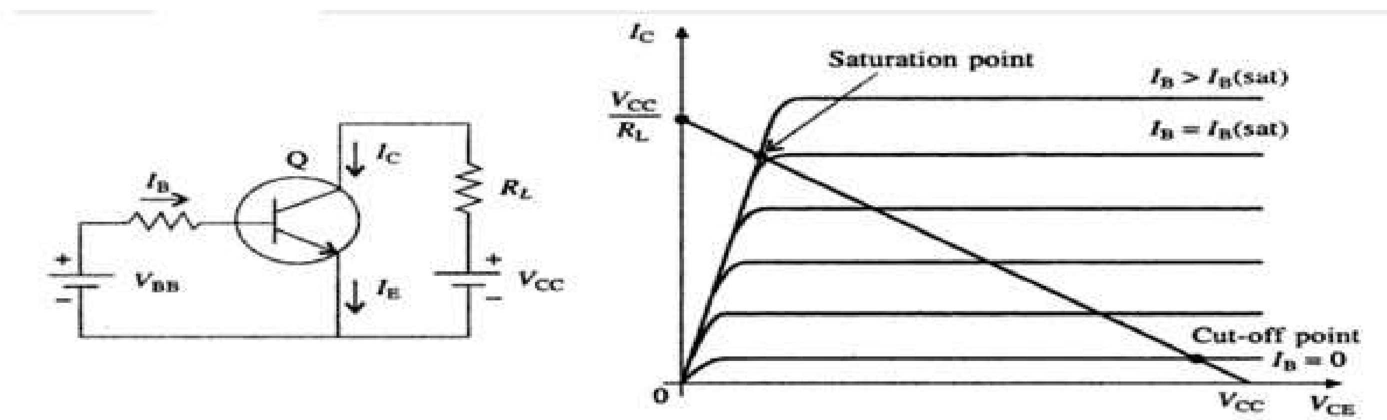


Represented as a battery of voltage = **Vγ** and forward resistance, **r_f** in series

Transistor as a switch

- A transistor can be used as a switch.
- It has three regions of operation
- When both EB junction and CB junction are reverse biased, the transistor operates in the cut-off region.
- When the EB junction is forward biased and CB junction is reverse biased , it operates in the active region and acts as an amplifier.
- When both the EB junction and CB junctions are forward biased it operates in the saturation region and acts as a closed switch.
- When Q is saturated it is like a closed switch from C to E.

- When Q is cut-off it is like an open switch from C to E.
- $I_c = V_{cc} - V_{CE} / R_L$ and $V_{BB} - V_{BE} / R_B$
- Referring to the output characteristics , the region below the I b = 0 curve is the cut-off region.
- The intersection of the load line with Ib = 0 curve is the cut-off point.

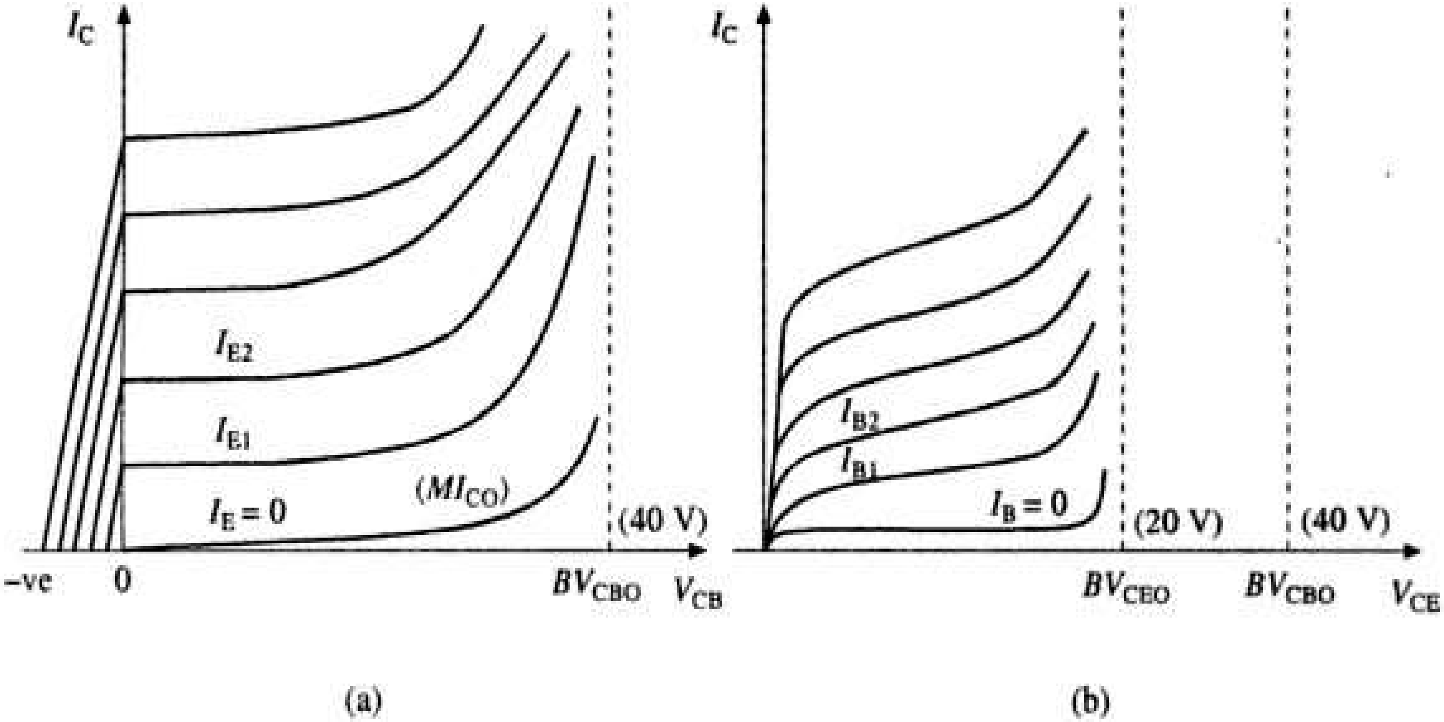


- The intersection of the load line with the Ib(sat) curve is called the saturation point.   Ib =
- At this point the base current is Ib(sat) and the collector current is maximum.
- $Ic(sat) = Vcc/R_L$
- Ib(sat) represents the minimum base current required to bring the transistor into saturation.
- For 0<Ib<Ib(sat), the transistor operates in the active region.
- If the base current is greater than Ib(sat),
- Ic ≈≈Vcc/Rc and transistor appears like a closed switch.

Breakdown voltage of a Transistor

- The maximum reverse biasing voltage which may be applied before breakdown between the collector and base terminal of the transistor(BVCBO)i.e the emitter lead be open circuited.
- The breakdown occurs because of the avalanche multiplication of the current Ico that crosses the collector junction.
- As the multiplication the current becomes Mico.
- $M = 1/1-(V_{CB} / BV_{CBO})^n$ M = Multiplication factor
- The parameter n lies in the range 2 to 10.
- Below Fig. shows the CB characteristics in the breakdown region. The curve for Ie =0 is function of Vcb.Ic has magnitude $M\acute{\alpha} I_E$.

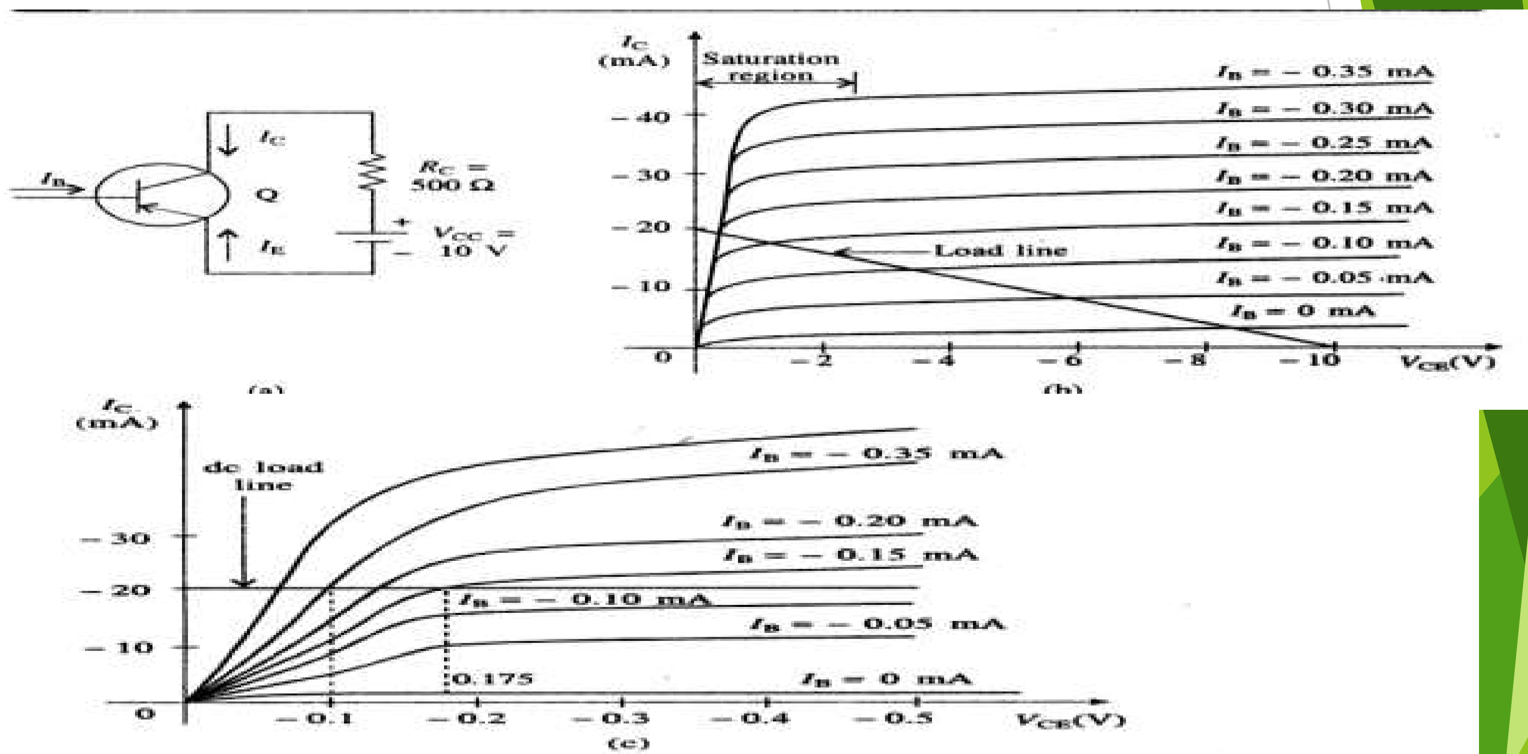
Breakdown voltage of a transistor



(a) CB characteristics extended into the breakdown region and (b) idealized CE characteristics extended into the breakdown region.

The transistor switch in saturation

- In the fast switching circuits, R_L must be kept small.
- In saturation the transistor current is normally Vcc/ R_L.
- The total voltage swing at the transistor switch is Vcc-Vce(sat).

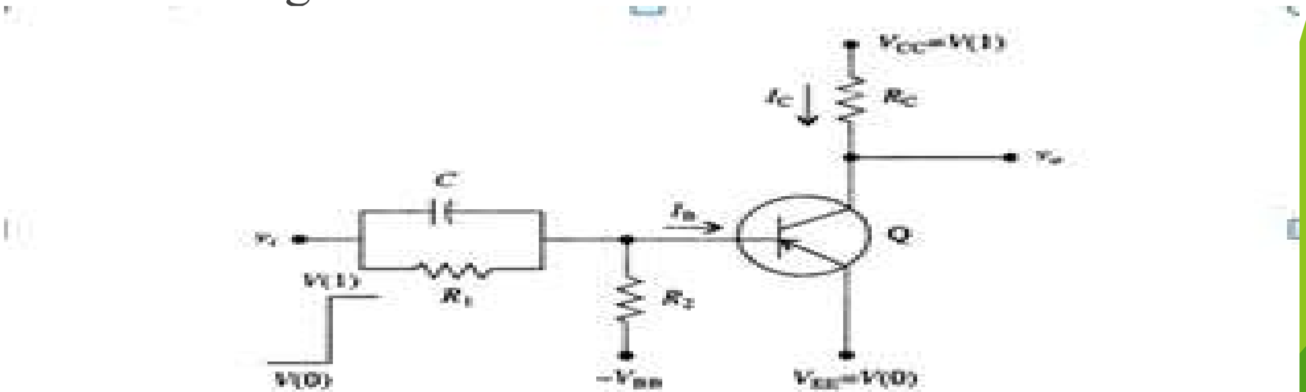


(a) Transistor circuit as a switch, (b) CE characteristics using Ge diode, and (c) expanded saturation region CE characteristics of the transistor.

- At Ib = -0.15mA the transistor is in saturation and Vce=-175mv
- At Ib = -0.35mA Vce has dropped to 100mv
- For a transistor operating in the saturation region a quantity of interest is the ratio Vce(sat)/Ic. This parameter is called the common emitter saturation resistance, Rce(sat).
- The saturation voltage Vce(sat) depends not only on the operating point but also on the semiconductor material.
- In the saturation region hfe is a useful parameter and is supplied by the manufacturer.
- Once we know Ic(Vcc/R_L) and hfe, the amount of base current Ib = Ic/hfe needed to saturate the transistor can be found.

Design of Transistor switch

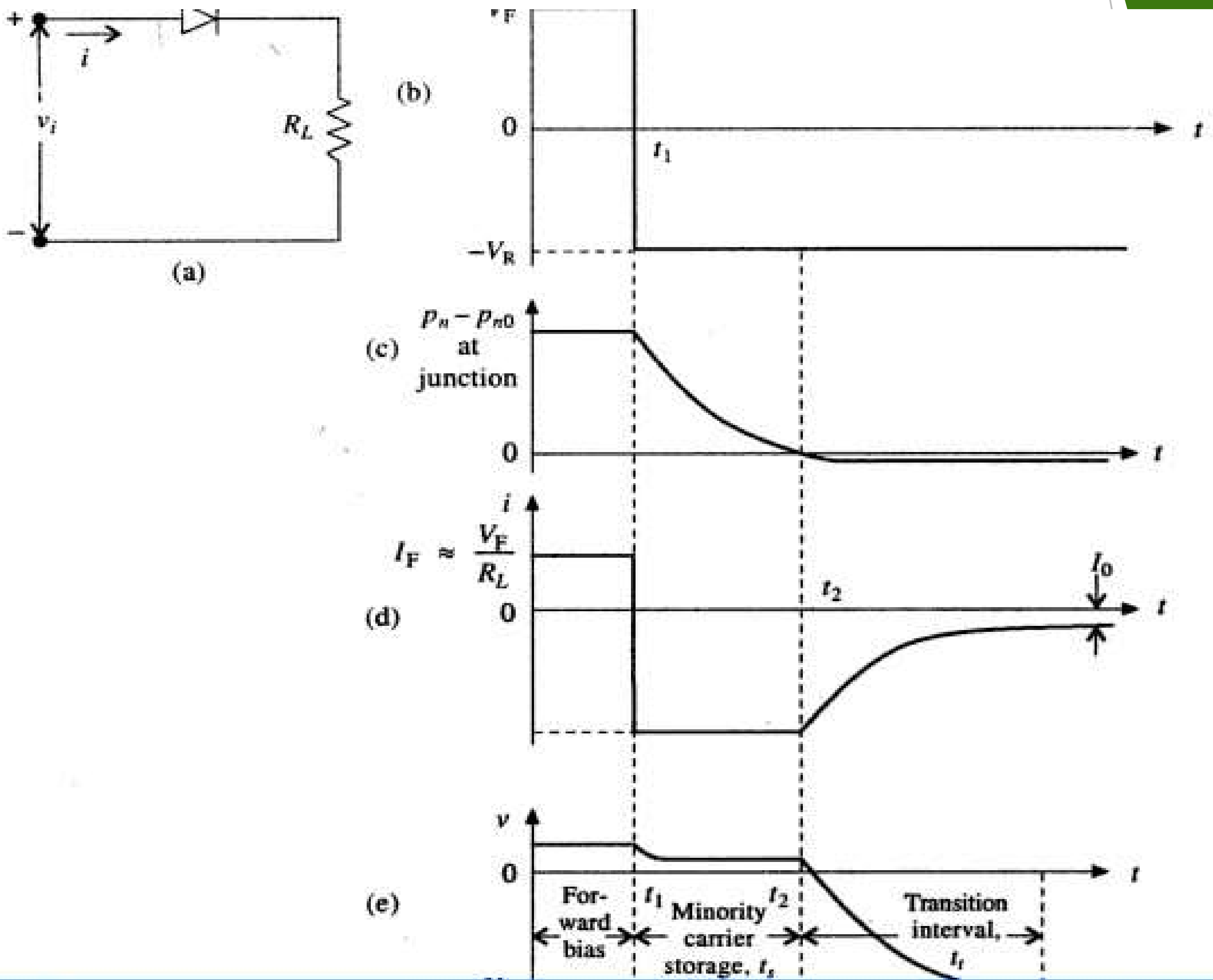
- The transistor that acts as a switch is driven between cut-off and saturation.
- For low input vi =0 the transistor is kept at cut-off, so the output is Vcc or 1.
- For high input , the transistor is driven into saturation. So the output i.e Vce(sat) = 0. Thus the transistor acts as a switch.
- To improve the transient response of the inverter the capacitor C is used across the resistor R1.
- This helps in removing minority carrier charges in the base when the signal changes between logic states.



Transistor as a switch.

- Design: when vi=0 the open circuit base voltage is
- Vb=-Vbb (R1/R1+R2). This voltage should be less than Vbe(cut-off).
- When vi=1, the transistor is in saturation.
- Ic=(Vcc-Vce(sat))/Rc and Ib(min) = Ic/hfe(min)
- The current through the resistance R1 is I1=(V(1)-Vbe(sat))/R1
- The current throhgh the resistor R2 is I2=[Vbe(sat)-(-Vbb)]/R2
- Ib = I1-I2
- This current Ib must be equal to Ic/hfe =Vcc-Vce(sat)/Rc.hfe
- Rc = [Vcc-Vce(sat)]/Ic
- Assuming the values of Vbe(sat) and Vce(sat).
- Select R1 and R2 such that I1-I2 = Ib

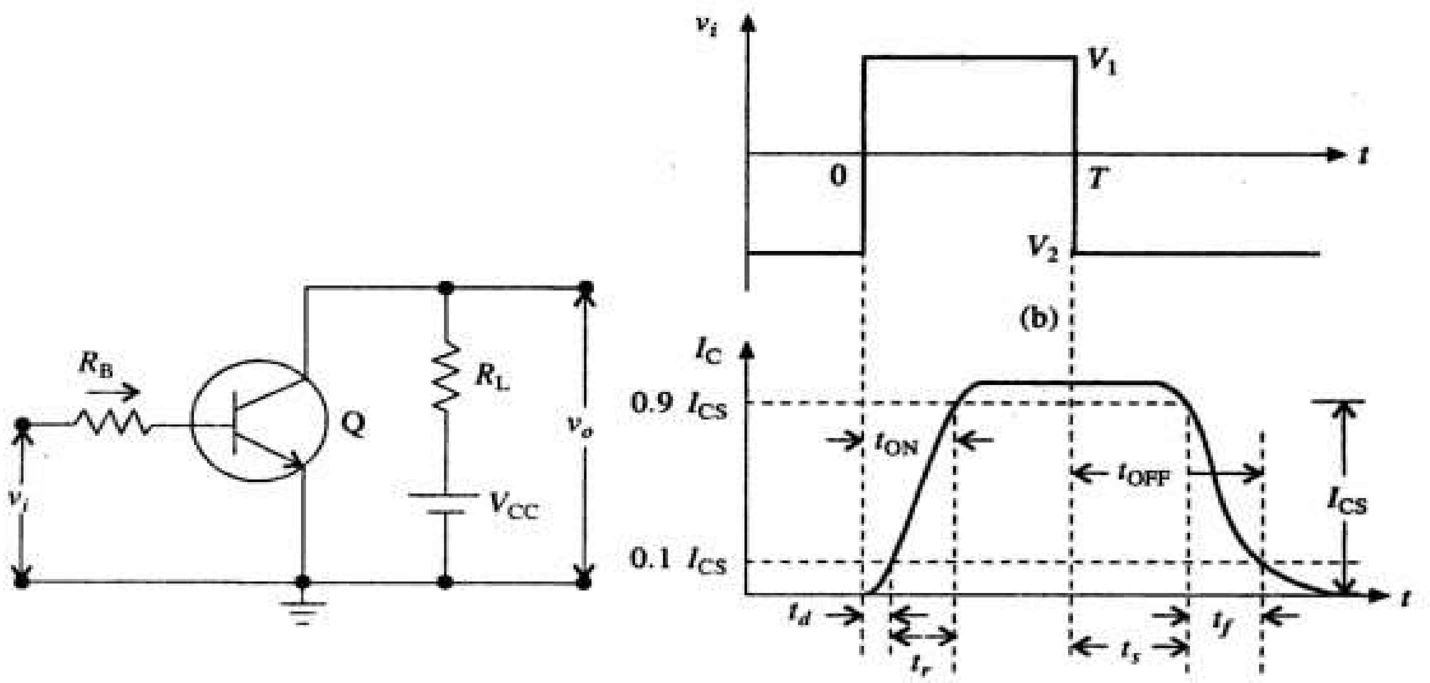
Diode switching Times



- Above Fig. shows the switching times of a diode
- Up to t = t1 vi=vf, the resistance RL is assumed large so that the drop across RL is large compared with the voltage across the diode. i=vf/RL
- At the time t=t1 ,the input voltage reverses abruptly to the value vi = -VR, the current reverses I = -VR/RL = -IR
- **Storage time**: the interval from t1 to t2 for the minority charge to become zero is called the storage time ts.
- **Transition time** : the time which elapses between t2 and the time when the diode has nominally recovered is called the transition time $t_{t.}$
- **Reverse recovery time : ts + $t_{t.}$**

Transistor switching Times

- When the transistor acts as a switch , it is either in cut-off or in saturation.
- To consider the behavior of the transistor as it makes transition from one state to the other.



- The pulse waveform makes the transitions between the voltage levels V2 and V1. At V2 the transistor is at cut-off and at V1 the transistor is in saturation.
- The input waveform vi is applied between the base and the emitter through a resistor R_B.
- The collector current does not immediately respond to the input signal.
- **Delay time(td)** : The interval of time between the application of the base current and the commencement of collector current is termed as delay time(td)
- **Rise time(tr)** : The time required for the collector current to rise from 10% to 90% of the maximum level.
- **Turn-on time** $t_{ON} = td + tr$

- **Storage time(ts)** : There is a time lag between the instant Ib =0 and the instant at which Ic begins to decrease. This interval is termed as storage time.
- **Fall time(t_f)** : The time required to fall from 90% to 10% of maximum value is termed as fall tome.
- **Turn-off time $t_{OFF} = ts + t_f$**
- **Decay time** : The collector current falls from 10% to level of Icbo. It is very small.