Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC507

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-I

B.Tech VIII Semester End Examinations, May - 2020

Regulations: R16

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

(ECE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1.	a)	Compute the linear convolution of finite duration sequences h (n) = {1, 2} and x(n) = {1, 2, -1, 2,3, -2, -3, -1,1,1,2,-1} by overlap add method	**[7M]**
	b)	Calculate the dynamic range and precision of each of the following number representation formats a) 48 bit double precision fixed point format b) a floating point format with a 16 bit mantissa and a 8 bit exponent	**[7M]**
2.	a)	Explain about A/D conversion errors in a DSP system and derive expressions for mean, variance and SNR?	**[7M]**
	b)	Consider the N-point sequence x(n) defined for n= 0,...,N−1. Show that if x(n) is real, then the N-point DFTX(k) satisfies X(N−k) =X(k), k= 0,...,N−1,(1)where the over line notation denotes the complex conjugate	**[7M]**

UNIT – II

3.	a)	Consider a MAC unit whose inputs are 16 bit numbers. If 256 products are to be summed up in this MAC, how many guard bits should be provided for the accumulator to prevent overflow condition from occurring?	**[7M]**
	b)	Explain in detail about the on chip peripherals and processor benchmarking	**[7M]**
4.	a)	If a sum of 256 products is to be computed using a pipelined MAC unit, and if the MAC execution time of the unit is 100nsec, what will be the total time required to complete the operation?	**[7M]**
	b)	Explain the assembly instructions memory addressing of VLIW processor with examples	**[7M]**

UNIT – III

5.	a)	Write a sequence of TMS320C54xx instructions to configure a circular buffer with a start address at 0200h and an end address at 021fh with current buffer pointer (AR6) pointing to address 0205h.	**[7M]**
	b)	Illustrate the concept of Internal memory and memory mapped Registers of the TMS320C54XX Processor	**[7M]**
6.	a)	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h	**[7M]**

b) Describe the following on-chip peripherals of TMS320C54xx processors **[7M]**
(a) Hardware Timer (b) Host port interface

UNIT – IV

7. a) Design an interface to connect a 64K x 16 flash memory to a TMS320C54XX processor. The processor address bus to be used is A0-A15 **[7M]**

b) Design a circuit to interface 4K x 16 and a 2K x 16 memory chip to realize program memory space for the TMS320C54xx processor in the address Ranges 03F000h-03FFFFh and 05F800h-05FFFFh, respectively. **[7M]**

8. a) Is it possible to connect a memory device without Decode (interfacing) Circuit? If so, connect 8k x 16 SRAM to TMS320C54xx. What are the merits & demerits of the solution? **[7M]**

b) Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved? **[7M]**

UNIT – V

9. a) Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations? **[7M]**

b) Write a pseudo code to determine 8 point DFT using DIT-FFT algorithm invoking butterfly
subroutine in a nested loop for each stage? **[7M]**

10. a) Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT **[7M]**

b) Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required. **[7M]**

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COURSE OBJECTIVES:

The course should enable the students to:

I	Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors.
II	Learn the architectural differences between DSP and General purpose processor.
III	Learn about interfacing of serial & parallel communication devices to the processor.
IV	Implement the DSP & FFT algorithms.

COURSE OUTCOMES (COs):

CO 1	Understand the basics of Digital Signal Processing and transforms.
CO 2	Able to distinguish between the architectural features of General purpose processors and DSP processors.
CO 3	Understand the architectures of TMS320C54xx devices and Acquire knowledge about various addressing modes of DSP TMS320C54XX.
CO 4	Discuss about various memory and parallel I/O interfaces.
CO 5	Design and implement basic DSP algorithms.

COURSE LEARNING OUTCOMES (CLOs):

AEC507.01	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.
AEC507.02	Understand the inter-relationship between DFT and various transforms.
AEC507.03	Understand the IEEE-754 floating point and source of errors in DSP implementations.
AEC507.04	Understand the fast computation of DFT and appreciate the FFT Processing.
AEC507.05	Understand the concept of multiplier and multiplier Accumulator.
AEC507.06	Design SMID ,VLIW architectures.
AEC507.07	Understand the modified bus structures and memory access in PDSPs.
AEC507.08	Understand the special addressing modes in PDSPs.
AEC507.09	Understand the architecture of TMS320C54XX DSPs.
AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.
AEC507.11	Understand the various interrupts and pipeline operation of TMS320C54XX processors.
AEC507.12	Analyze the Program control, instruction set and programming.
AEC507.13	Understand the concept of on-chip Peripherals.
AEC507.14	Understand the significance of memory space organization.

AEC507.15	Analyze external bus interfacing signals.
AEC507.16	Explain about parallel I/O interface, programmed I/O.
AEC507.17	Understand the significance of Interrupts and Direct Memory Access.
AEC507.18	Understand the basic concepts of convolution and correlation.
AEC507.19	Compare the characteristics of IIR and FIR filters.
AEC507.20	Analyze the concepts of interpolation and decimation filters.

MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES

SEE Question No		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC507.01	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.	CO 1	Remember
	b	AEC507.02	Understand the inter-relationship between DFT and various transforms.	CO 1	Understand
2	a	AEC507.03	Understand the IEEE-754 floating point and source of errors in DSP implementations.	CO 1	Apply
	b	AEC507.04	Understand the fast computation of DFT and appreciate the FFT Processing.	CO 1	Understand
3	a	AEC507.05	Understand the concept of multiplier and multiplier Accumulator.	CO 2	Remember
	b	AEC507.06	Design SMID ,VLIW architectures.	CO 2	Apply
4	a	AEC507.07	Understand the modified bus structures and memory access in PDSPs.	CO 2	Remember
	b	AEC507.08	Understand the special addressing modes in PDSPs.	CO 2	Understand
5	a	AEC507.09	Understand the architecture of TMS320C54XX DSPs.	CO 3	Apply
	b	AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.	CO 3	Remember
6	a	AEC507.09	Understand the architecture of TMS320C54XX DSPs.	CO 3	Apply
	b	AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.	CO 3	Remember
7	a	AEC507.16	Explain about parallel I/O interface, programmed I/O.	CO 4	Understand
	b	AEC507.17	Understand the significance of Interrupts and Direct Memory Access.	CO 4	Understand
8	a	AEC507.16	Explain about parallel I/O interface, programmed I/O.	CO 4	Remember
	b	AEC507.17	Understand the significance of Interrupts and Direct Memory Access.	CO 4	Understand
9	a	AEC507.19	Compare the characteristics of IIR and FIR filters.	CO 5	Understand
	b	AEC507.20	Analyze the concepts of interpolation and decimation filters.	CO 5	Remember
10	a	AEC507.19	Compare the characteristics of IIR and FIR filters.	CO 5	Understand
	b	AEC507.20	Analyze the concepts of interpolation and decimation filters.	CO 5	Remember

Signature of Course Coordinator **HOD, ECE**