Hall Ticket No | | | | | | | | | | |

Question Paper Code: AECB05

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER - I

B.Tech III Semester End Examinations, November – 2019

Regulations: R18

DIGITAL ELECTRONICS

(EEE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each MODULE
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. a) Perform the subtraction operation using 1's complement of the subtrahend **[7M]**
   i. $(3C)_{16} - (4E)_{16}$
   ii. $(C5)_8 - (6A)_8$
   b) Write about binary logic in detail and explain binary Division and binary subtraction with examples. **[7M]**

2. a) Convert the following to the designated bases **[7M]**
   a. $(1000)_2$ to ( ) gray
   b. $(67.64)_{10}$ to $(\ )_{16}$
   c. $(321F)_8$ to $(\ )_{16}$
   b) Illustrate the process of detecting errors during the transmission of information from one location to another using parity bits. **[7M]**

MODULE – II

3. a) Write the truth table for Consensus theorem by taking an example **[7M]**
   b) What is Radix complement? Explain the procedure of complementing r of an n-digit number N in base r. **[7M]**

4. a) Explain the working of multiplexer with the help truth table and logic diagram. **[7M]**
   b) Enumerate the implementation of full-adder using two half-adders and an OR gate, for the following boolean expressions: **[7M]**

$$S = x'y'z' + x'yz' + xy'z' + xyz$$

$$C = x'y + xz' + yz$$

MODULE– III

5. a) Explain the design procedure for 5-bit binary counter using jk-flip-floP. **[7M]**
   b) Design a MOD-5 synchronous counter using flip flops and Implement it? Also draw the timing diagram? **[7M]**

6. a) Design a Ripple counter using T Flip Flops. **[7M]**
   b) Explain the process of construction and characteristic table of RS flip-flop using NAND gates. **[7M]**

MODULE– IV

7. a) Explain the following types of Analog to digital converters with suitable circuit diagrams. **[7M]**
   (i) Successive approximation
   (ii) Flash type
   b) Draw the circuit diagram for flash type DAC and explain in detail. **[7M]**

8. a) Explain the types of digital to analog converters with suitable circuit diagrams for Binary Weighted Resistor DAC. **[7M]**
   b) With a neat block diagram explain in detail about Dual slope type analog to digital converter. **[7M]**

MODULE – V

9. a) Using PLA, realize the following expressions **[7M]**

   $F1\ (a, b, c) = \sum m\ (0,1,5\ 7)$

   $F2\ (a, b, c) = \sum m\ (0, 1, 2, 6, 4)$

   b) Implement the circuit with a PAL **[7M]**

   $F1\ (a, b, c) = \sum m\ (0, 1, 3, 4)$

   $F2\ (a, b, c) = \sum m\ (1, 2, 3, 4,5)$

10. a) Design a BCD to excess-3 code converter and implement using suitable PAL. **[7M]**
    b) Implement the Combinational circuit defined by the function with a ROM.

    $F1\ (a,b,c,d) = \sum m\ (2,10,12,13)$ **[7M]**

    $F2(a,b,c,d) = \sum m\ (8,9,10,11,1,13,14,15)$

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COURSE OBJECTIVES:

I	Familiarize the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra.
II	Analyze Combination logic circuit and sequential logic circuits such as multiplexers, adders, decoders flip flops and latches.
III	Understand about synchronous and asynchronous sequential logic circuits.
IV	Analyze and design analog to digital and digital to analog Converters.
V	Impart the basic understanding of memory organization, ROM, RAM, CPLD, FPGA, and CCD.

COURSE OUTCOMES (COs):

CO 1	Understand the basic concept of number systems and integrated circuits
CO 2	Analyze Combination logic circuit such as multiplexers, adders, decoders
CO 3	Understand about synchronous and asynchronous sequential logic circuits.
CO 4	Analyze analog to digital and digital to analog Converters.
CO 5	Understanding of memory organization, ROM, RAM, CPLD, FPGA, and CCD.

COURSE LEARNING OUTCOMES (CLOs):

AECB03.01	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.
AECB03.02	Explain 2's complement representation and implement binary subtraction using 1's and 2's complements.
AECB03.03	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.
AECB03.04	Design TTL/CMOS integrated circuits and study the TTL and CMOS logic families.
AECB03.05	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method
AECB03.06	Design Gate level minimization using KMaps and realize the Boolean function using logic gates.
AECB03.07	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.
AECB03.08	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit.
AECB03.09	Discuss about MSI chip, ALU design.
AECB03.10	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops
AECB03.11	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
AECB03.12	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers

AECB03.13	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB03.14	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB03.15	Understand the classifications, characteristics and need of data converters such as ADC and DAC.
AECB03.16	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC
AECB03.17	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters, Dual slope converter.
AECB03.18	Implement the A/D converter using voltage to frequency and voltage to time conversion, specifications of A/D converters
AECB03.19	Understand the concept of memory organization, Read only memory and random access memory.
AECB03.20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.
AECB03.21	Analyze the concepts of CAM, FPGA.

MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES

SEE Question No		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AECB03.01	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.	CO 1	Understand
	b	AECB03.01	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.	CO 1	Understand
2	a	AECB03.01	Understand the basic concept of number systems, Binary addition and subtraction for digital systems.	CO 1	Understand
	b	AECB03.03	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.	CO 1	Understand
3	a	AECB03.03	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.	CO 2	Understand
	b	AECB03.03	Discuss about digital logic gates, error detecting and Correcting codes for digital systems.	CO 2	Remember
4	a	AECB03.06	Design Gate level minimization using KMaps and realize the Boolean function using logic gates.	CO 2	Understand
	b	AECB03.08	Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit	CO 2	Understand
5	a	AECB03.10	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops	CO 3	Understand
	b	AECB03.13	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops	CO 3	Understand
6	a	AECB03.10	Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops	CO 3	Understand
	b	AECB03.13	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops	CO 3	Understand
7	a	AECB03.16	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC	CO 4	Understand
	b	AECB03.17	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters, Dual slope converter.	CO 4	Understand
8	a	AECB03.16	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC	CO 4	Understand
	b	AECB03.17	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters, Dual slope converter.	CO 4	Understand

9	a	AECB03.19	Understand the concept of memory organization, Read only memory and random access memory.	CO 5	Understand
	b	AECB03.20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	CO 5	Understand
10	a	AECB03.20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	CO 5	Understand
	b	AECB03.20	Discuss and implement combinational and sequential logic circuits using PLA and PLDs.	CO 5	Understand

Signature of Course Coordinator **HOD, ECE**