Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC010

INSTITUTE OF AERONAUTICALENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER - I

III B.Tech V Semester End Examinations, December - 2018

Regulation: IARE-R16

COMPUTER ORGANIZATION

(Electronics and Communication Engineering)

Time:3Hours **Max Marks:70**

Answer any ONE question from each Unit
All questions carry equal marks
All parts of the question must be answered in one place only

UNIT – I

1	a)	What is memory address register (MAR) and memory data register (MDR) and Describe the IEEE standard for floating point numbers for single precision number.?	[7M]
	b)	Explain instruction formats for various types of computer organizations as single accumulator, general register andstack?	[7M]
2	a)	Explain the issues to be consider in accumulator based CPU with respect to programming considerations, instruction set.	[7M]
	b)	Illustrate the diagram for connection between the processor and the memory and explain basic operational concepts of computer.	[7M]

UNIT – II

3	a)	Write short notes on the following i. CPU-IOP communication ii. Micro program sequencer iii. Floating point arithmetic (addition and multiplication).	[7M]
	b)	Explain Booth's multiplication algorithm for signed 2's complement numbers in details, with a suitable example and give the hard ware requirement.	[7M]
4	a)	What is pipelining, branch penalty, and Draw the floating point addition subtraction unit neatly and explain the operation?	[7M]
	b)	Derive an algorithm in flow chart form for non restoring algorithm method of fixed point binary division?	[7M]

UNIT – III

5	a)	Write control signals for storing a word in memory and Draw a block diagram of control signal for register MDR?	[7M]
	b)	Explain in detail the decoding and encoding function of hardwired control unit and Compare hardwired control unit and micro programmed control unit?	[7M]

6 a) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. [7M]

b) Explain in detail regarding the implementation requirements of the pipeline? [7M]

UNIT – IV

7 a) Write formula for calculating the average access time experienced by the processor in a system with two level of caches? [7M]

b) Explain the following nodes of transfer in brief : [7M]

i. Interrupt – initiated I/O
ii. DMA.
iii. Explain the methods employed for establishing priority for simultaneous interrupts.

8 a) Draw the organization of the serial access memory unit and explain its accessing mechanism? [7M]

b) Criticize the following statement : "Using the faster processing chip results in a corresponding increase in the performance of computer even if the main memory speed remains the same". [7M]

UNIT – V

9 a) What are the three different mechanism commonly used in bus arbitration and What are the various mechanism for implementing i/o operation? [7M]

b) Write a short notes on the following: [7M]

i. RISC/CISC –Differentiate.
ii. Stored program organization

10 a) Write notes on: [7M]

i. Polling
ii. Vectored Interrupts
iii. Synchronous I/O
iv. Asynchronous I/O

b) Write a program to evaluate the arithmetic statement: X = (A - B + C * (D * E - f)) / (G + H*K) [7M]

a. Using a general register computer with three address instructions.
b. Using a general register computer with two addressinstructions.
c. Using an accumulator type computer with one address instructions.
d. Using a stack organized computer with zero-address operation instructions.

COURSE OBJECTIVES:

The course should enable the students to:

I	Understand the basic structure and operation of a digital computer.
II	Understand the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
III	Interpret the different types of control and the concept of pipelining.
IV	To study the different ways of communicating with I/O devices and standard I/O interfaces and RISC and CISC processors.
V	To study the hierarchical memory system including cache memories and virtual memory.

COURSE OUTCOMES:

CO 1	Ability to understand the concepts of associated with the computer system design and data representation.
CO 2	Explore the concepts associated with the fixed point arithmetic operations and algorithms.
CO 3	Understand the concepts of Control design of a computer.
CO 4	Ability to learn the concepts associated with the memory organization.
CO 5	Explore the concepts of System Organization including types of interrupts and processors.

COURSE LEARNINGOUTCOMES:

Students who complete the course will have demonstrated the ability to do the following.

AEC010.01	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.
AEC010.02	Understand the concepts associated with the computer organization.
AEC010.03	Describe various data representations and explain how arithmetic and logical operations are performed by computers.
AEC010.04	Understand instruction types, addressing modes and their formats in the assembly language programs.
AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.
AEC010.06	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).
AEC010.07	Describe the pipeline processing concept with multiple functional units.
AEC010.08	Understand the concept of the modified booth’s algorithm
AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.

AEC010.10	Describe the design of control unit with address sequencing and microprogramming Concepts.
AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.
AEC010.12	Understand the functionality of super scalar processing and Nano programming.
AEC010.13	Understand the concept of memory hierarchy and different typed of memory chips.
AEC010.14	Describe the concepts of magnetic surface recording, optical memories.
AEC010.15	Understand the cache and virtual memory concept in memory organization.
AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.
AEC010.17	Understand the various bus control interfaces and system control interfaces.
AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).
AEC010.19	Understand the functionally of RISC and CISC processors.
AEC010.20	Describe the concepts of superscalar and vector processor.

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNINGOUTCOMES:

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC010.03	Describe various data representations and explain how arithmetic and logical operations are performed by computers.	CO 1	Understand
	b	AEC010.04	Understand instruction types, addressing modes and their formats in the assembly language programs.	CO 1	Understand
2	a	AEC010.04	Understand instruction types, addressing modes and their formats in the assembly language programs.	CO 1	Understand
	b	AEC010.01	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.	CO 1	Understand
3	a	AEC010.06	Describe the various major algorithmic techniques (Robertson algorithm, booth‘s algorithm, non-restoring division algorithm).	CO 2	Understand
	b	AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.	CO 2	Understand
4	a	AEC010.07	Describe the pipeline processing concept with multiple functional units.	CO 2	Understand
	b	AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.	CO 2	Remember
5	a	AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.	CO 3	Understand
	b	AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.	CO 3	Remember
6	a	AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.	CO 3	Understand
	b	AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.	CO 3	Understand

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
7	a	AEC010.15	Understand the cache and virtual memory concept in memory organization.	CO 4	Understand
	b	AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.	CO 4	Understand
8	a	AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.	CO 4	Understand
	b	AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.	CO 4	Understand
9	a	AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).	CO 5	Understand
	b	AEC010.19	Understand the functionally of RISC and CISC processors.	CO 5	Remember
10	a	AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).	CO 5	Understand
	b	AEC010.20	Describe the concepts of superscalar and vector processor.	CO 5	Remember

Signature of Course Coordinator **HOD, ECE**