INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONIC DEVICES AND CIRCUITS
III SEMISTER
(COMMON TO ECE/EEE)

Prepared By

Mr. V R Seshagiri Rao, Professor

Dr. P Ashok Babu, Professor

Mr. K Sudhakar Reddy, Asst. Prof.

Mr. S Rambabu, Asst. Prof.

Mr. B Naresh, Asst. Prof.

UNIT-1
SEMICONDUCTOR DIODES

Introduction

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.

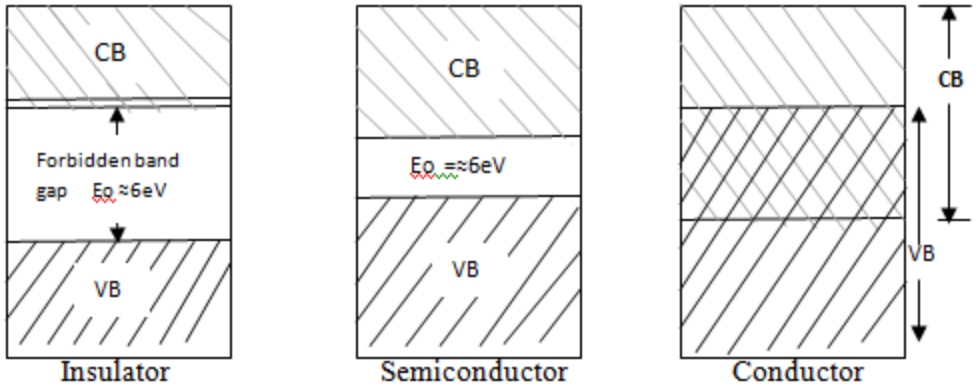


Fig.1: Energy band diagrams for insulator, semiconductor and conductor

Insulator: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Ex: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of 10^{10} to 10^{12} Ω-cm. The energy band structure of an insulator is shown in the fig.1.

Introduction

Conductors:

- A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. I.e. it has very high conductivity. Ex: Copper, Aluminum, Silver, and Gold. The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} Ω-cm.
- The Valance and conduction bands overlap (fig.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

Introduction

Semiconductor

A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and 10^4 Ω-cm. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable of conducting some current at room temperature.

Introduction

Semiconductor Types:

Intrinsic Semiconductor: A pure form of semiconductors is called as intrinsic semiconductor (sc). Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used.

Other examples include Gallium arsenide GaAs, InSb etc.

Extrinsic Semiconductor: The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor.

By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping.

Introduction

N type semiconductor:

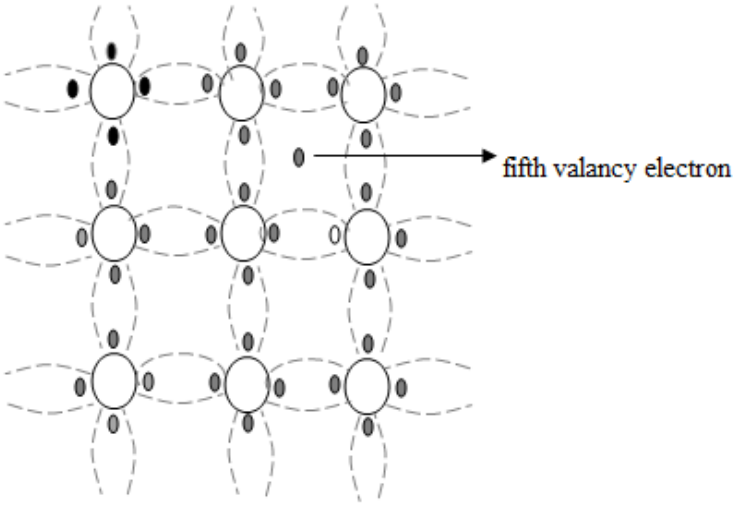


Fig.2: Crystal structure of N-type Semiconductor

If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

Introduction

N type semiconductor:

- A pentavalent impurity has five valance electrons. Fig.2 shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms.

- The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy.

Introduction

P type semiconductor:

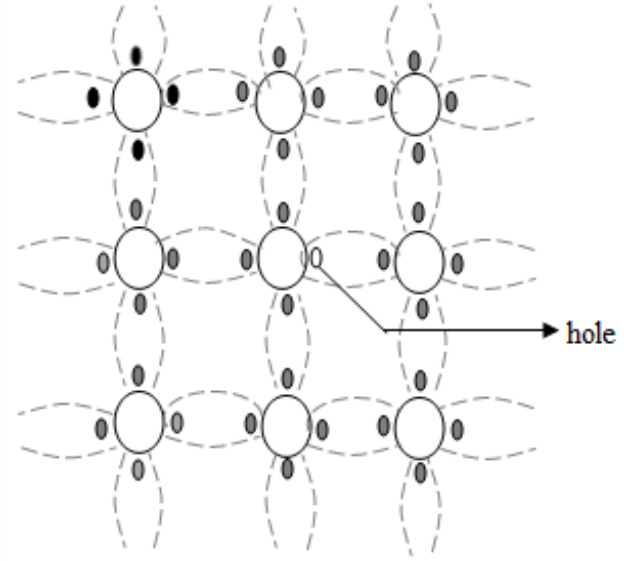


Fig.3: Crystal structure of P-type Semiconductor

If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium, indium etc.

Introduction

P type semiconductor:

The crystal structure of p type sc is shown in the fig.3. The three valance electrons of the impurity (boon) forms three covalent bonds with the neighboring atoms and a vacancy exists in the fourth bond giving rise to the holes.

The hole is ready to accept an electron from the neighboring atoms. Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valance band.

At the same time the no. electrons are decreased compared to those available in intrinsic sc because of increased recombination due to creation of additional holes.

Introduction

Conductivity of semiconductor:

In a pure semiconductor, the no. of holes is equal to the no. of electrons. Thermal agitation continue to produce new electron- hole pairs and the electron hole pairs disappear because of recombination with each electron hole pair created , two charge carrying particles are formed . One is negative which a free electron with mobility (μn) is. The other is a positive i.e., hole with mobility (μp). The electrons and hole move in opposite direction in an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic sc is given by

$$J = J_n + J_p$$

$$= q\, n\, \mu_n\, E + q\, p\, \mu_p\, E$$

$$= (n\, \mu_n + p\, \mu_p)\, qE$$

$$= \sigma\, E$$

Qualitative theory of PN Junction diode

PN JUNCTION WITH NO APPLIED VOLTAGE OR OPEN CIRCUIT CONDITION

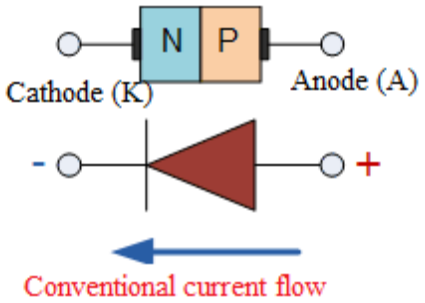


Fig.4: construction of PN junction

- In a piece of sc, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig.4.
- The n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of free electrons to diffuse over to the P side and the holes to the N side. This process is called diffusion.

Qualitative theory of PN Junction diode

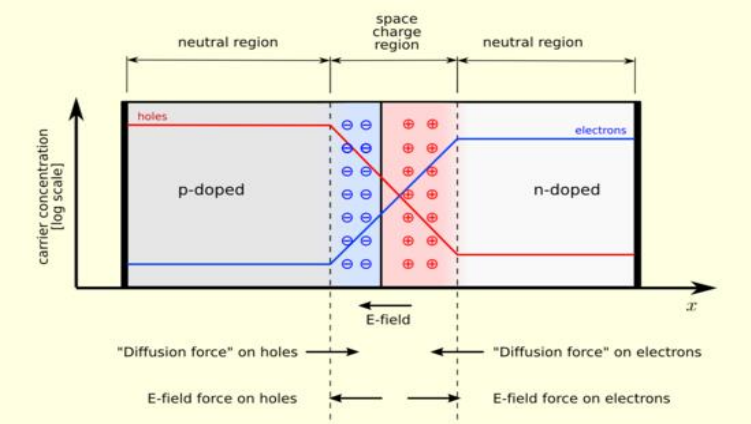


Fig.5: Charge carrier density

➢The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction.

Qualitative theory of PN Junction diode

➢The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a negatives pace charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig.5

Operation of PN Junction under forward bias

pn junction diode

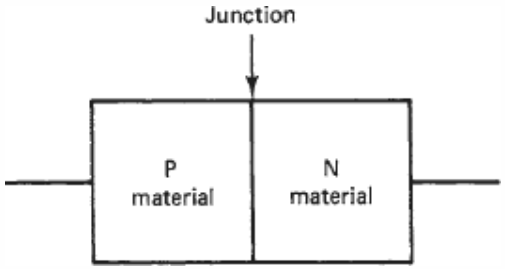
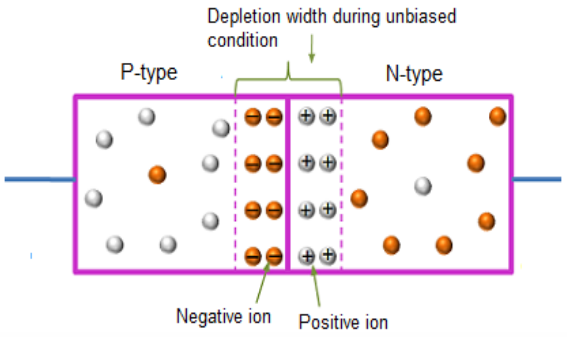


Fig.6: Formation of pn junction

- A diode is a two layer, two-terminal Semiconductor device. One terminal is attached to P material and the other to N material.
- The common connecting point where these materials are joined is called a junction.
- The terminal which is connected to P side is anode and the terminal which is connected to N side is called cathode.

Operation of PN Junction under forward bias

Unbiased diode



- When a diode is connected in a Zero Bias condition, no external potential energy is applied to the PN junction.
- However if the diodes terminals are shorted together, a few holes (majority carriers) in the P-type material with enough energy to overcome the potential barrier will move across the junction against this barrier potential. This is known as the “Forward Current” and is referenced as IF.

Operation of PN Junction under forward bias

Operation of PN Junction under forward direction

An external voltage applied to a PN junction is called BIAS. The positive terminal of the bias battery is connected to the P-type material and the negative terminal of the battery is connected to the N-type material.

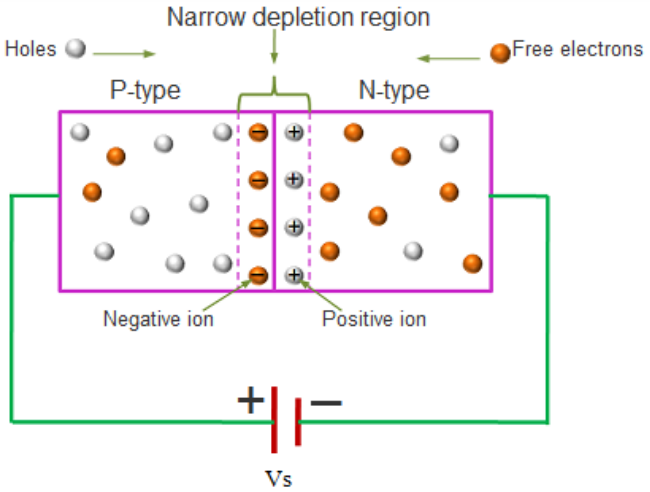


Fig.7: Forward biased pn junction diode.

Operation of PN Junction under Reverse bias

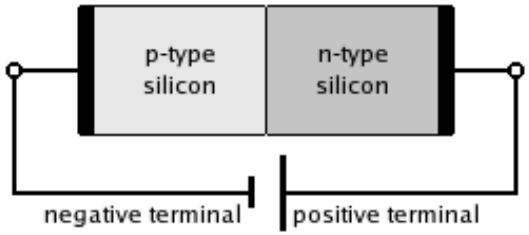


Fig.8: Reverse biased pn junction diode.

- When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.
- The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.
- The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Operation of PN Junction under reverse bias

Reverse Biased Junction Diode showing an Increase in the Depletion Layer

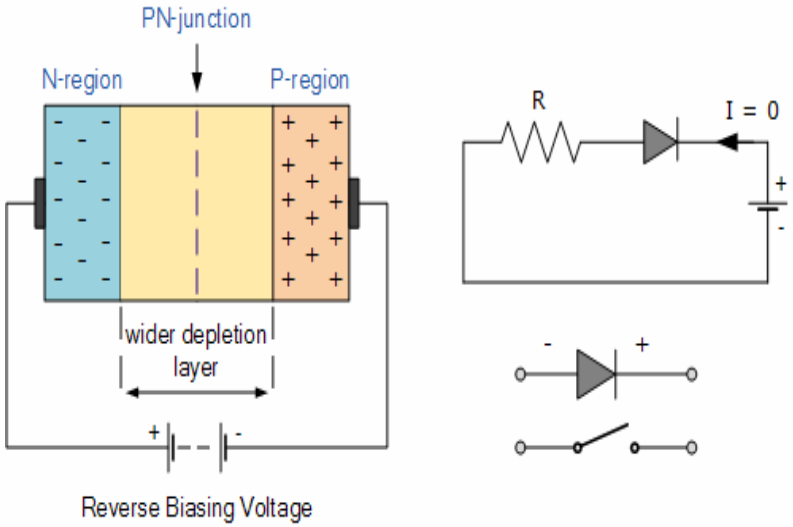


Fig.9: reverse biased pn junction with increased depletion layer.

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small leakage current does flow through the junction which can be measured in microamperes, (μA)

Volt-Ampere Characteristics

Forward Characteristics:

- When a diode is connected in the forward bias direction it conducts forward current IF. The value of IF is directly dependant on the amount of forward voltage VF.
- When the forward voltage of the diode equals 0V, the IF equals 0 mA. This value starts at the origin point (0) of the graph.
- If VF is gradually increased in 0.1-V steps, IF begins to increase. When the value of VF is great enough to overcome the barrier potential of the P-N junction, a substantial increase in IF occurs.
- The point at which this occurs is often called the knee voltage V_K (Cut-in voltage or threshold voltage).

Volt-Ampere Characteristics

Forward Characteristics:

- For germanium diodes VK is approximately 0.3 V and 0.7 V for silicon.

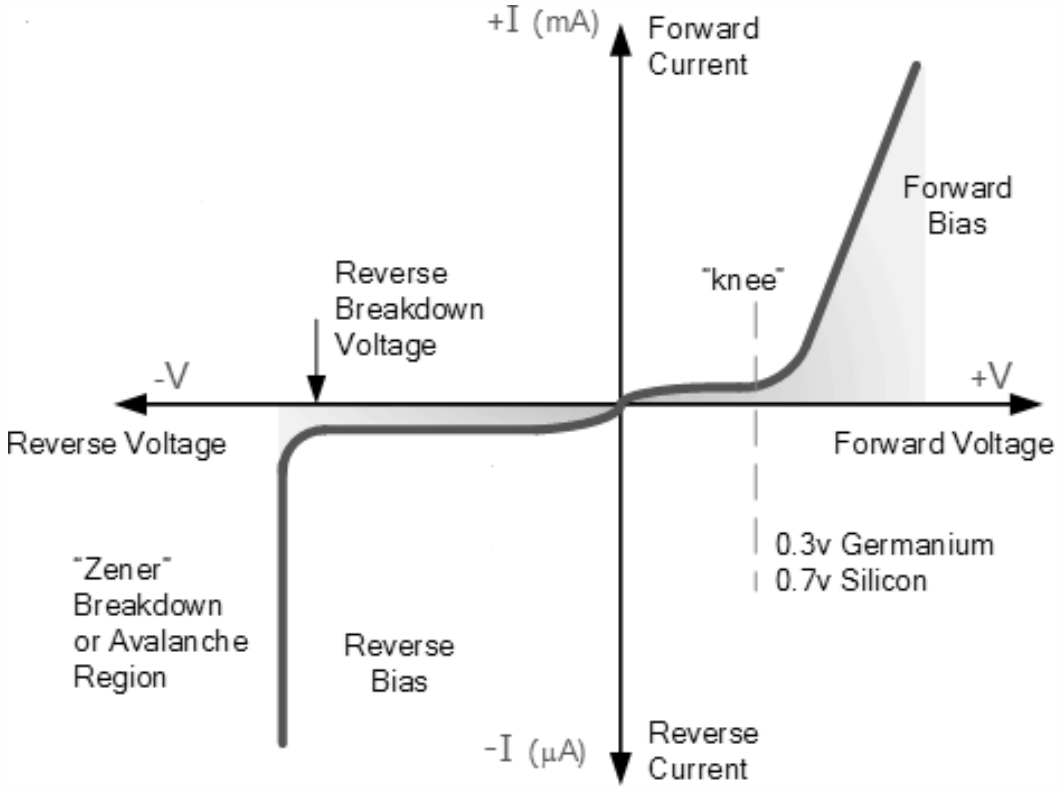


Fig.10: forward & reverse V-I Characteristics

Volt-Ampere Characteristics

Reverse Characteristics:

- When a diode is connected in the reverse bias direction it has a V_R - I_R characteristic. This characteristic has different values of I_R and V_R. Reverse current is usually quite small.
- The vertical I_R line in this graph has current values graduated in microamperes. Starting in zero when the reverse voltage of a diode is increased there is a very slight change in I_R. At the breakdown voltage V_{BR} point, current increases very rapidly.
- The voltage across the diode remains fairly constant at this time. Break down occurs in PN junction diode because of Avalanche effect.

Volt-Ampere Characteristics

Reverse Characteristics:

- Avalanche breakdown occurs in lightly doped diodes. Here the applied reverse voltage is not enough to break covalent bonds but can accelerate the minority carriers.
- Accelerated minority carriers collide with semiconductor atoms and produces new electron hole pairs. Newly created carriers also participation in current conduction and produce more electron hole pairs. This process is cumulative.
- The process continues to build up until an avalanche of current carriers takes place. When this occurs the process is irreversible and it may damage the junction.

Diode Equation

When a forward bias is applied to a diode, holes are injected from the p side to the n side. Due to this, the concentration of holes in the n side (p_n) is increased from its thermal equilibrium vakue (p_{no}) and injected hole concentration [$P_{n(x)}$] decreases exponentially with respect to distance (x)

$$P_n(x) = P_n - P_{no} = P_n(0)e^{-\frac{x}{L_p}}$$

Where L_p is the diffusion length for holes in the N- material.

Diode Equation

Injected hole concentration at x=0 is

$$P_n(0) = P_n(0) - P_{no}$$

Let p_p and p_n be the hole concentration at the edges of the space charge in the p and b sides, respectively. Let VB (= Vo-V) be the effective barrier potential across the depletion layer. Then

$$P_p = P_n e^{\frac{V_B}{V_T}}$$

Diode Equation

Under open circuit condition (i.e. V=0), $P_p = P_{po}$, $P_n = P_{no}$ and $V_B = V_o$, then above equation can be changed into

$$P_{po} = P_{no} e^{\frac{V_o}{V_T}}$$

Forward currents:

The hole current crossing the junction into the n side with x=o is

$$I_{pn}(0) = \frac{AeD_p P_n(0)}{L_p} = \frac{AeD_p P_{n0}}{L_p}(e^{V/V_T} - 1)$$

Diode Equation

The electron current crossing the junction unto the p side with x=0 is

$$I_{pn}(0) = \frac{AeD_n N_p(0)}{L_n} = \frac{AeD_n n_{p0}}{L_n}(e^{V/V_T} - 1)$$

The total diode current,

$$I = I_{pn}(0) + I_{np}(0) = I_0(e^{V/V_T} - 1)$$

Where

$$I_0 = \frac{AeD_p P_{n0}}{L_p} + \frac{AeD_n n_{p0}}{L_n}$$

If we consider carrier generation and recombination in the space charge region, the general equation of the diode current is approximately given by

Diode Equation

$$I = I_0 (e^{V/\eta V_T} - 1)$$

Where

I= diode current

I_0= diode reverse saturation current at room temperature

V= external voltage applied to the diode

η = a constant, 1 for germanium and 2 for silicon

$V_T = KT/q = T/11600$

K= Boltzmann's constant, q = charge of the electron

T = temperature of the diode junction.

At room temperature, VT = 26mV.

Temperature dependence of V-I characteristics

Diode terminal characteristics equation for diode junction current

$$I_D = I_0 (e^{\frac{v}{\eta v_T}} - 1)$$

Where

VT = kT/q

VD- diode terminal voltage, Volts

Io - temperature-dependent saturation current, µA

T - absolute temperature of p-n junction, K

k - Boltzmann's constant 1.38x 10 -23J/K

q - electron charge 1.6x10-19 C

= empirical constant, 1 for Ge and 2 for Si

Temperature dependence of V-I characteristics

- The reverse saturation current I_o of diode increases approximately 7 percent/^oC for both germanium and silicon. Since $(1.07)^{10}= 2$, reverse saturation current approximately doubles for every 10^o C rise in temperature.

- Hence, if the temperature is increased at fixed voltage, the current I increases. To bring the current I to its original value, the voltage V has to be reduced.

Temperature dependence of V-I characteristics

Temperature Effects on Diode

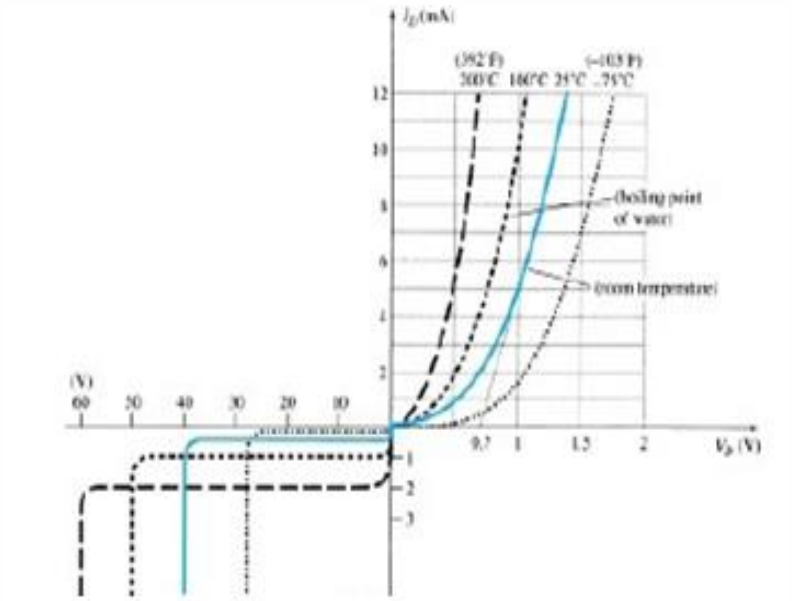


Fig.11: variations in diode characteristics with temperature change

Temperature dependence of V-I characteristics

Temperature Effects on Diode

- For germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium.
- The increasing levels of Io with temperature account for the lower levels of threshold voltage, as shown in Fig.1. Simply increase the level of Io in and not rise in diode current. Of course, the level of TK also will be increase, but the increasing level of Io will overpower the smaller percent change in TK. As the temperature increases the forward characteristics are actually becoming more “ideal”.

Ideal Vs Practical – Resistance levels

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.and applying the following Equation

$$R_D = \frac{V_D}{I_D}$$

Ideal Vs Practical – Resistance levels

DC or Static Resistance

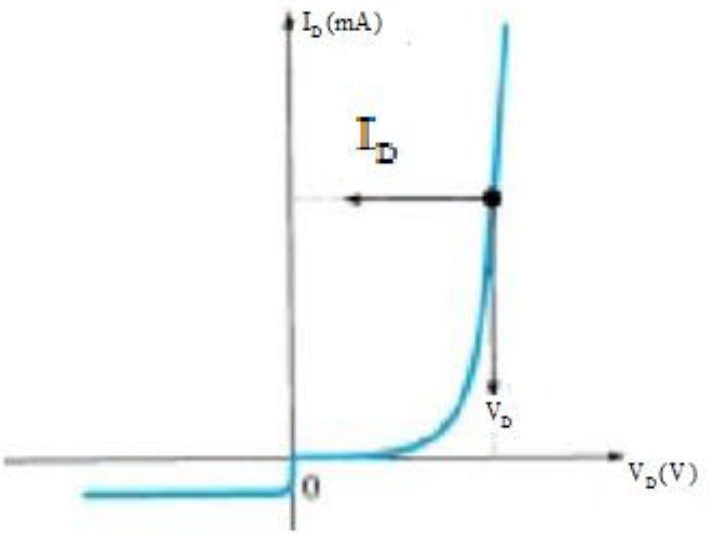


Fig.12: Determining the dc resistance of a diode at a particular operating point.

Ideal Vs Practical – Resistance levels

AC or Dynamic Resistance

- If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig.2 With no applied varying signal, the point of operation would be the Q-point appearing on Fig.2 determined by the applied dc levels.
- The designation Q-point is derived from the word quiescent, which means “still or unvarying.” A straight-line drawn tangent to the curve through the Q-point as shown in Fig.2.

Ideal Vs Practical – Resistance levels

AC or Dynamic Resistance

AC Resistance is given by

$$r_D = \frac{\Delta V_D}{\Delta I_D}$$

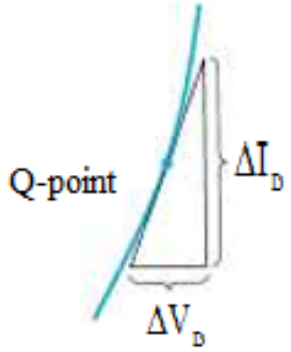


Fig.13: Determining the AC resistance at Q-Point

Transition and Diffusion Capacitances

In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by C = €A /d

The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig.14.

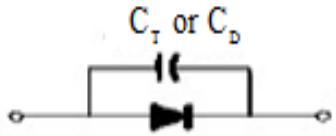


Fig.14: Including the effect of transition and diffusion capacitances.

Transition and Diffusion Capacitances

Diffusion capacitance (C_D)

Diffusion capacitance occurs in a forward biased p-n junction diode. Diffusion capacitance is also sometimes referred as storage capacitance. It is denoted as C_D. In a forward biased diode, diffusion capacitance is much larger than the transition capacitance. Hence, diffusion capacitance is considered in forward biased diode. The diffusion capacitance occurs due to stored charge of minority electrons and minority holes near the depletion region.

When forward bias voltage is applied to the p-n junction diode, electrons (majority carriers) in the n-region will move into the p-region and recombines with the holes. A large number of charge carriers, which try to move into another region will be accumulated near the depletion region before they recombine with the majority carriers. As a result, a large amount of charge is stored at both sides of the depletion region.

Transition and Diffusion Capacitances

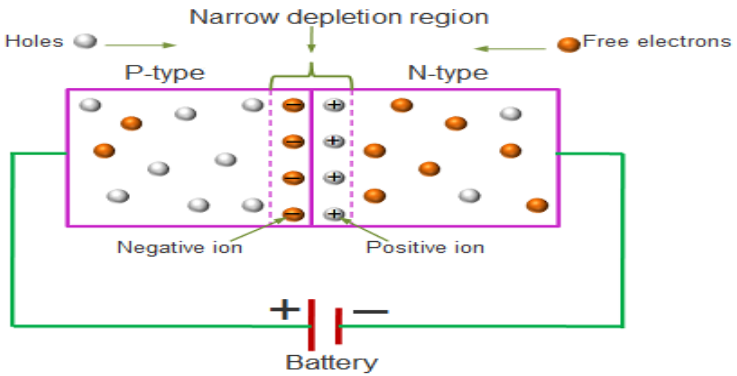


Fig.15: PN Junction diode forward bias

The formula for diffusion capacitance is

$$CD = dQ / dV$$

Where,

CD = Diffusion capacitance

dQ = Change in number of minority carriers stored outside the depletion region

dV = Change in voltage applied across diode

Transition and Diffusion Capacitances

Transition capacitance (CT)

- Just like the capacitors, a reverse biased p-n junction diode also stores electric charge at the depletion region. The depletion region is made of immobile positive and negative ions. In a reverse biased p-n junction diode, the p-type and n-type regions have low resistance.
- Hence, p-type and n-type regions act like the electrodes or conducting plates of the capacitor. The depletion region of the p-n junction diode has high resistance. Hence, the depletion region acts like the dielectric or insulating material. Thus, p-n junction diode can be considered as a parallel plate capacitor.

Transition and Diffusion Capacitances

Transition capacitance (CT)

The transition capacitance can be mathematically written as,

$$C_T = \varepsilon A / W$$

Where,

ε = Permittivity of the semiconductor

A = Area of plates or p-type and n-type regions

W = width of depletion region

The Ideal - Diode Model

Perfect conductor with zero voltage drops when the diode is forward biased. Open circuit, when the diode is reversed biased.

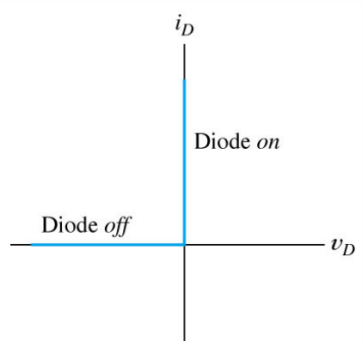


Fig.16: Ideal diode characteristics

Diode Equivalent Circuits, Load Line Analysis

Simplified Equivalent Circuit

- For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. The removal of r_{av} from the equivalent circuit is the same as implying that the characteristics of the diode appear as shown in Fig.17.

- The reduced equivalent circuit appears in the same figure. It states that a forward-biased silicon diode in an electronic system under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current.

Diode Equivalent Circuits, Load Line Analysis

Simplified Equivalent Circuit

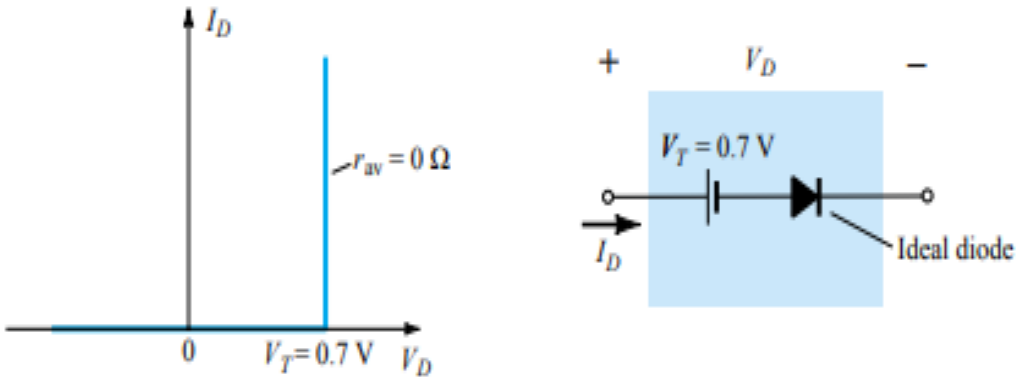


Fig.17: Simplified equivalent circuit for semiconductor diode.

Diode Equivalent Circuits, Load Line Analysis

Piecewise-Linear Equivalent Circuit

➢One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig.18.

➢The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 16 that the straight-line segments do not result in an exact duplication of the actual

Piecewise-Linear Equivalent Circuit

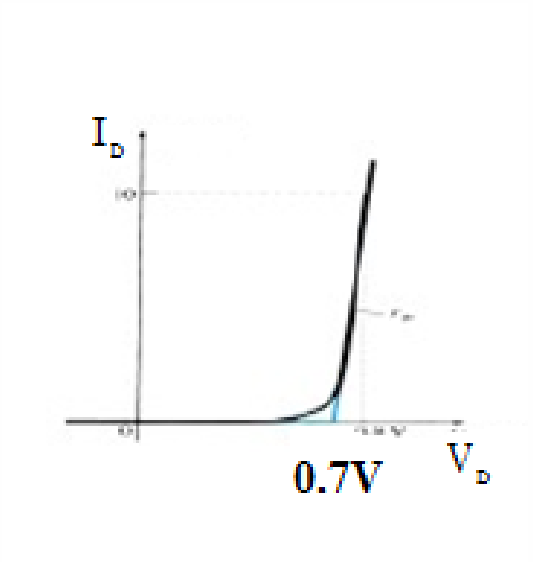


Fig.18: Piecewise linear equivalent circuit

Diode Equivalent Circuits, Load Line Analysis

Load line Analysis

- The applied load will normally have an important impact on region of operation of device.
- If analysis is done in graphical approach, a line can be drawn on the characteristics of the device that represents applied load.
- The intersection of load line with the characteristics will determine the point of operation. Such an analysis is called as load-line analysis. The intersection point is called ‘Q’ point or operating point.

Breakdown Mechanisms in Semiconductor Diodes

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction

1. avalanche breakdown and
2. Zener breakdown.

Breakdown Mechanisms in Semiconductor Diodes

Avalanche breakdown

- The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semi-conductor material.
- As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown.

Breakdown Mechanisms in Semiconductor Diodes

Zener breakdown

- Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current.
- This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 10^7 V/m.

Breakdown Mechanisms in Semiconductor Diodes

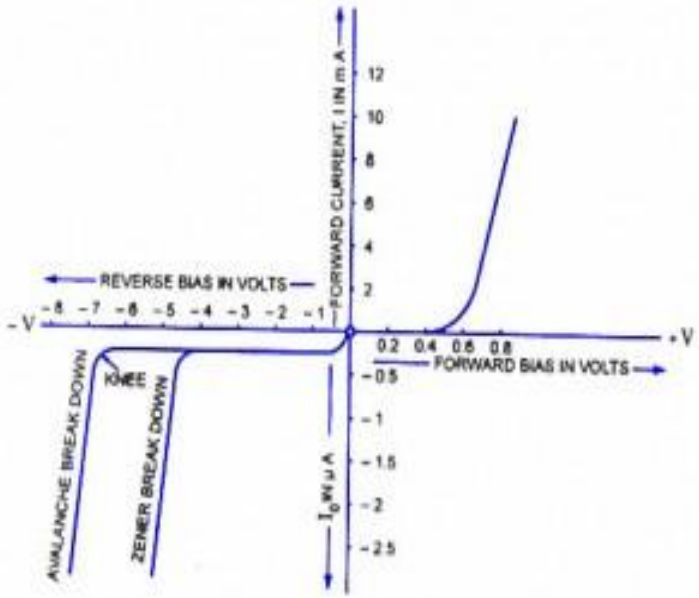


Fig.19: avalanche breakdown and Zener breakdown.

Zener Diode Characteristics

Zener diode

A Zener diode is a type of diode that permits current not only in the forward direction like a normal diode, but also in the reverse direction if the voltage is larger than the breakdown voltage known as "Zener knee voltage" or "Zener voltage". The device was named after Clarence Zener, who discovered this electrical property.

Fig.20: Zener Diode symbol

Zener Diode Characteristics

Zener diode Characteristics

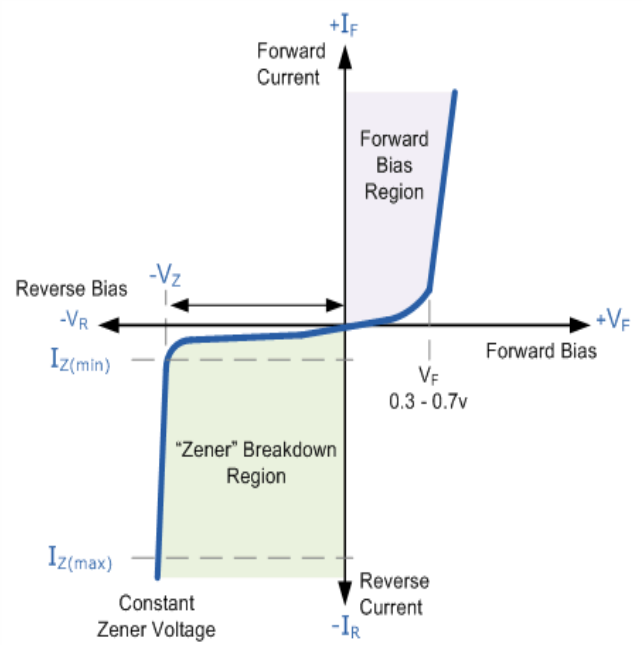


Fig.21: Zener diode characteristics

Zener Diode Characteristics

Zener diode Characteristics

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.

Zener diode as a voltage regulator

- Keeping the zener diode in parallel with a variable load resistance R_L, ensures a constant output voltage even though the load current and the supply voltage varies. In practical circuits the simplest form of current source is a resistor.
- The key in using the zener diode as voltage regulator is that as long as the zener diode is reverse biased, the flow of current greater than a few micro amperes must be accompanied by a voltage greater than the Zener voltage. This type of arrangement of the circuit provides safety for equipment connected to terminals. This arrangement of regulator circuit is referred to as a shunt regulator in which the regulating element is placed in parallel with the load.

Zener diode as a voltage regulator

Zener as Voltage regulator

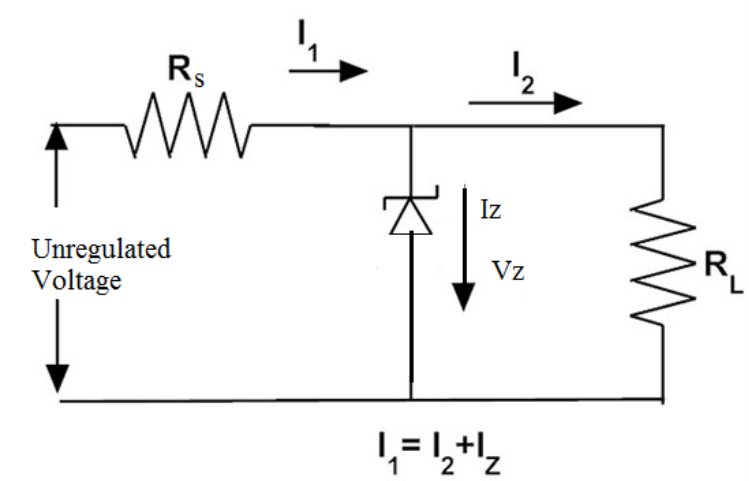


Fig.22: Zener Diode as Voltage Regulator

Zener diode as a voltage regulator

Zener as Voltage regulator

- When the load is not connected across the zener diode, no load current will be conducted and all the current due to the circuit will pass through the zener diode dissipating maximum amount of power that causes overheating of the diode and damages permanently.

- Selecting the appropriate values of series resistance R_s is also important because it also causes greater diode current, so that maximum power dissipation of the diode should not be exceeded under no load or at high impedance condition.

Zener diode as a voltage regulator

Zener as Voltage regulator

- Whenever a load is connected in parallel with zener diode, voltage across the load is same as the zener diode voltage. However the source voltage must be greater than the zener voltage and the upper limit of zener current depends on the power rating of the zener diode, otherwise the zener voltage will simply follow the applied input voltage.
- It is also necessary that both zener diode and resistor should have a high rating of power to handle all of the current across the circuit. If a decoupling capacitor is present across the zener diode, it is more useful in providing additional smoothing to the DC supply which is necessary to stabilize the voltage.

UNIT- 2

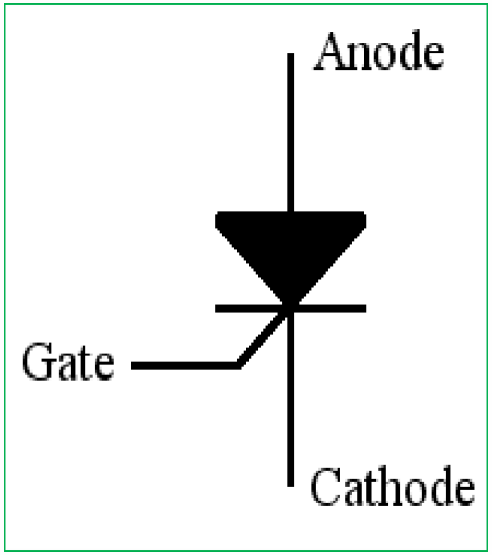
SPECIAL ELECTRONIC DEVICES AND RECTIFIERS

SCR

What is a silicon control rectifier?

A Silicon Controlled Rectifier (SCR) is a four layer solid state device that controls current flow. SCR is a three terminal device.

- The terminals are:
  - Gate (G)
  - Anode (A)
  - Cathode (K)



Basic SCR structure

- The SCR consists of a four layer p-n-p-n structure with the outer layers are referred to as the anode (p- type) and cathode (n-type). The control terminal of the SCR is named the gate and it is connected to the p-type layer located next to the cathode.
- The three junctions are normally denoted as J_1, J_2, and J_3. They are numbered serially with J_1 being nearest to the anode.

VARACTOR DIODE

INTRODUCTION

Varactor diode is a special type of PN junction diode, in which PN junction capacitance is controlled using reverse bias voltage. When the diode is forward biased, current will flow through the diode. When the diode is reverse biased, charges in the P and N semiconductors are drawn away from the PN junction interface and hence forms the high resistance depletion zone.

The Varactor diode is also known as:

- Variable capacitance (Varicap) diode
- Voltage – Variable Capacitor (VCC) diode
- Tuning diode
- Variable reactance diode

RECTIFIERS

RECTIFIERS

- Rectifier is a device which convert AC voltage in to pulsating DC
- A rectifier utilizes unidirectional conducting device Ex : P-N junction diodes

IMPORTANT VARIBLES IN RECTIFIERS

- Rectifier efficiency
- Peak value of the current
- Peak value of the voltage
- Ripple factor

TYPES

- Depending up on the period of conduction
  - ❖ Half wave rectifier
  - ❖ Full wave rectifier
- Depending up on the connection procedure
  - ❖Bridge rectifier

RECTIFIERS

HALF WAVE RECTIFIER

- As diodes conduct current in one direction and block in other.
- When connected with ac voltage, diode only allows half cycle passing through it and hence convert ac into dc.
- As the half of the wave get rectified, the process called half wave rectification. A diode is connected to an ac source and a load resistor forming a half wave rectifier.
- Positive half cycle causes current through diode, that causes voltage drop across resistor.

RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 \, d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m \, sim(wt))^2 \, d(wt)}$$

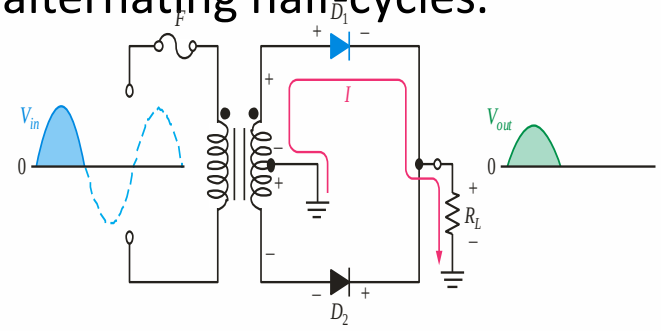
$$V_{rms} = \frac{V_m}{2}$$

RMS CURRENT:

$$I_{rms} = \frac{I_m}{2}$$

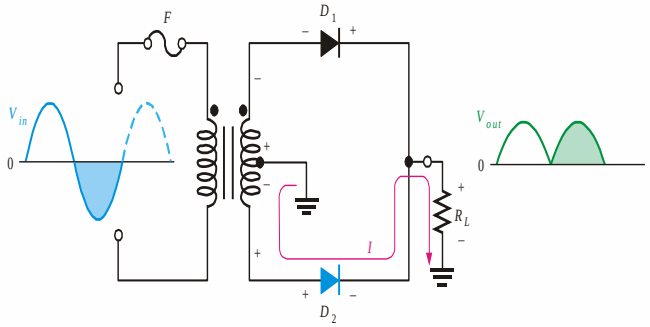
FULLWAVE RECTIFIER

- A center-tapped transformer is used with two diodes that conduct on alternating half-cycles.



During the positive half-cycle, the upper diode is forward-biased and the lower diode is reverse-biased.

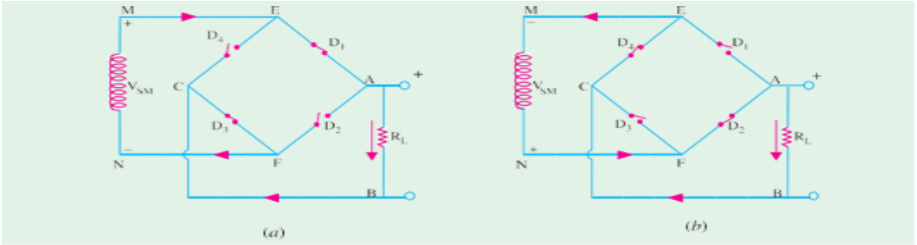
During the negative half-cycle, the lower diode is forward-biased and the upper diode is reverse-biased.



BRIDGE RECTIFIER

WORKING

- During the positive input half-cycle, terminal *M* of the secondary is positive and *N* is negative as shown separately in Fig. Diodes *D*1 and *D*3 become forward-biased (ON) whereas *D*2 and *D*4 are reverse-biased (OFF). Hence, current flows along *MEABCFN* producing a drop across *RL*.
- During the negative input half-cycle, secondary terminal *N* becomes positive and *M* negative. Now, *D*2 and *D*4 are forward-biased. Circuit current flows along *NFABCEM* as shown in Fig. (*b*). Hence, we find that current keeps flowing through load resistance *RL* in the same direction *AB* during both half-cycles of the ac input supply.



HARMONIC COMPONENTS IN A RECTIFIER CIRCUIT

- The term harmonic is defined as “a sinusoidal component of a periodic waveform or quantity possessing a frequency, which is an integral multiple of the fundamental frequency.”
- By definition, a perfect sine wave has no harmonics, except fundamental component at one frequency. Harmonics are present in waveforms that are not perfect sine waves due to distortion from nonlinear loads. The French mathematician named Fourier discovered that a distorted waveform can be represented as a series of sine waves, with each being an integer multiple of the fundamental frequency and each with a specific magnitude.

PI-SECTION FILTER

- It consists of one inductor and two capacitors connected across its each end. The three components are arranged in the shape of the Greek letter p. It is also called capacitor input p-filter. The input capacitor *C*1 is selected to offer very low reactance to the ripple frequency. Hence, major part of filtering is done by *C*1. Most of the remaining ripple is removed by the combined action of *L* and *C*2.
- This circuit gives much better filtering than *LC* filter circuit. However, *C*1 is still directly connected across the supply and would need high pulses of current if load current is large. Since these high peak current pulses are likely to damage the rectifier diode, this filter is used *with low-current equipment*.
- Though this filter-gives somewhat higher output voltage, its voltage regulation is inferior to that of the *LC* filter.

PI-SECTION FILTER

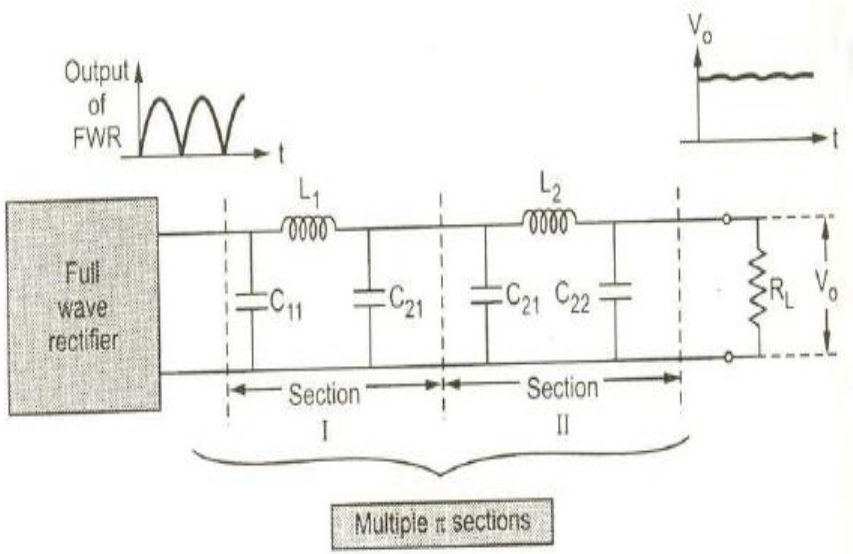
1. By acting as a pre-load on the supply, it causes an initial voltage drop. When the real load is connected, there is only a small amount of additional drop. In this way, difference between no-load and full- load voltage is reduced thereby improving the regulation.

2. It provides safety to the technicians handling the equipment. When power supply is switched off, it provides a path for the filter capacitor to discharge through. That is why it is called bleeder resistor. Without it, the capacitor will retain its charge for quite sometime even when the power supply is switched off. This high voltage can be dangerous for people working with the equipment.

3. By maintaining a minimum current through the choke, it improves its filtering action. Value of *RB* should be such as to conduct 10 per cent of the total load current

MULTIPLE SECTION FILTER

To obtain almost pure dc to the load, more Π-sections may be used one after another. Sucha filter using more than one Π-section is called multiple Π-section filter. The figure shows multipleΠ-section filters



$$\gamma = \sqrt{2}\,\frac{X_{c_{11}}}{R_L}\,\frac{X_{c_{12}}}{X_1}\,\frac{X_{c_{22}}}{X_2}$$

UNIT 3

Transistors

Transistor Construction, BJT Operation

INTRODUCTION

- The basic of electronic system nowadays is semiconductor device.
- The famous and commonly use of this device is BJTs (Bipolar Junction Transistors).
- It can be use as amplifier and logic switches.
- BJT consists ofthree terminal:

  collector : C base : B emitter : E
- Two types of BJT : pnp and npn

Transistor Construction

- 3 layer semiconductor device consisting:

  -2 n- and 1 p-type layers of material -npn transistor

  - 2 p- and 1 n-type layers of material-pnp transistor

  •The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material

  •A single pn junction has two different types of bias:

  - forward bias
  - reverse bias

  •Thus, a two-pn-junction device has four types of bias.

Position of the terminals and symbol of BJT.

- Base is located at the middle and more thin from the level of collector and emitter
- The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material

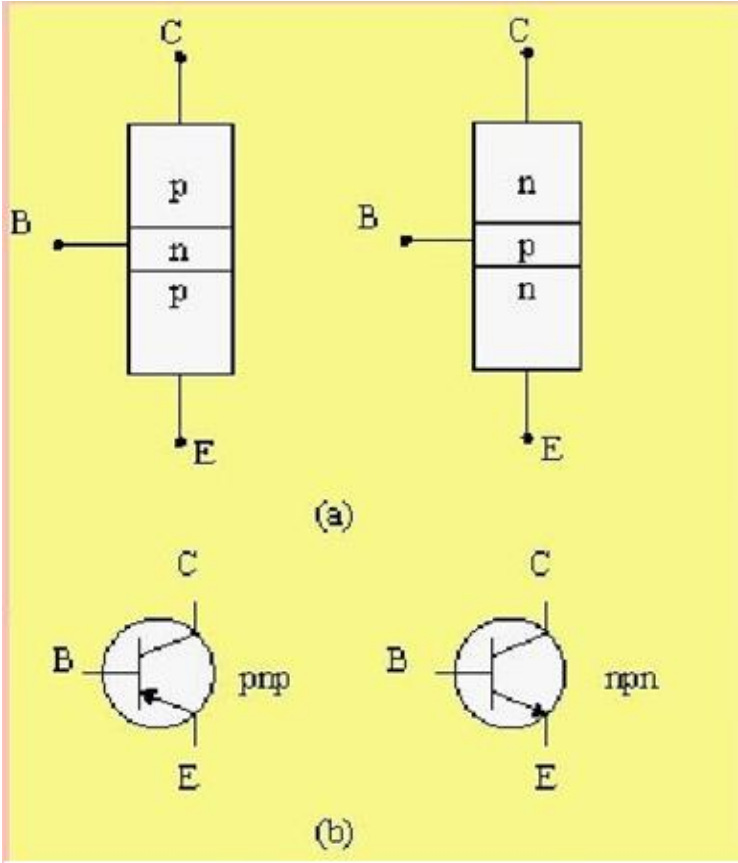


Fig.1a : Positionof Terminals,
Fig.1b: Types of Transistors

BJT Operation

- Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.
- Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.
- A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.
- The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal.

Minority carrier distribution and current components

- By imaging the analogy of diode, transistor can be construct like two diodes that connected together.
- It can be conclude that the work of transistor is base on work of diode.

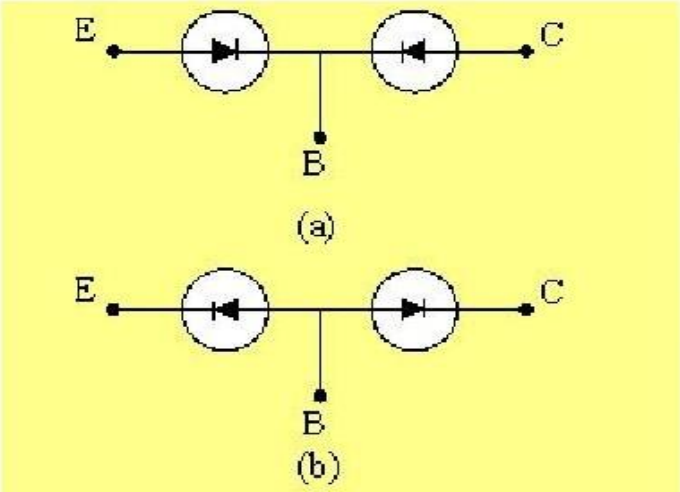


Fig. 4.2: (a) pnp transistor (b) npn transistor

Transistor Construction

- 3 layer semiconductor device consisting:

  -2 n- and 1 p-type layers of material -npn transistor

  - 2 p- and 1 n-type layers of material-pnp transistor

  •The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material

  •A single pn junction has two different types of bias:

  - forward bias
  - reverse bias

  •Thus, a two-pn-junction device has four types of bias.

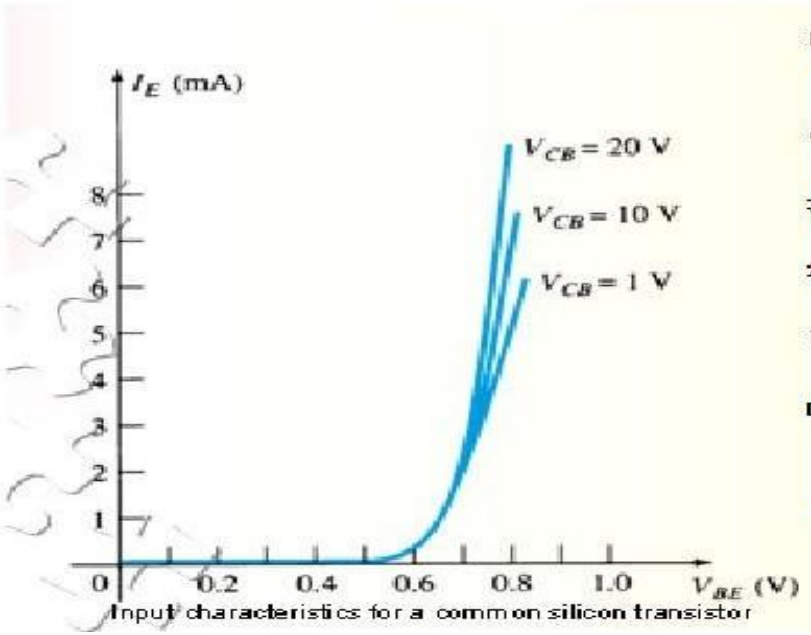
CB Configurations, Characteristics

Common-Base Configuration

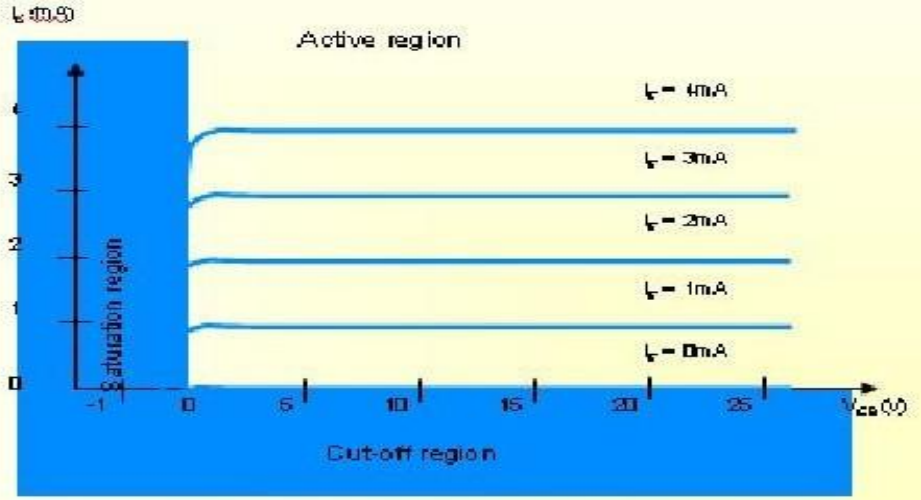
- Common-base terminology is derived from the fact that the base is common to both input and output of the configuration. Base is usually the terminal closest to or at ground potential.
- All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.
- Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

CB Configurations, Characteristics

- To describe the behavior of common-base amplifiers requires two set of characteristics:
  - Input or driving point characteristics.
  - Output or collector characteristics
- The output characteristics has 3 basic regions:
  - Active region -defined by the biasing arrangements



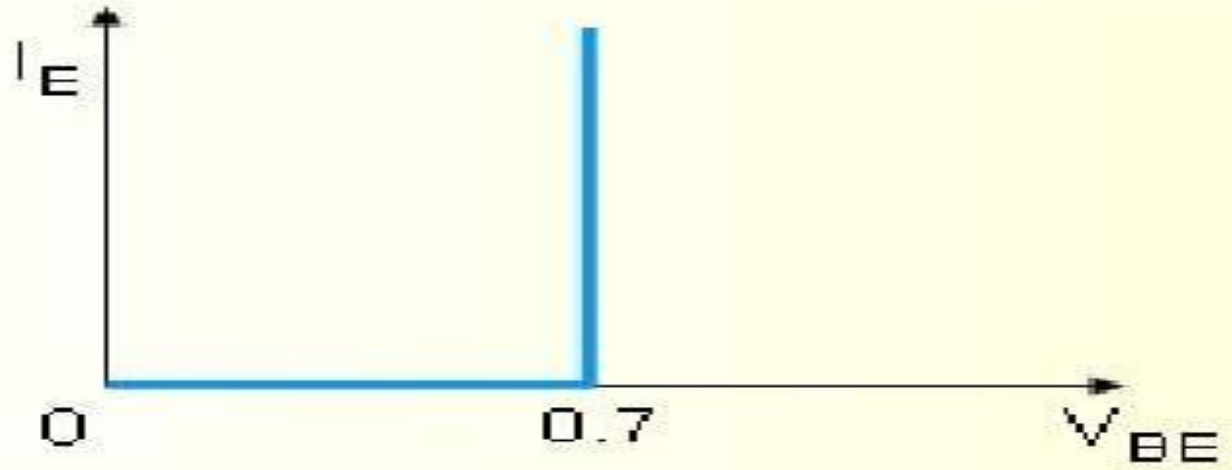
Input characteristics for a common silicon transistor



Output of collector characteristics for common-base transistor amplifier

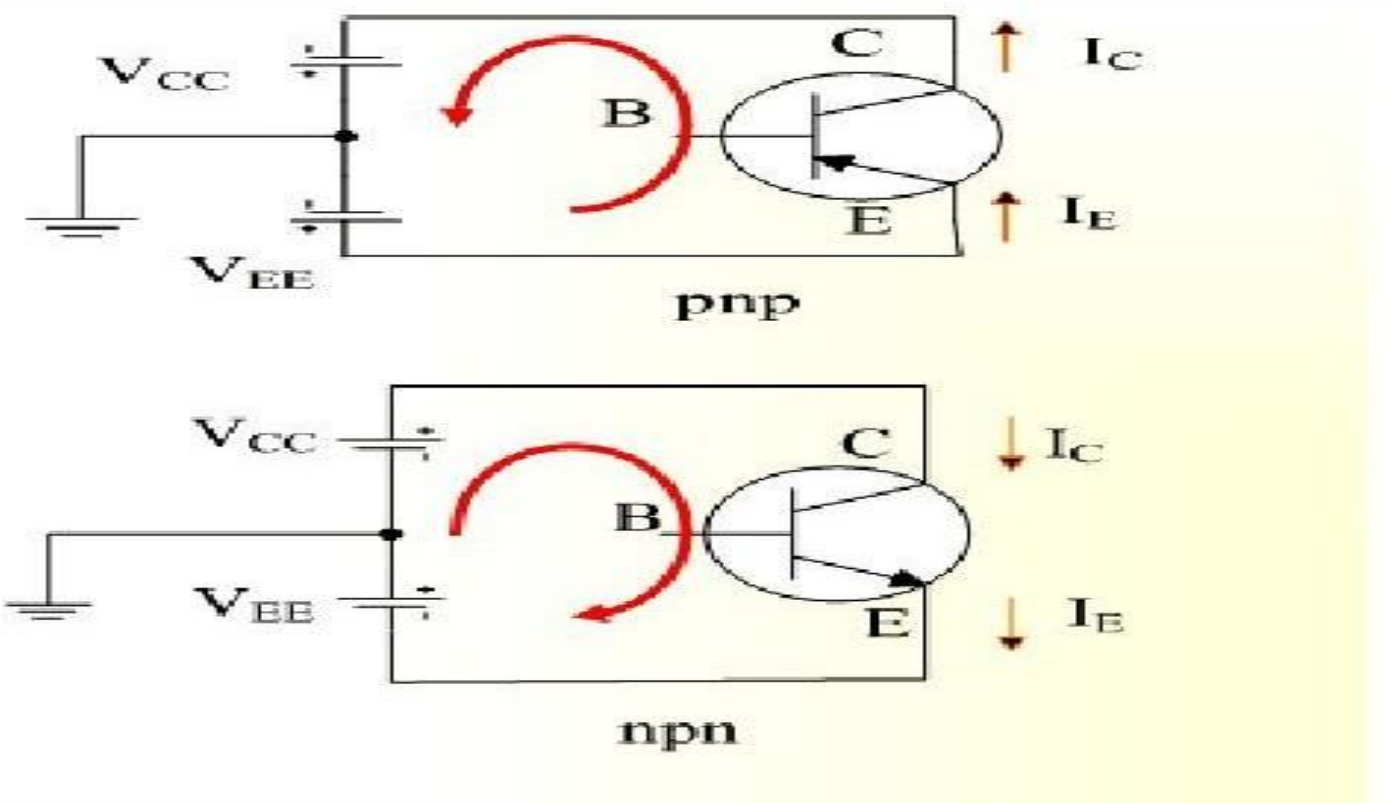
CB Configurations, Characteristics

- The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by IC ≈IE
- Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be VBE = 0.7V



CB Configurations, Characteristics

- In the dc mode the level of IC and IE due to the majority carriers are related by a quantity called alpha = Ic/ Ie



CE Configurations, Characteristics

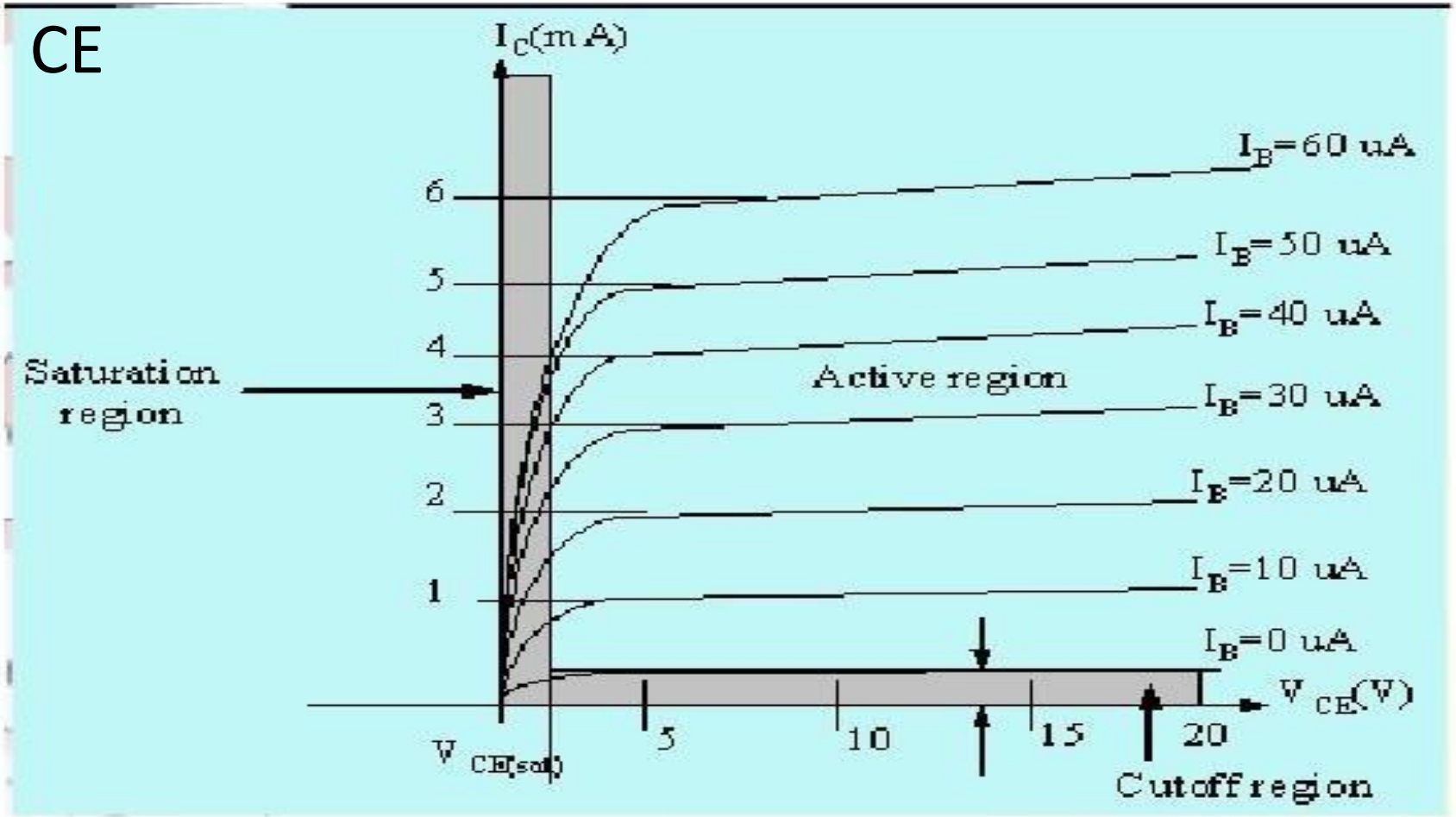
Common-Emitter Configuration

- It is called common-emitter configuration since emitter is common or reference to both input and output terminals.

  -emitter is usually the terminal closest to or at ground potential.
- Almost amplifier design is using connection of CE due to the high gain for current and voltage.
- Two set of characteristics are necessary to describe the behavior for CE

CE Configurations, Characteristics

- CE



CC Configurations, Characteristics

- For the common-collector configuration, the output characteristics are a plot of IE vs VCE for a range of values of IB.

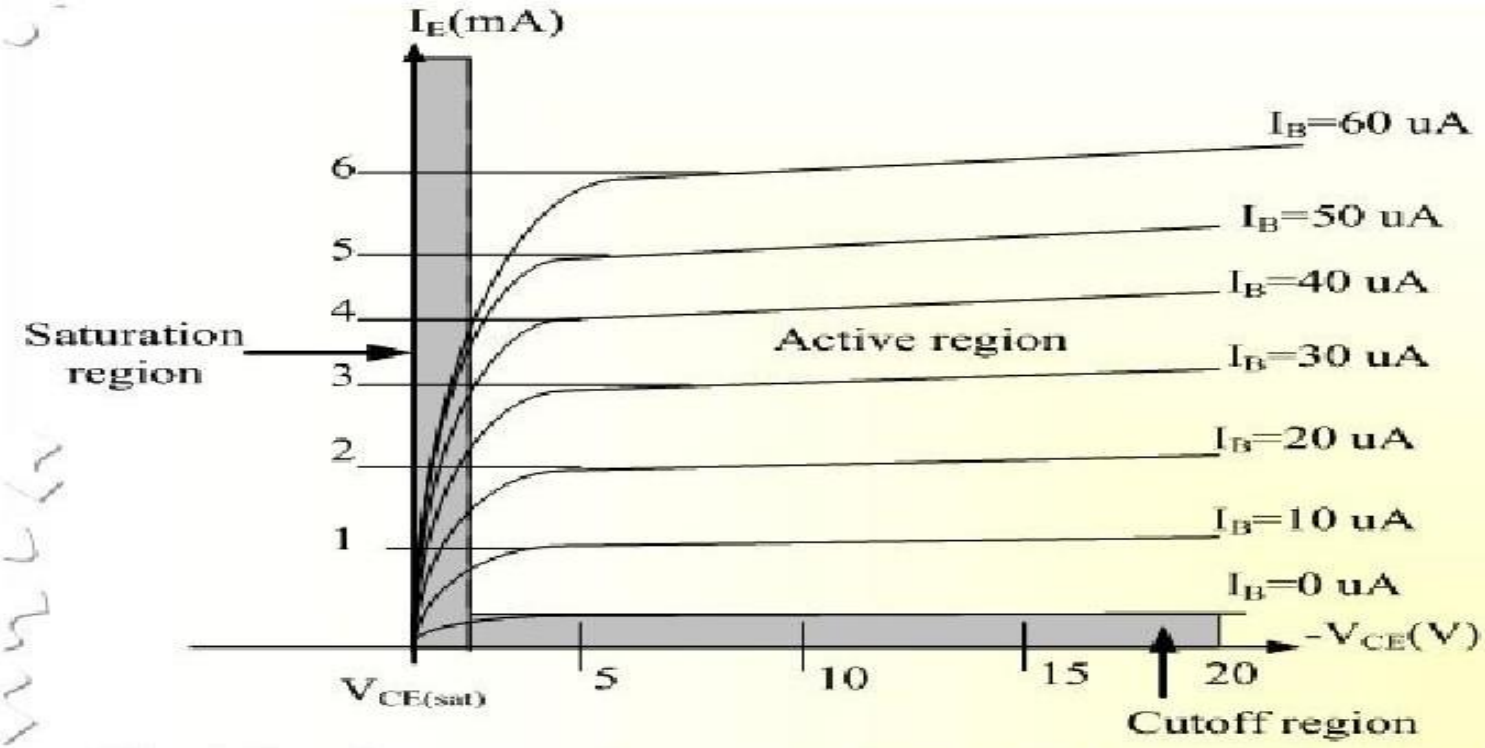
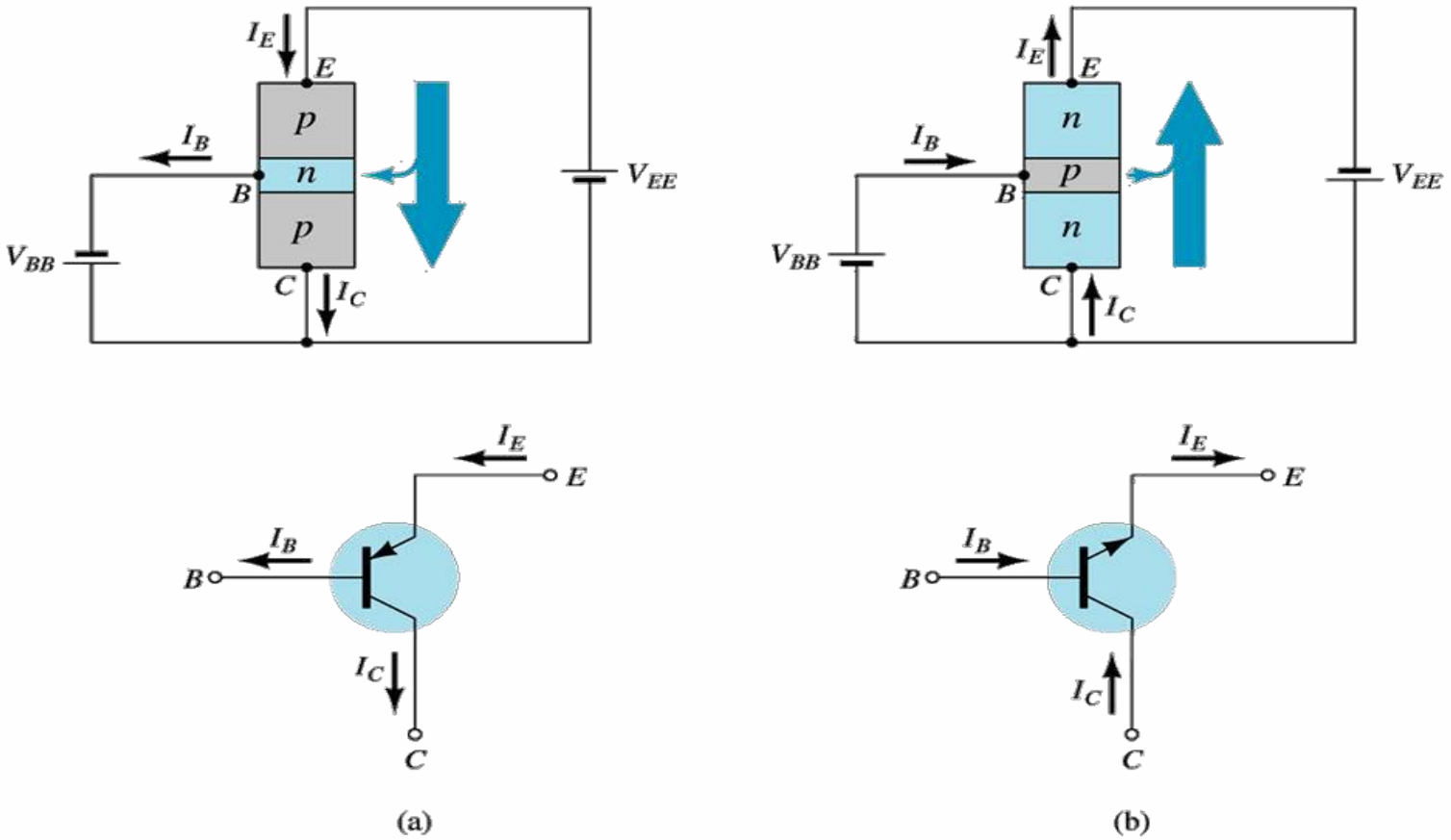


Fig 4.9 : Output characteristic in CC configuration for npn transistor

BJT specifications, Applications Amplifier



Notation and symbols used with the common-collector configuration: (a) pnp transistor ; (b) npn transistor.

- For the common-collector configuration, the output characteristics are a plot of IE vs VCE for a range of values of IB.

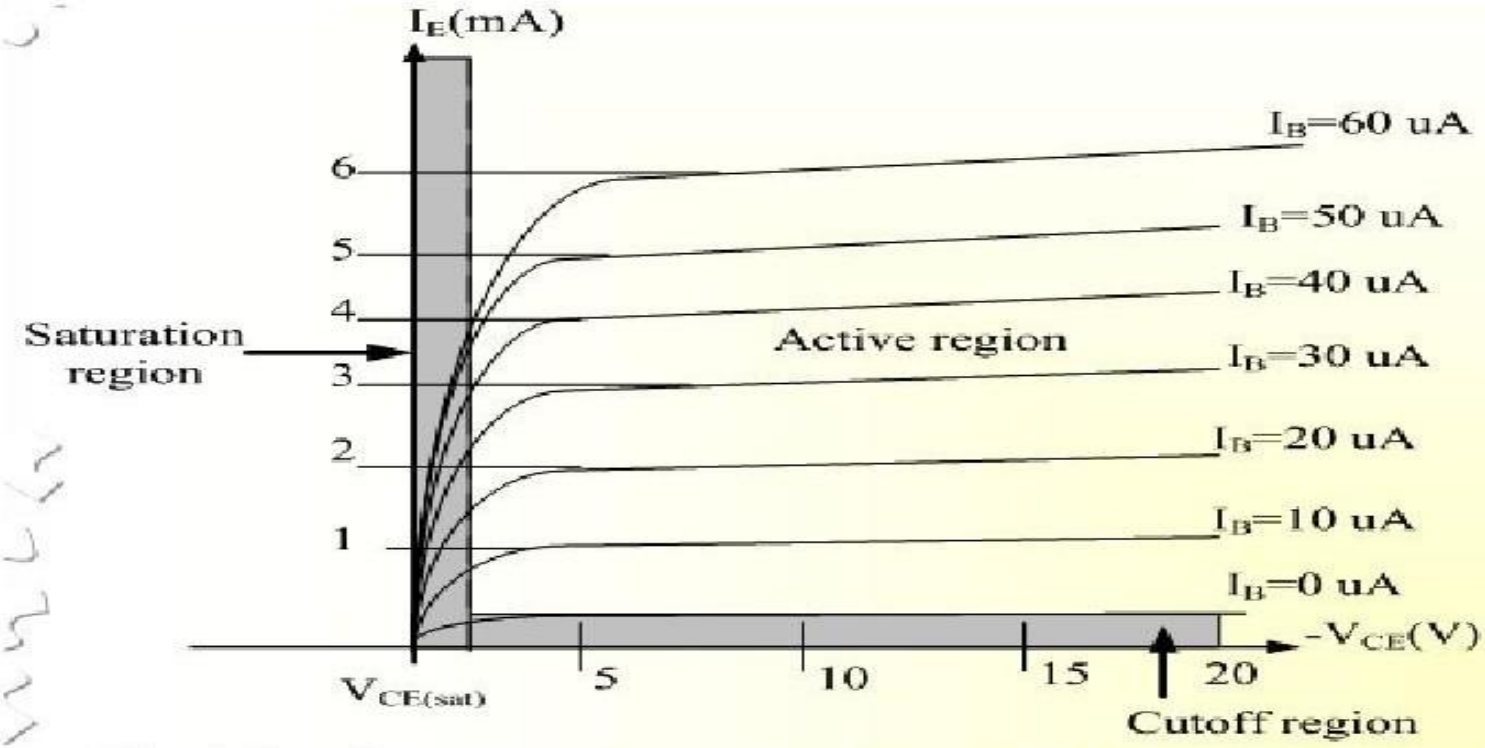
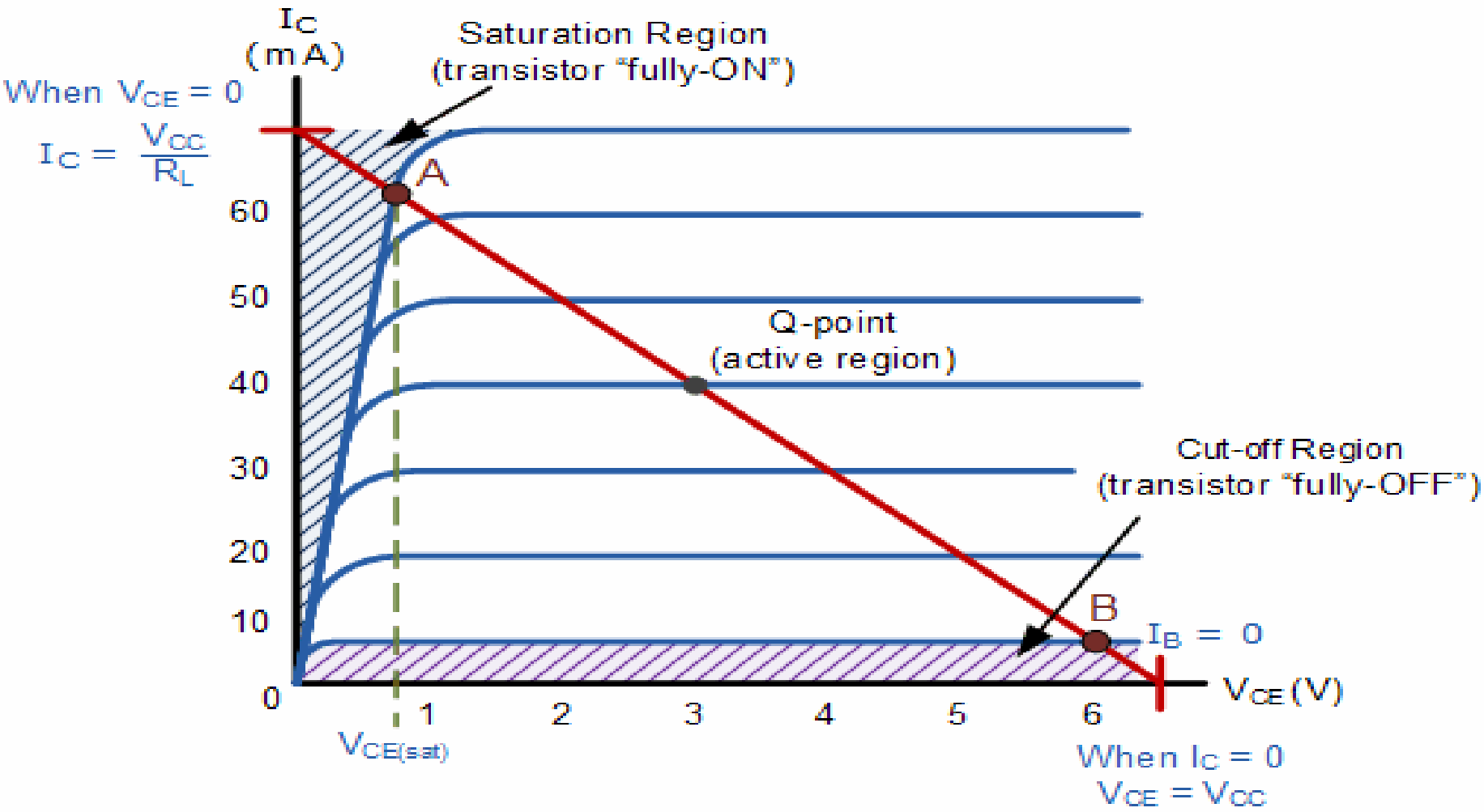


Fig 4.9 : Output characteristic in CC configuration for npn transistor

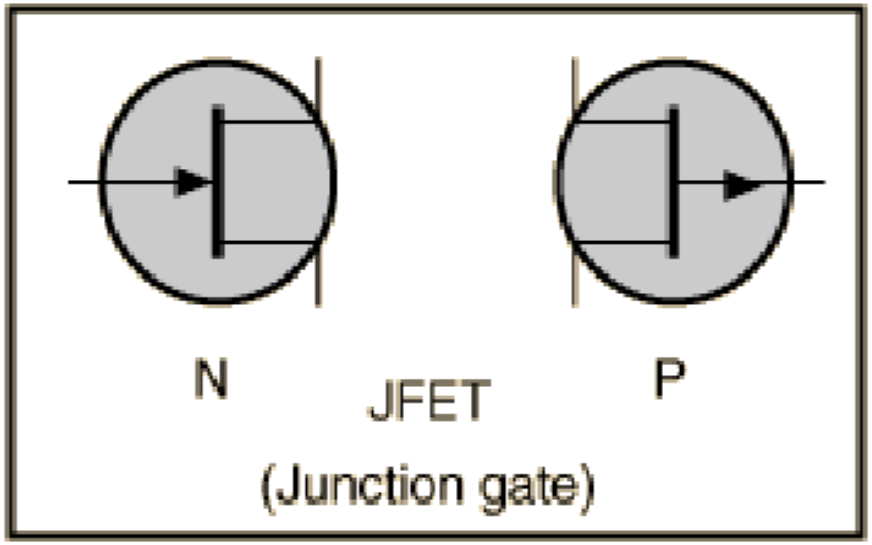
TRANSISTOR AS A SWITCH



Types of FET, FET construction, symbol

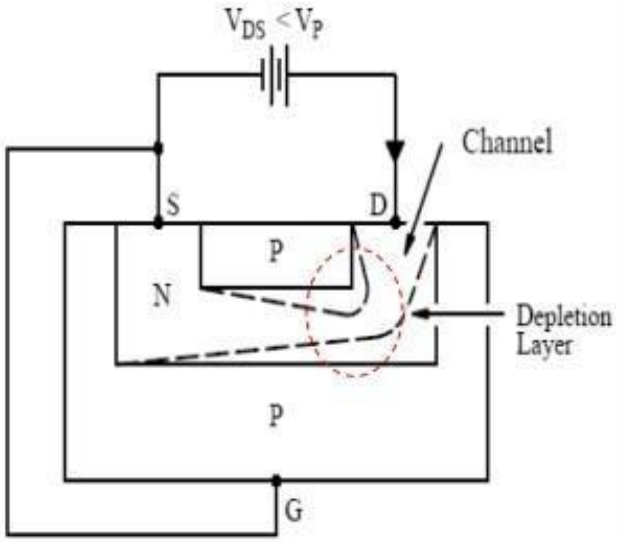
The family of FET devices may be divided into :

- Junction FET
- Depletion Mode MOSFET
- Enhancement Mode MOSFET



FET principle of operation

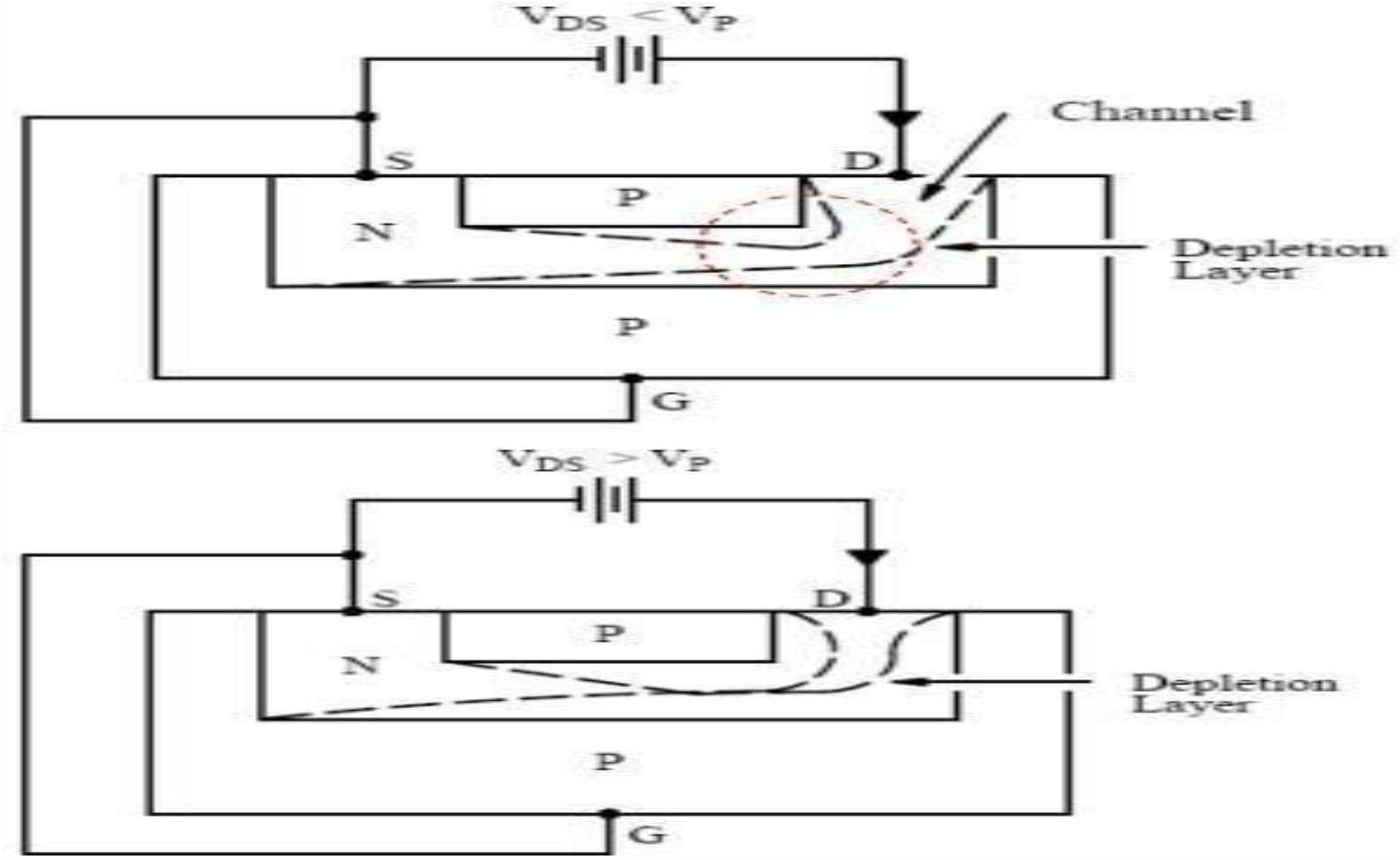
How JFET Function



- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a depletion layer, where almost all the electrons

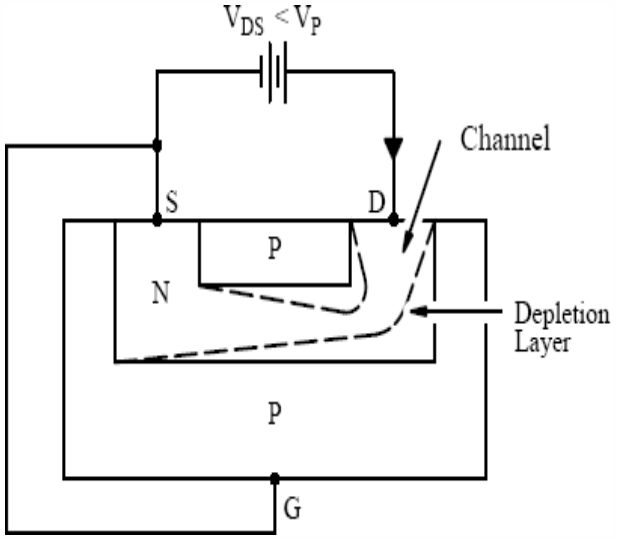
FET principle of operation

How JFET Funcion

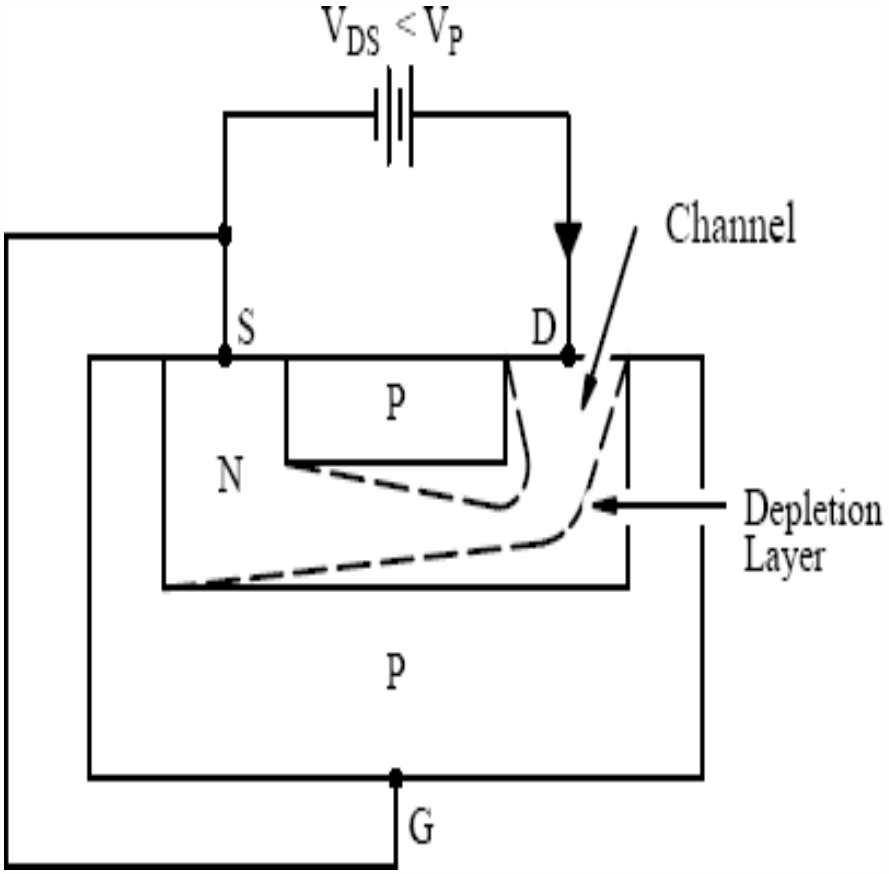


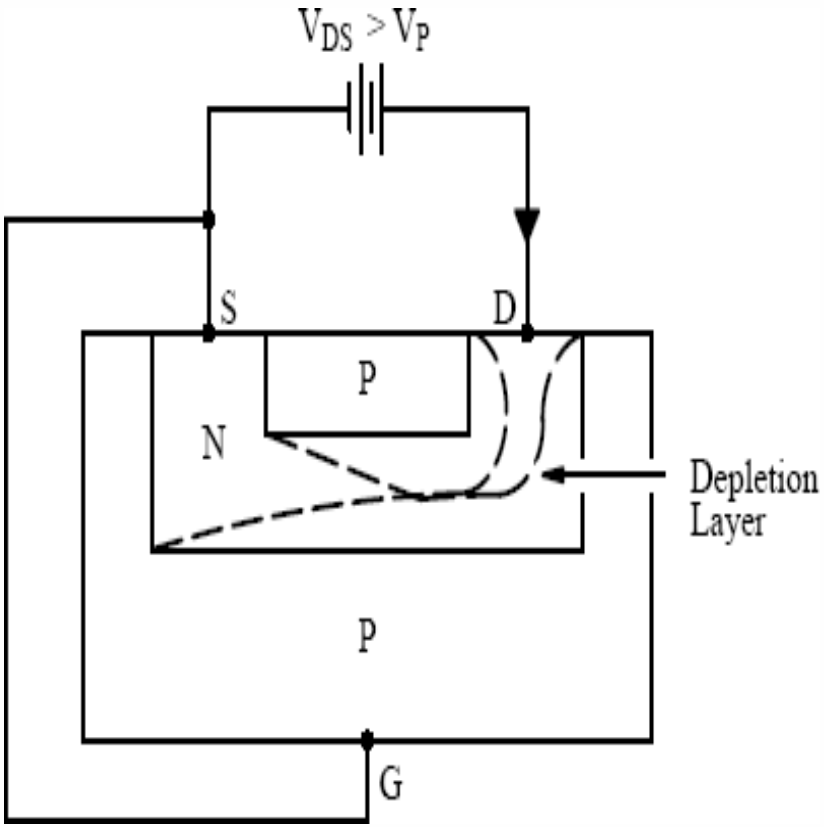
FET principle of operation

- The gate is connected to the source.
- Since the pn junction is reverse-biased, little current will flow in the gate connection.
- The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away.
- The most depleted portion is in the high field between the G and the D, and the least-depleted area is between the G and the S.



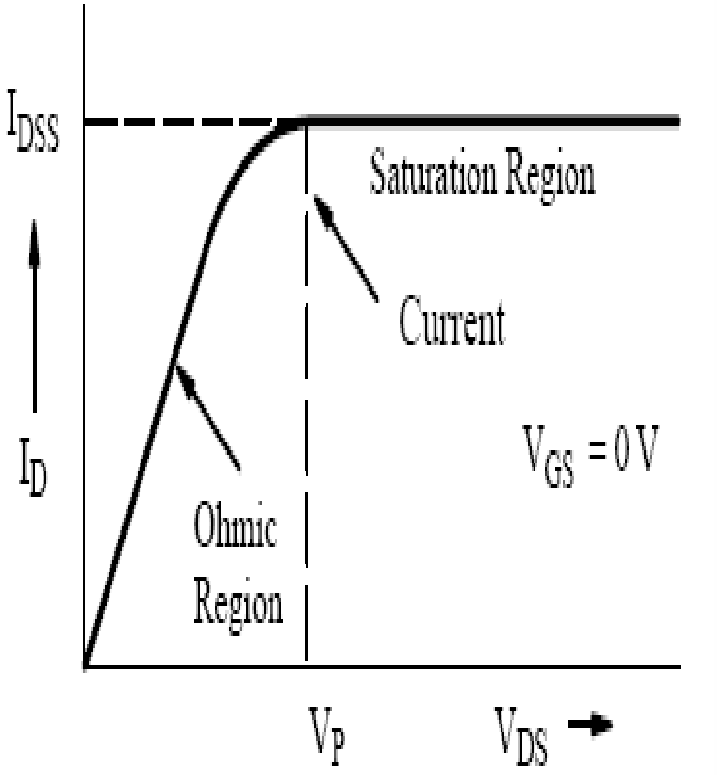
FET principle of operation





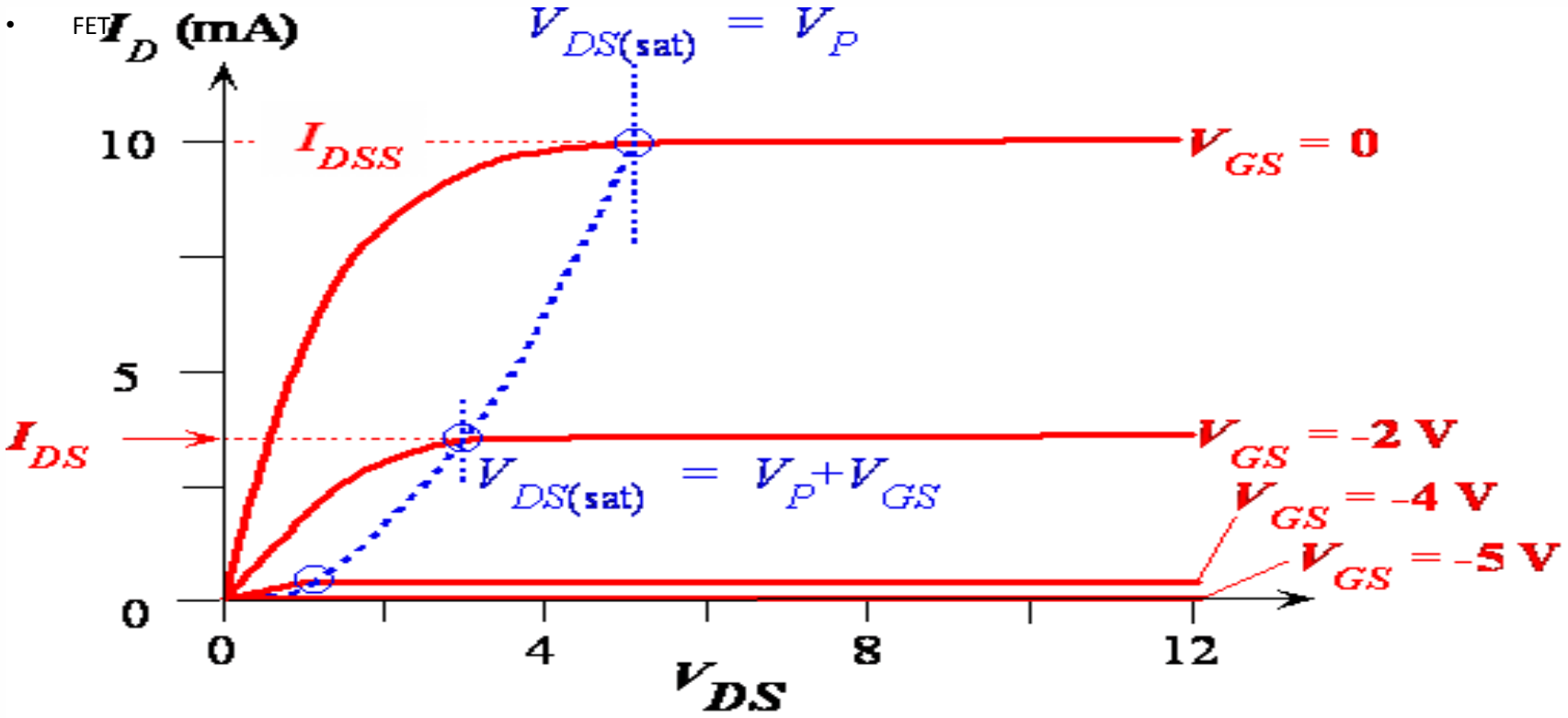
FET V-I characteristics

- The output characteristics of an n-channel JFET with the gate short-circuited to the source.
- The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases.
- The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off.
- The physical meaning of this term leads to one definition of pinch-off voltage, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



FET V-I characteristics

- FET



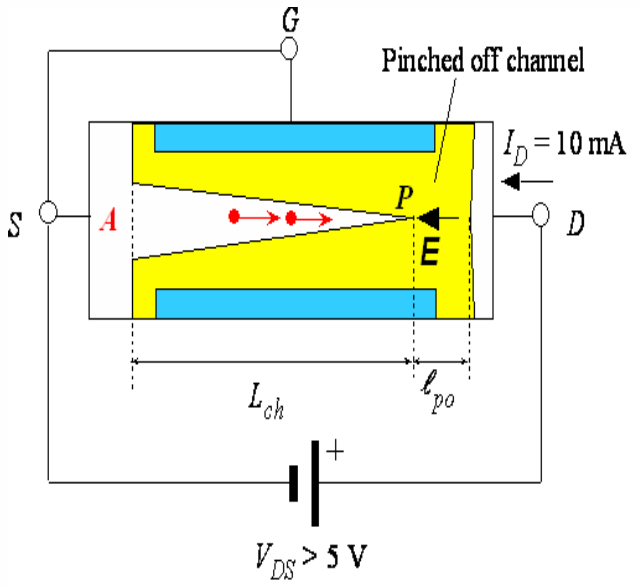
Typical I_D vs V_{DS} characteristics of a JFET for various fixed gate voltages V_{GS}.

FET V-I characteristics

- Beyond $V_{DS} = V_P$, there is a short pinch- off channel of length, ℓ_{po}.
- As V_{DS} increases, most of additional voltage simply drops across as this region is depleted of carriers and hence highly resistive.
- Voltage drop across channel length, L_{ch} remain as V_P.
- Beyond pinch-off then

$$I_D = V_P/R_{AP}$$

($V_{DS}>V_P$).



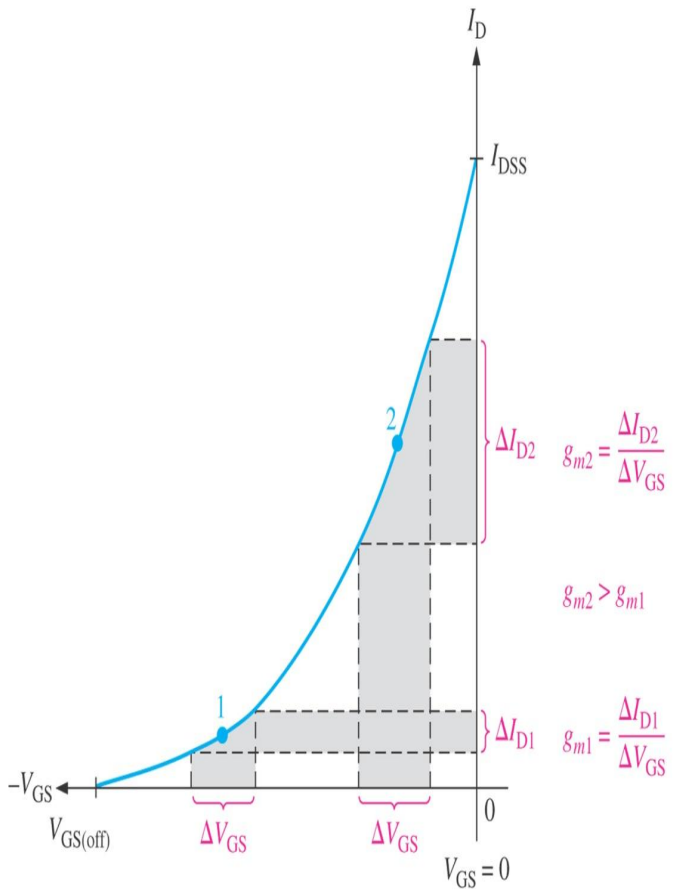
The pinched-off channel and conduction for $V_{DS} > V_P$ (=5 V).

FET parameters

Forward transfer conductance, g_m of JFETs is the changes in I_D based on changes in V_{GS} with V_{DS} is constant**.**

Forward transfer conductance referred to as $g_m = \Delta I_D / \Delta V_{GS}$. Unit is Siemens (s)

The value is larger at the top of the curve (near V_{GS}=0) but become smaller as you increase V_{GS} (near $V_{GS(off)}$).



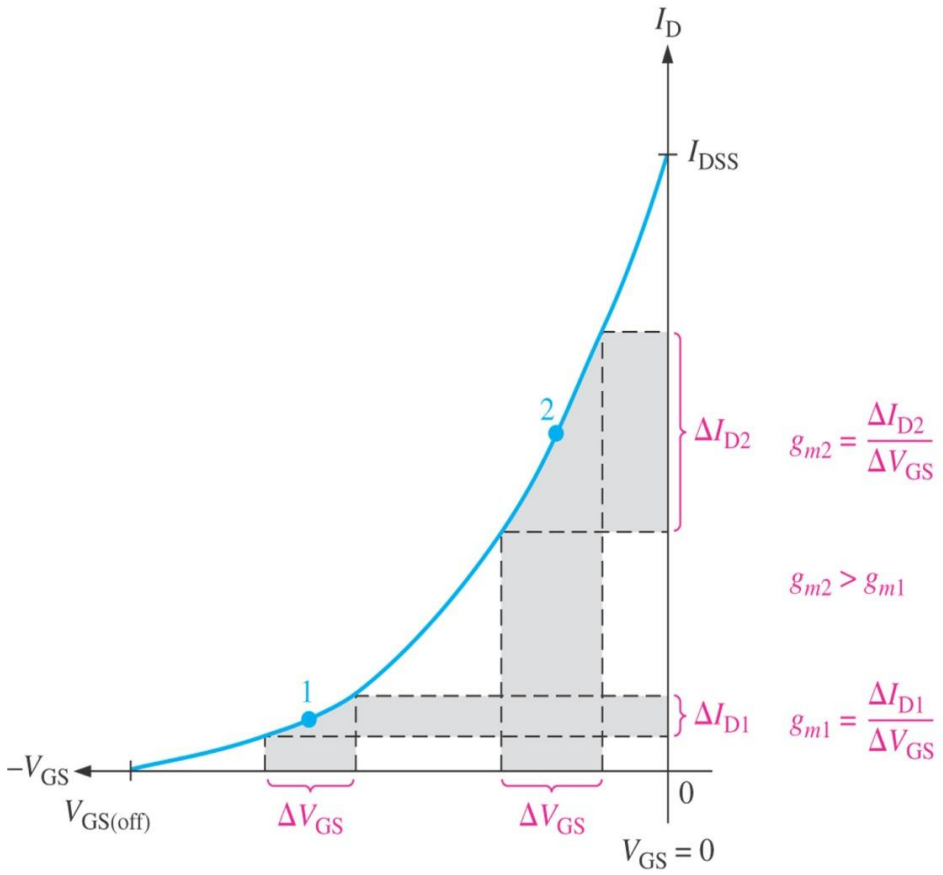
FET parameters

At V_{GS} =0, the parameter is known as minimum transfer conductance, g_{mo} and can be calculated using this equation:

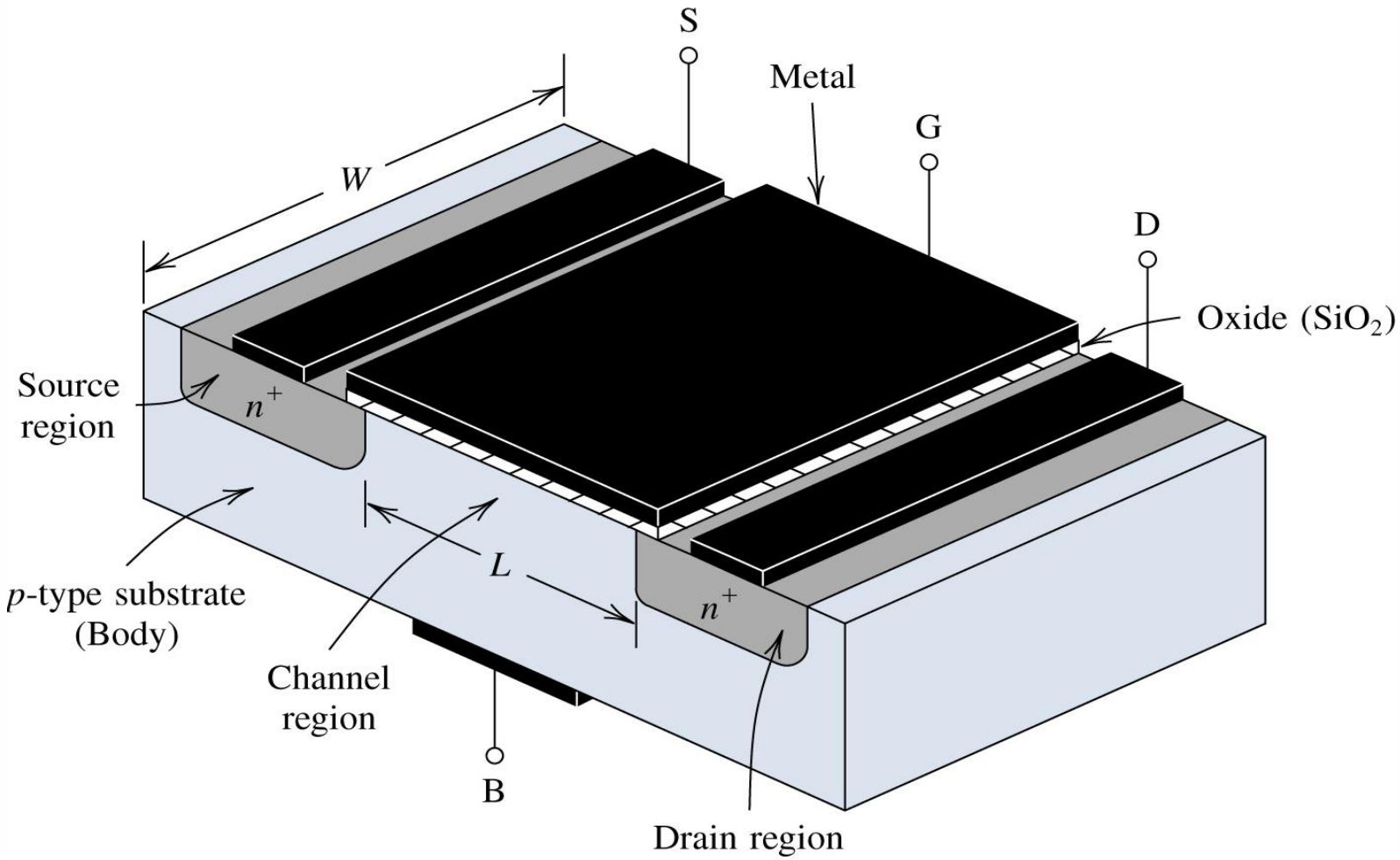
$g_{mo} = 2I_{DSS}/|V_{GS(off)}|$ and

$g_m = g_{mo}(1 - V_{GS}/V_{GS(off)})$

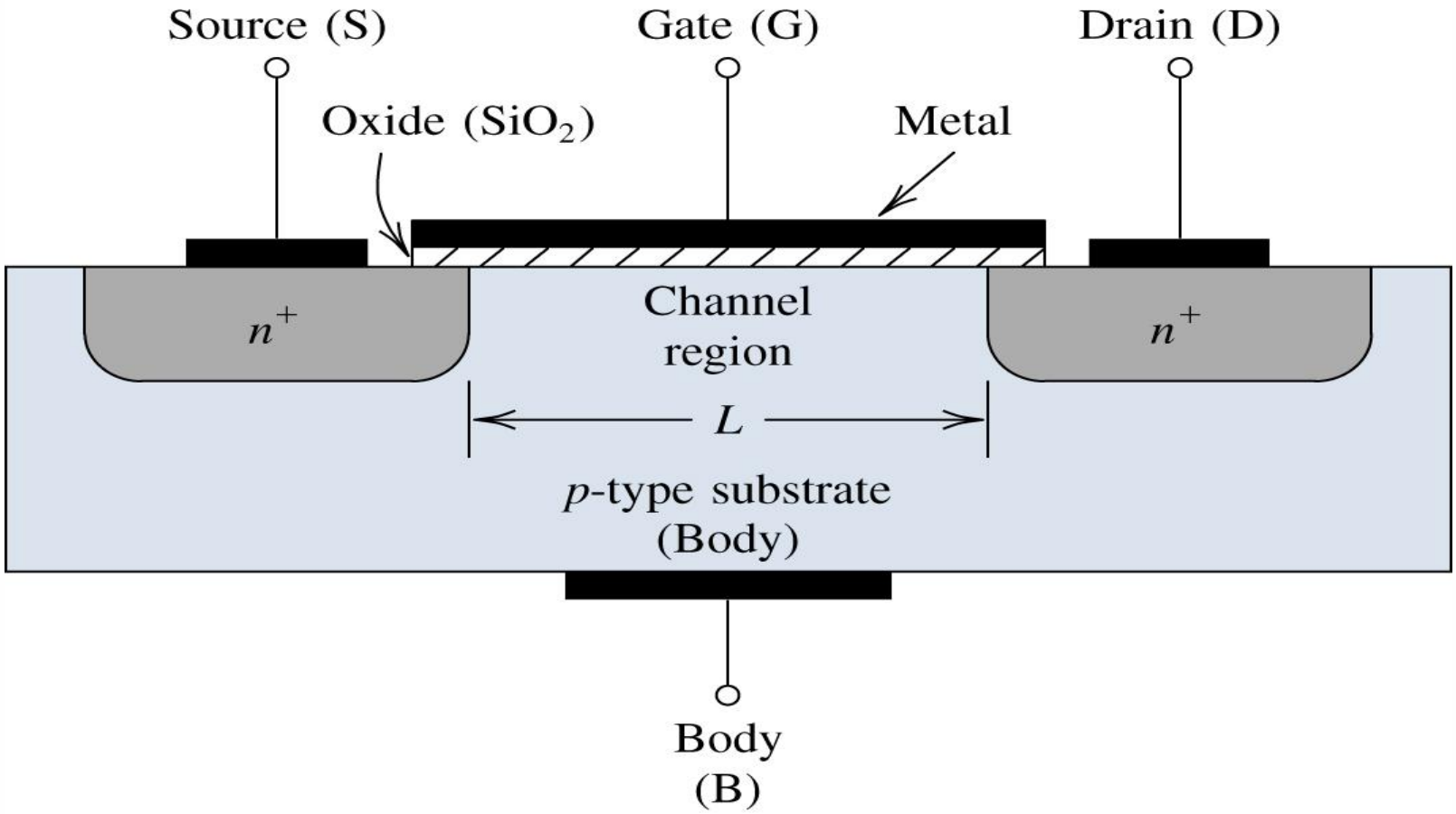
g_{mo} can be read from the datasheet as g_{fs} or y_{fs} and sometimes written as Forward Transfer Admittance.



MOSFET construction and operation

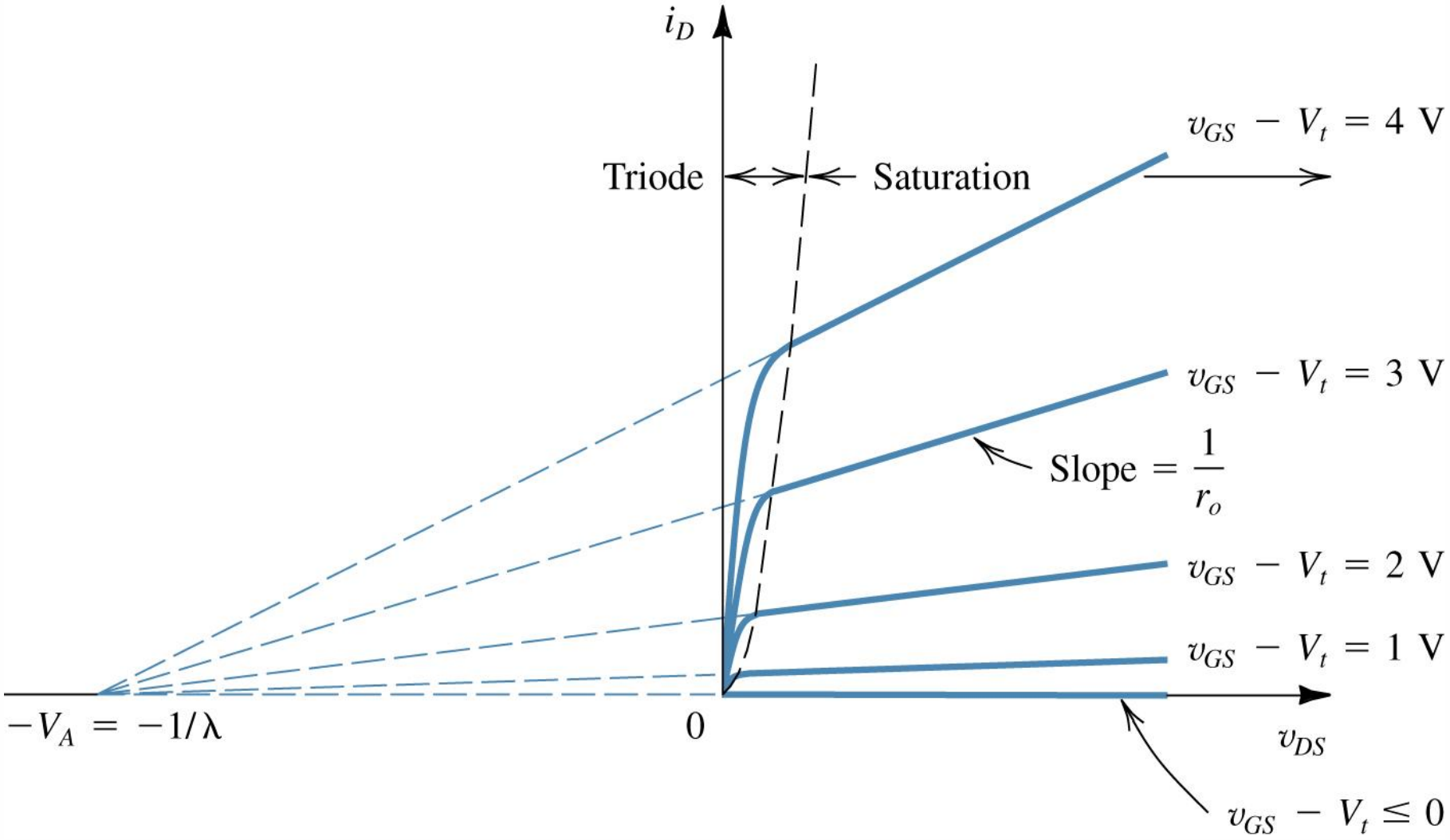


MOSFET construction and operation

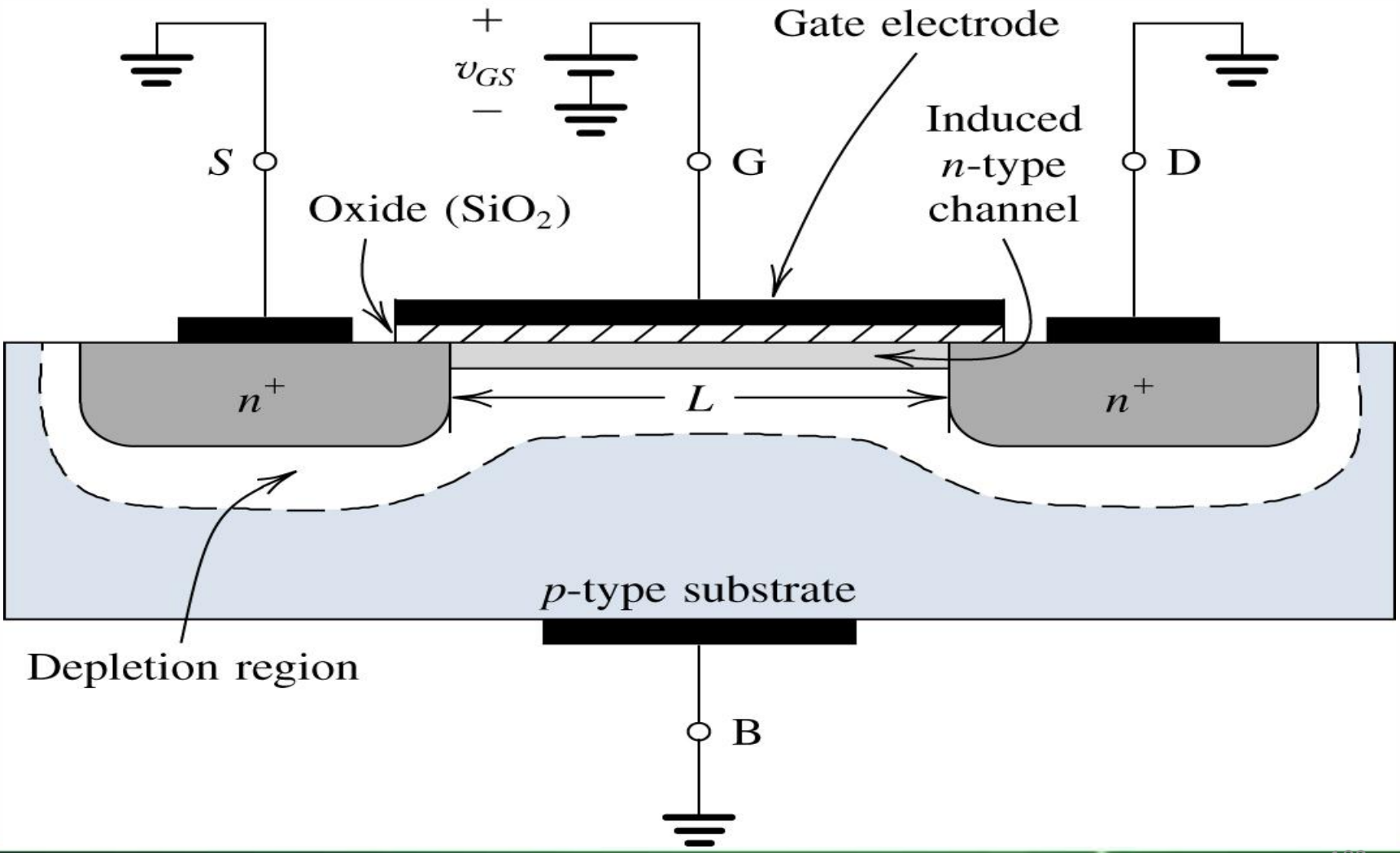


(b)

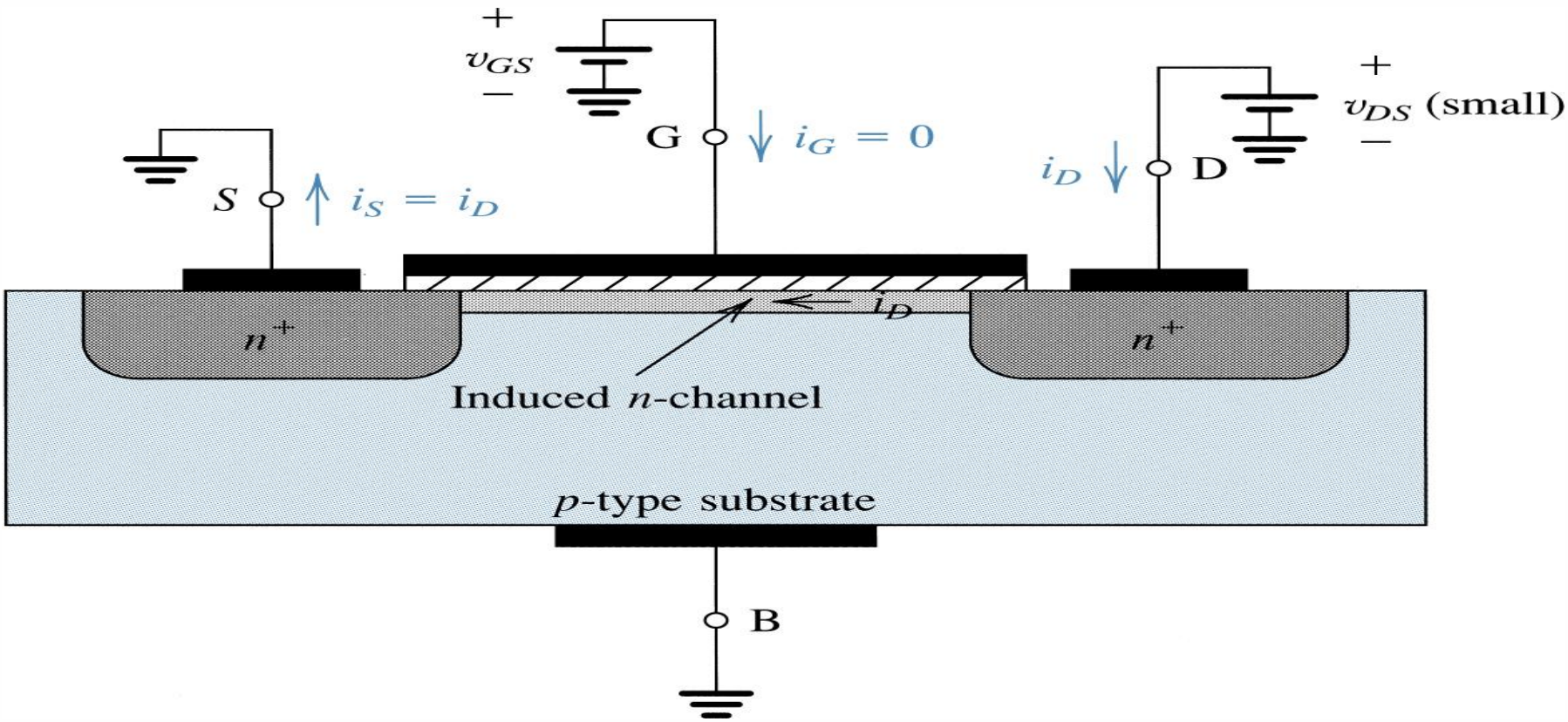
MOSFET construction and operation



MOSFET construction and operation



MOSFET construction and operation



An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a conductance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and this i_D is proportional to $(v_{GS} - Vt)$ v_{DS}. Note that the depletion region is not shown (for simplicity).

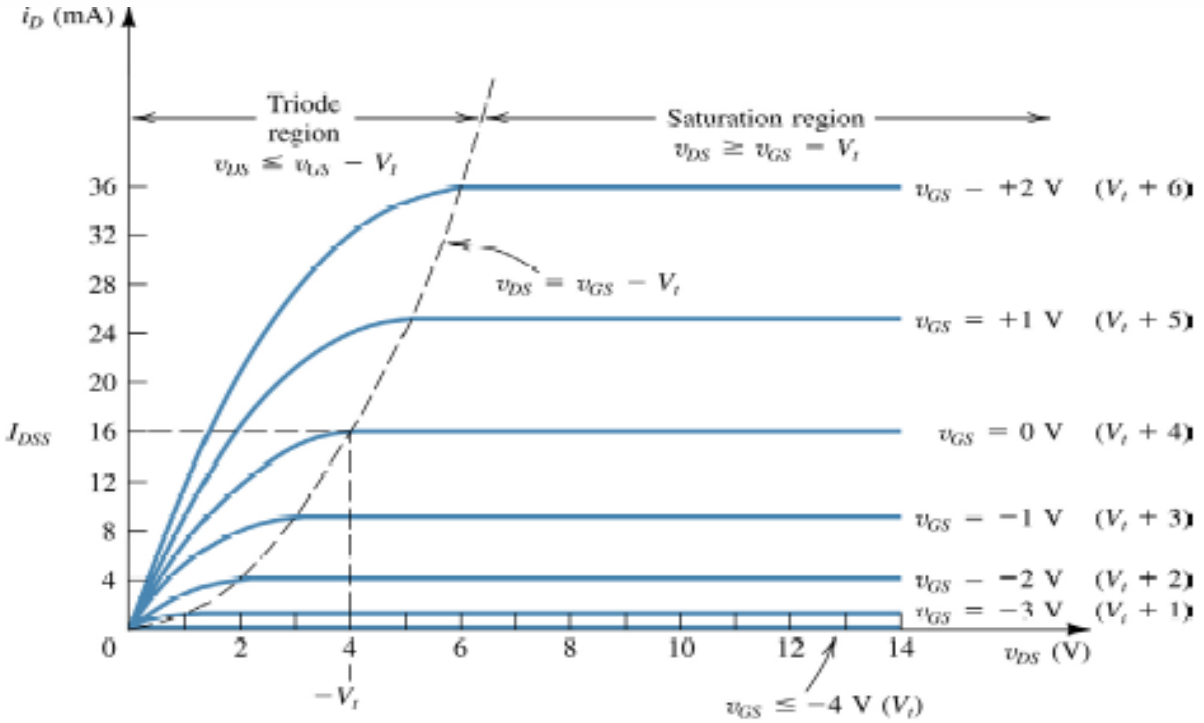
MOSFET construction and operation

MOSFET
Depletion Type

For the transistor to operate in the saturation region, $v_{DS} > |Vt|$.

For $v_{GS} = 0$, the drain current is denoted as I_{DSS} and is given by,

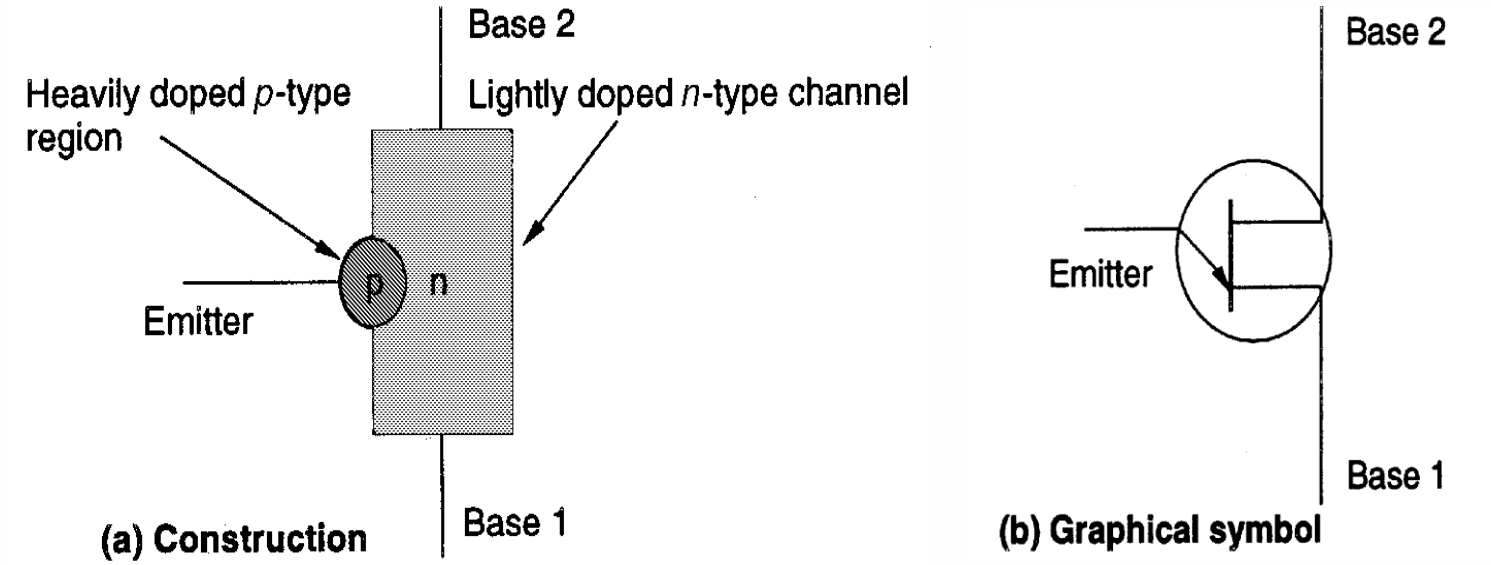
$$I_{DSS} = \frac{1}{2}k'(W/L)(V_t)^2$$



The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which $V_t = -4$ V and $k'_n(W/L) = 2$ mA/V²: the i_D - v_{GS} characteristic in saturation.

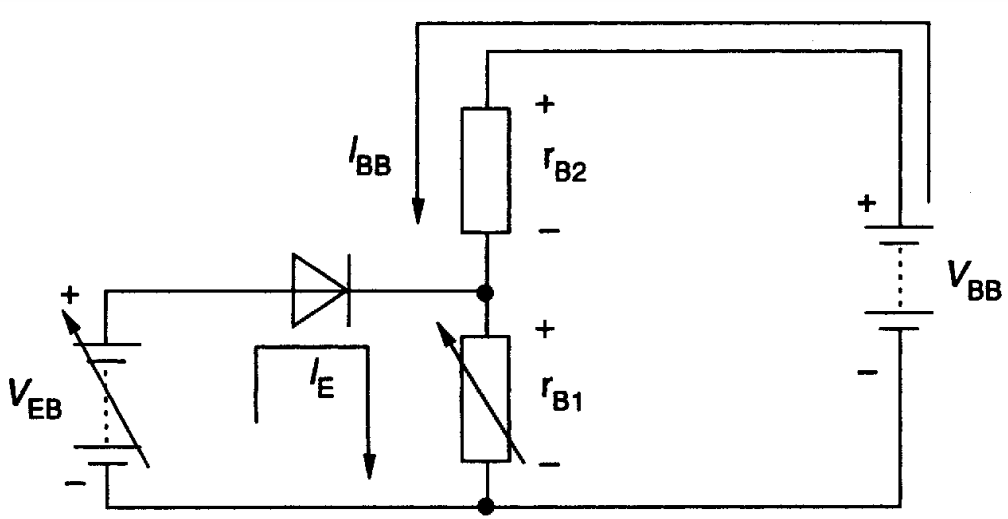
UJT: Symbol Principle of operation

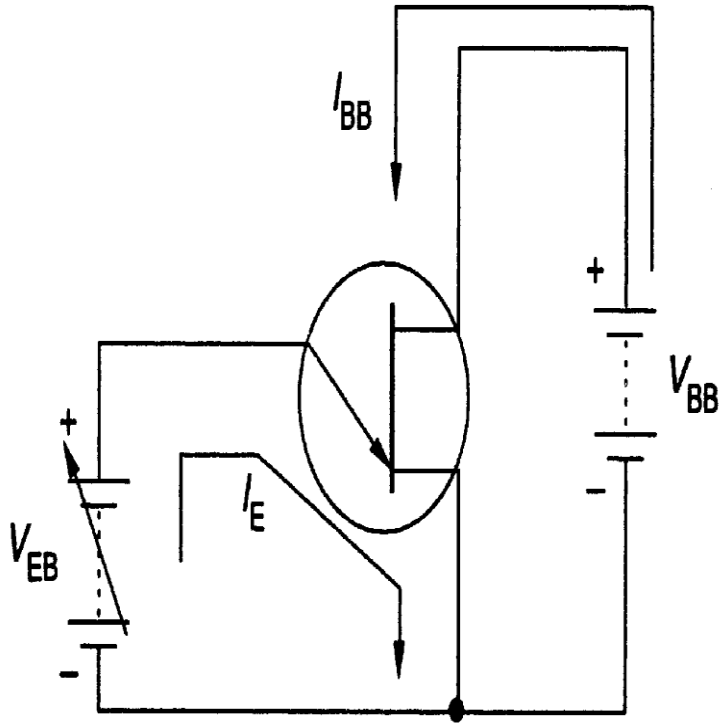
UJT construction and symbol



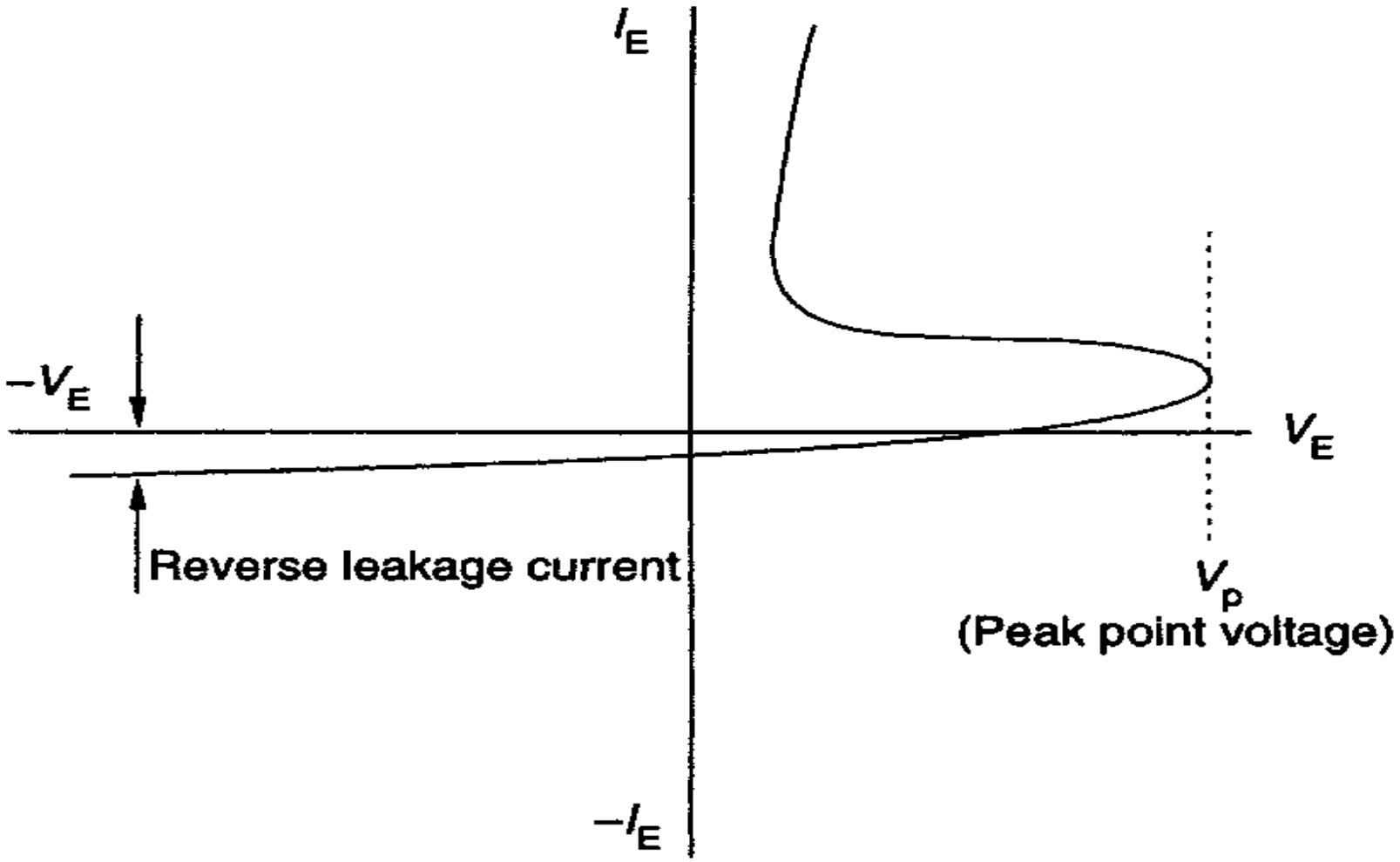
UJT: Symbol Principle of operation

UJT emitter current



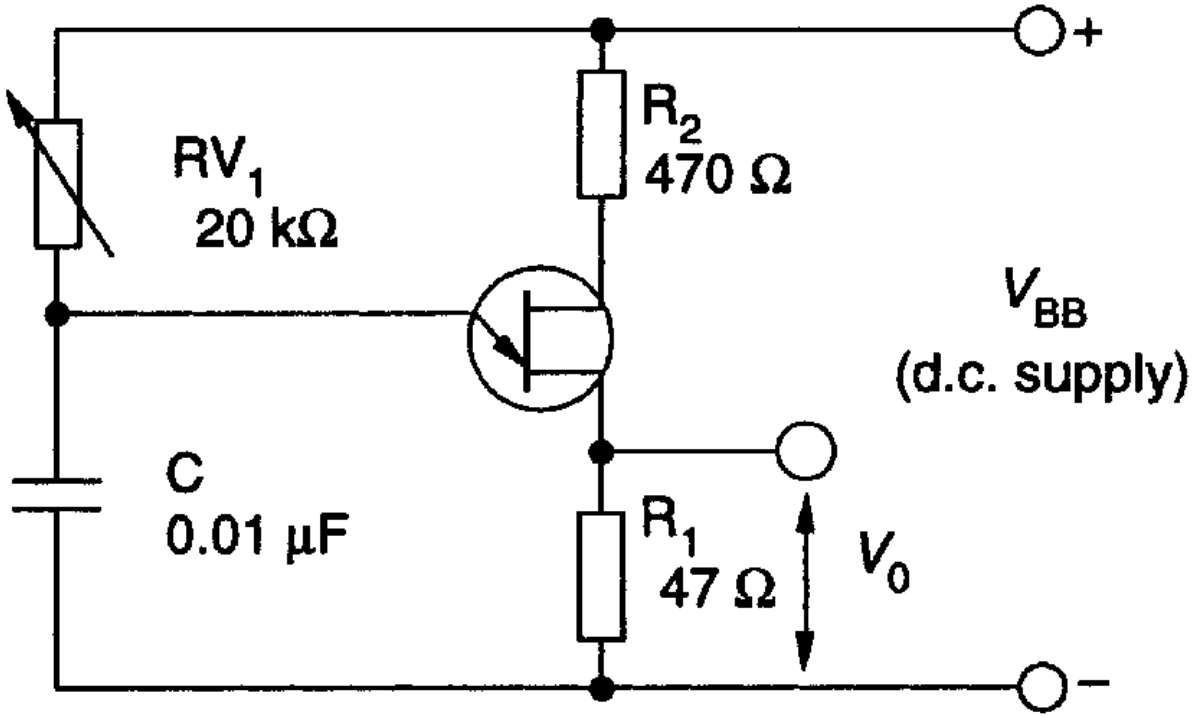


UJT Characteristics and applications



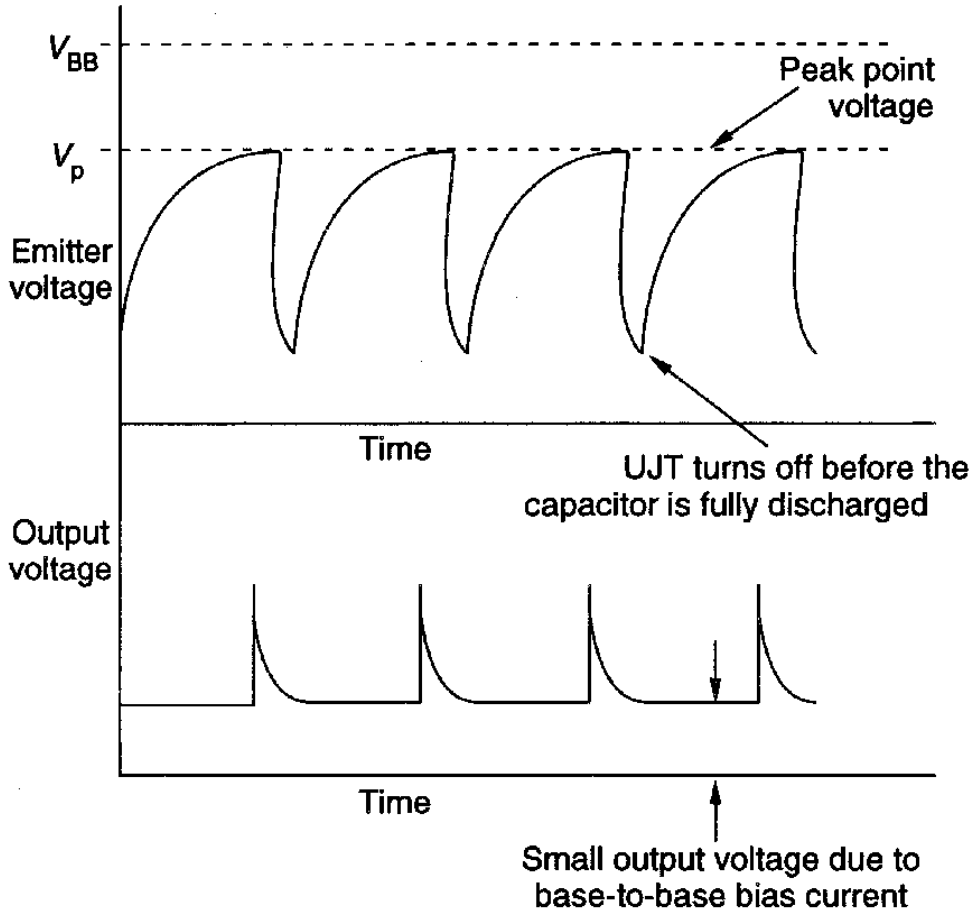
UJT Characteristics and applications

UJT relaxation oscillator



UJT Characteristics and applications

Relaxation oscillator waveforms



UNIT 4

BIASING AND COMPENSATION TECHNIQUES

Transistor Biasing

Biasing

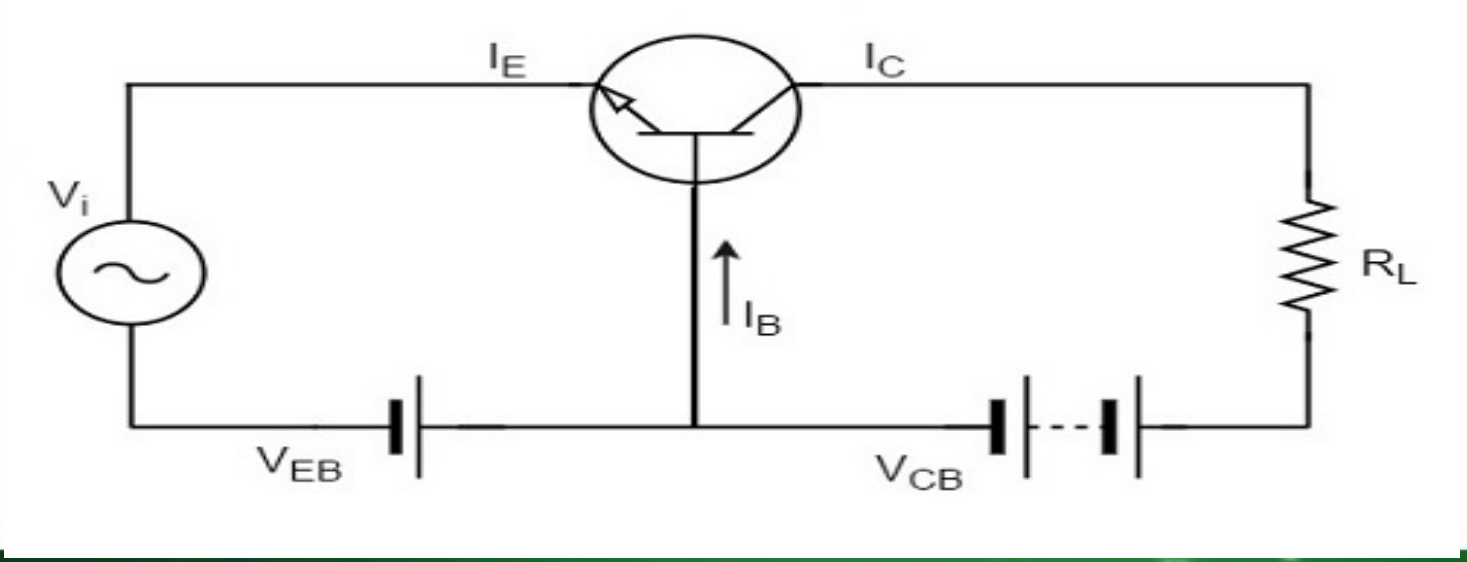
The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

- If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.
- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

Transistor Biasing(contd.)

- If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.
- For a transistor to be operated as a faithful amplifier, the operating point should be stabilized. Let us have a look at the factors that affect the stabilization of operating point.



Operating Point

- A transistors steady state of operation depends a great deal on its base current, collector voltage, and collector current and therefore, if a transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point.

- Establishing the correct operating point requires the proper selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions.

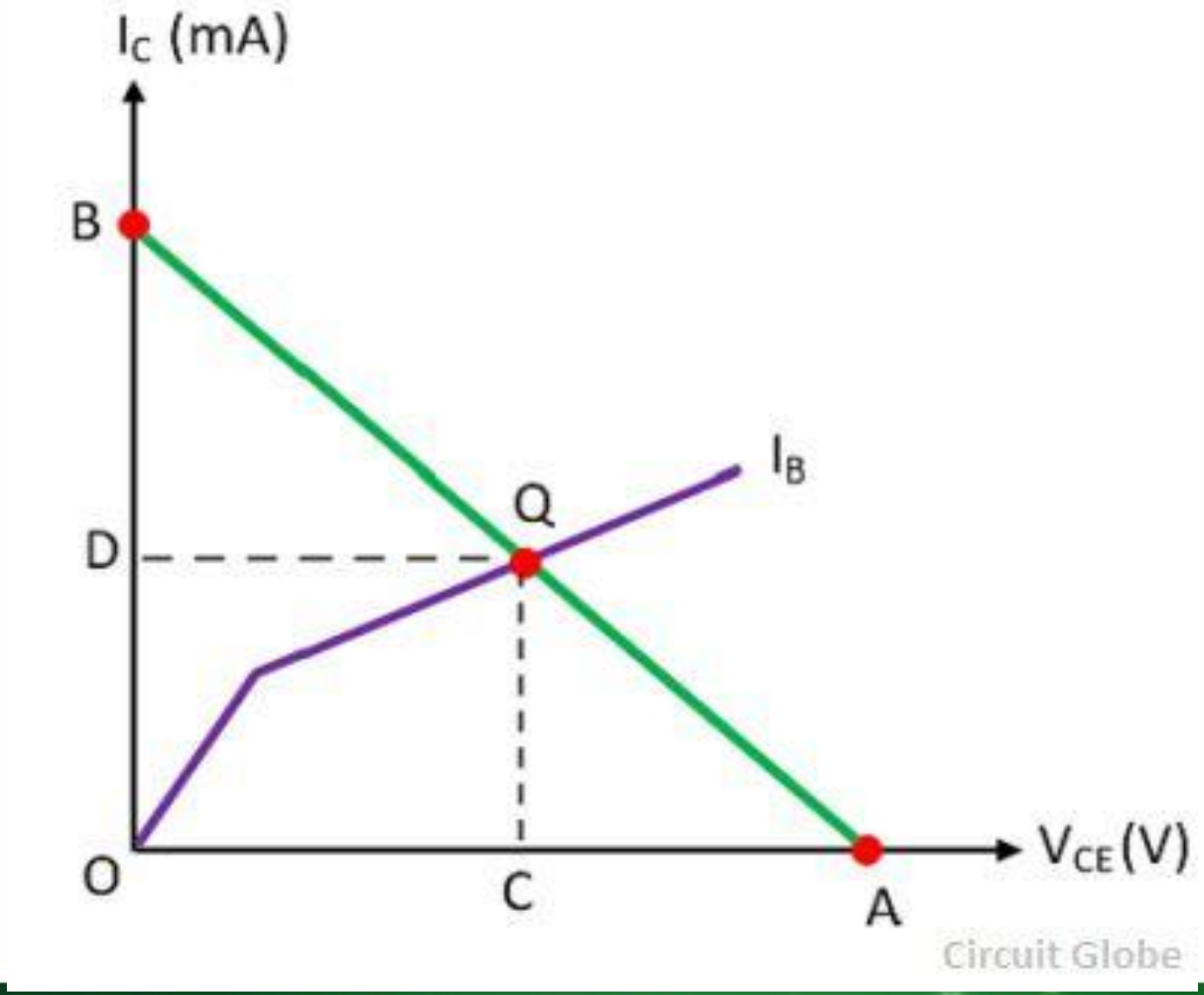
- The correct biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation with respect to it being either “fully-ON” or “fully-OFF” along its load line. This central operating point is called the “Quiescent Operating Point”, or **Q-point** for short.

Operating Point(contd.)

Factors affecting the operating point

- The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.
- As temperature increases, the values of I_{CE}, β, V_{BE} gets affected.
- I_{CBO} gets doubled (for every 10^o rise)
- V_{BE} decreases by 2.5mv (for every 1^o rise)
- So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

Operating Point(contd.)



DC Load line

DC load line

- The dc load line is the locus of I_C and V_{CE} at which BJT remains in active region i.e. it represents all the possible combinations of I_C and V_{CE} for a given amplifier.

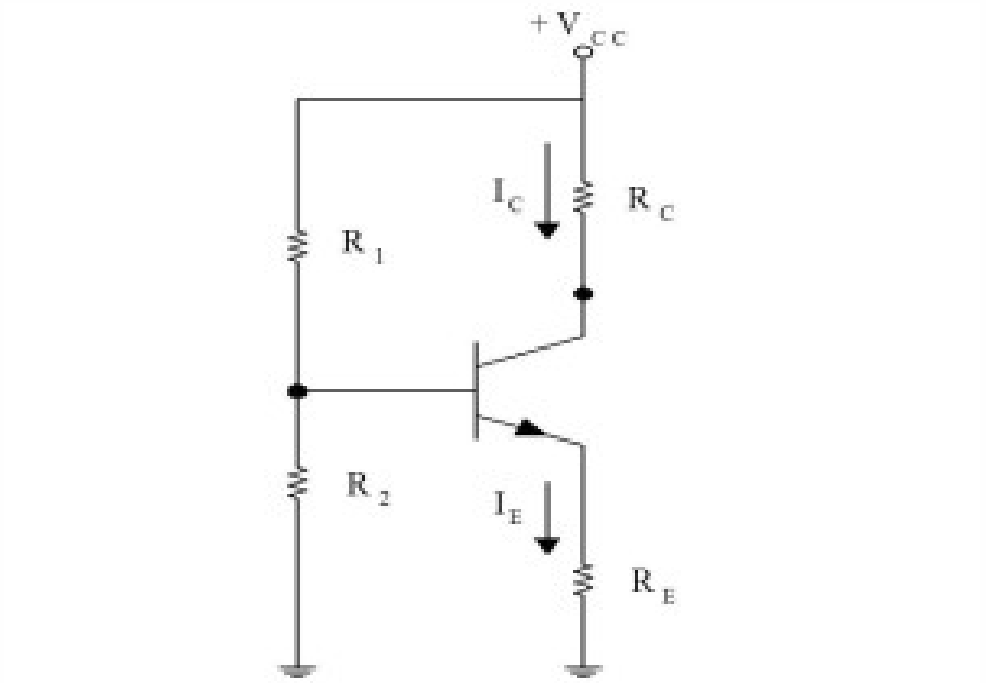
Procedure to draw DC load line

- To draw DC load line of a transistor we need to find the saturation current and cutoff voltage. The saturation current is the maximum possible current through the transistor and occurs at the point where the voltage across the collector is minimum. The cutoff voltage is the maximum possible voltage across the collector and occurs at zero collector current.
- $V_{ce} = V_{cc} - R_c * I_c$

DC Load line(contd.)

- From the DC equivalent circuit by applying Kirchoff's voltage Law in collector loop in

$$V_{ce} = V_{cc} - R_c * I_c$$

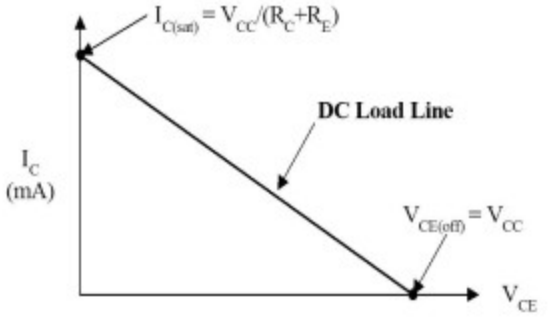


DC Load line(contd.)

Cutoff point : To find the cutoff point equate the collector current to zero(actually in cutoff the collector current is I_{CO} which will be of micro amperes order and hence can be assumed to be zero). In equation 1 equating I_c to zero the cutoff point is (V_{cc}, 0).

Saturation point : To find the saturation point equate the collector voltage to zero(actually in saturation the collector voltage will be around o.2 Volts which is small and hence can be assumed to be zero). In equation 1 equating V_{ce} to zero the cutoff point is (0, V_{cc}/R_c).

(V_{cc}, 0) is cut off point where transistor enters in to cut off region from active region and (0, V_{cc}/R_c) is saturation point where the transistor enters saturation region.



AC Load line

AC load line

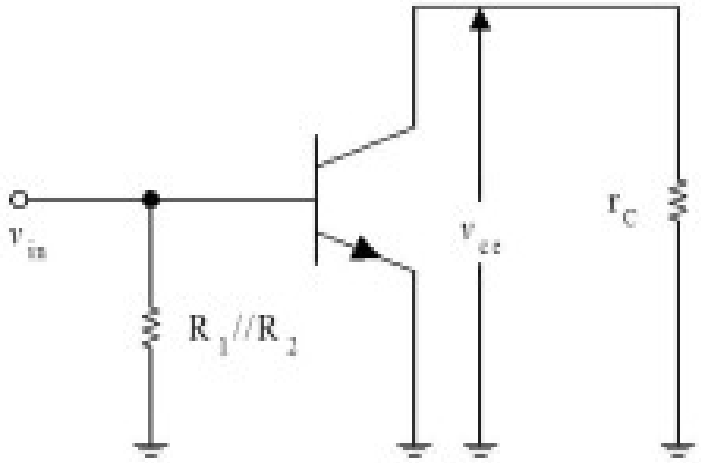
- DC load line analysis gives the variation of collector currents and voltage for static situation of Zero AC voltage. The ac load line tells you the maximum possible output voltage swing for a given common-emitter amplifier i.e. the ac load line will tell you the maximum possible peak-to-peak output voltage $V_{ce(cut\ off)}$ from a given amplifier.

- For AC input signal frequencies the biasing capacitors are chosen such that they acts as short circuits and as open circuits for DC voltages. Hence the AC signal equivalent circuit is shown in the figure below along with the AC load line

AC Load line(contd.)

- From the AC equivalent circuit we will get

$$V_{ce} = (R_c//R_l)*I_c$$

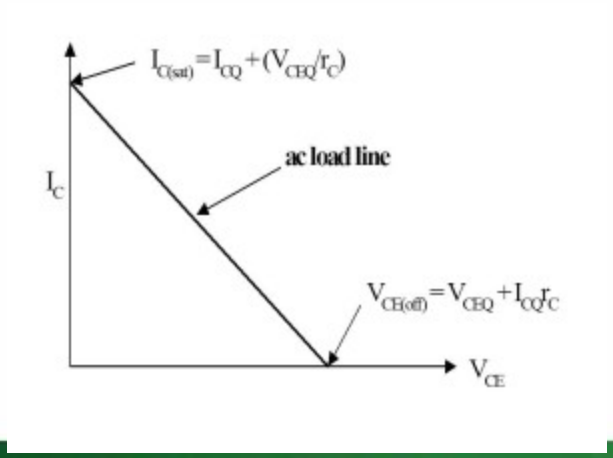


$$r_C = R_C//R_L$$

AC Load line(contd.)

- The AC output V_{ce} can have at most V_{ceq} (since normally the quiescent point is chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles i.e $V_{max} = + V_{ceq}$ and $V_{min} = -V_{ceq}$ so that the transistor stays in active region for entire input signal excursion), hence the maximum current for that corresponding V_{ceq} is $V_{ceq} / (R_c//R_l)$. Also output collector current can be at most I_{cq} hence the maximum voltage for that corresponding I_{cq} is $I_{cq}*(R_c//R_l)$. Hence by adding quiescent currents the end points of AC load line are

$$I_{c(sa)t} = I_{cq} + V_{ceq}/(R_c//R_l) \text{ and } V_{ce(off)} = V_{ceq} + I_{cq}*(R_c//R_l)$$



Types of biasing circuits

Types of biasing circuits

- Fixed bias
- Collector-to-base bias
- Fixed bias with emitter resistor
- Voltage divider bias or potential divider
- Emitter bias

Bias stabilization.

- A transistor can work as amplifier, only if the dc/ac voltages and currents in the circuit are suitably fixed. The operating point or **bias** point or quiescent point(or simply Q-point) is the voltage or current which, when applied to a device, causes it to operate in a certain desired fashion. Need for **bias stabilization**.

Need for BIAS STABILIZATION

- After fixing the operating point suitably, it should remains there only. But there are two reasons for the operating point to shift.
- The transistor parameters such as VBE & β changes from device to device
- Transistor parameters are also temperature dependent. Since the collector current is Ic = β IB + (1+ β) Ico (β, IB and Ico are temperature dependent)
- β of a transistor is strongly dependent on temperature. As temp. increases, β increases

Stabilization Factors

Stability Factor

- It is understood that I_C should be kept constant in spite of variations of I_{CBO}or I_{CO}. The extent to which a biasing circuit is successful in maintaining this is measured by **Stability factor**. It denoted by **S**.

- By definition, the rate of change of collector current I_C with respect to the collector leakage current I_{CO} at constant β and I_B is called **Stability factor**.

- S=dICdICOS=dICdICO at constant I_B and β

- Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. S=1 is the ideal value.

Stabilization Factor(contd.)

- The general expression of stability factor for a CE configuration can be obtained as under.

$$I_c = \beta I_B + (1 + \beta) I_{c0}$$

- Differentiating above expression with respect to I_C, we get

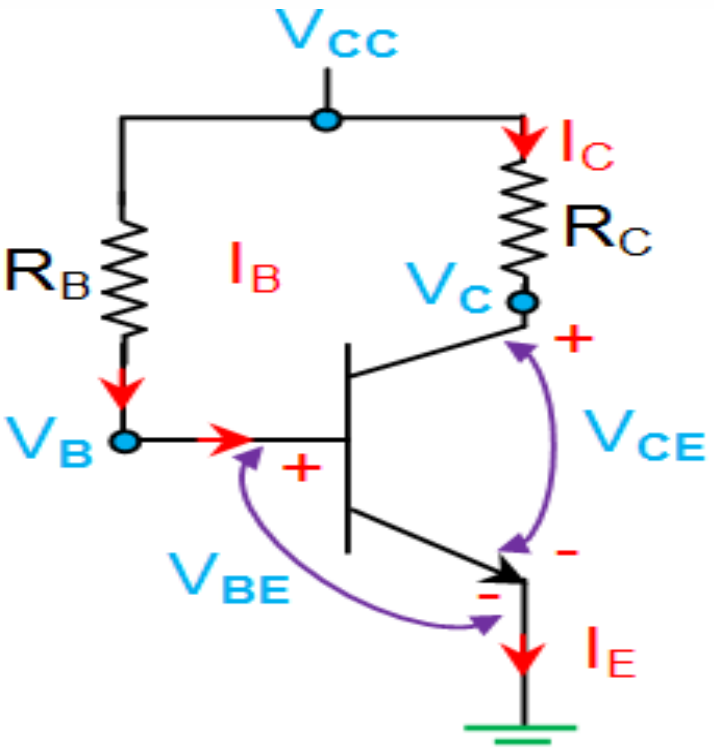
$$S = \frac{1 + \beta}{1 - \beta \frac{dIB}{dIc}}$$

- Hence the stability factor S depends on β, I_B and I_C.

Fixed Base Bias or Fixed Resistance Bias

- The biasing circuit shown by below Figure has a base resistor R_B connected between the base and the V_{CC}. Here the base-emitter junction of the transistor is forward biased by the voltage drop across R_B which is the result of I_B flowing through it. From the figure, the mathematical expression for I_B is obtained as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



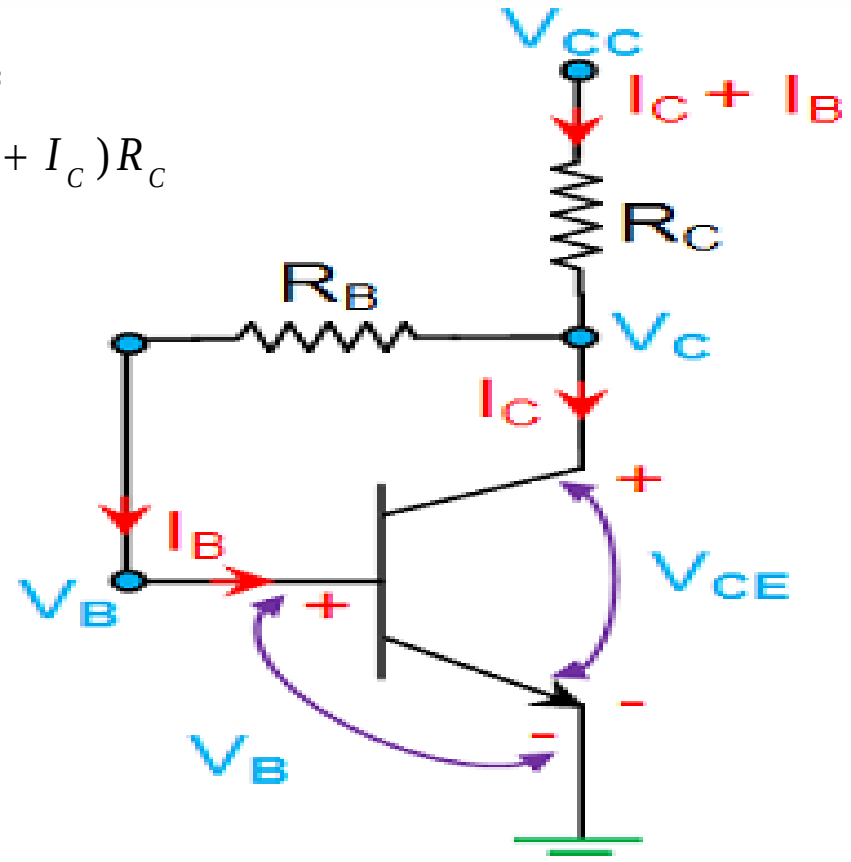
Fixed Base Bias Circuit

Collector Feedback Bias

- In this circuit , the base resistor R_B is connected across the collector and the base terminals of the transistor. This means that the base voltage, V_B and the collector voltage, V_C are inter-dependent due to the fact that

$$V_B = V_C - I_B R_B$$

$$V_C = V_{CC} - (I_B + I_C) R_C$$



Collector Feedback Bias Circuit

Collector Feedback Bias(contd.)

- From these equations, it is seen that an increase in I_C decreases V_C which results in a reduced I_B, automatically reducing I_C. This indicates that, for this type of biasing network, the Q-point (operating point) remains fixed irrespective of the variations in the load current causing the transistor to always be in its active region regardless of β value.
- Further this circuit is also referred to as self-biasing negative feedback circuit as the feedback is from output to input via R_B. This kind of relatively simple bias has a stability factor which is less than (β+1), which results in a better stability when compared to fixed bias. However the action of reducing the collector current by base current leads to a reduced amplifier gain. Here,
- other voltages and currents are expressed as

$$V_B = V_{BE}$$

$$I_C = \beta I_B$$

$$I_E \approx I_C$$

Collector Feedback Bias(contd.)

Example:

Find the required collector feedback bias resistor for an emitter current of 1 mA, a 4.7K collector load resistor, and a transistor with β=100 . Find the collector voltage V_C. It should be approximately midway between V_{CC} and ground.

$$\beta = 100 \qquad V_{CC} = 10V \qquad I_C \approx I_E = 1ma \qquad R_C = 4.7k$$

$$R_B = \beta\left[\frac{V_{CC} - V_{BE}}{I_E} - R_C\right] = 100\left[\frac{10 - 0.7}{1mA} - 4.7k\right] = 460k$$

$$V_C = V_{CC} - I_C R_C = 10 - (1mA)\cdot(4.7k) = 5.3V$$

Collector Feedback Bias(contd.)

- The closest standard value to the 460k collector feedback bias resistor is 470k. Find the emitter current I_E with the 470 K resistor. Recalculate the emitter current for a transistor with β=100 and β=300.

$$\beta = 100 \qquad V_{CC} = 10V \qquad R_C = 4.7k \qquad R_B = 470k$$

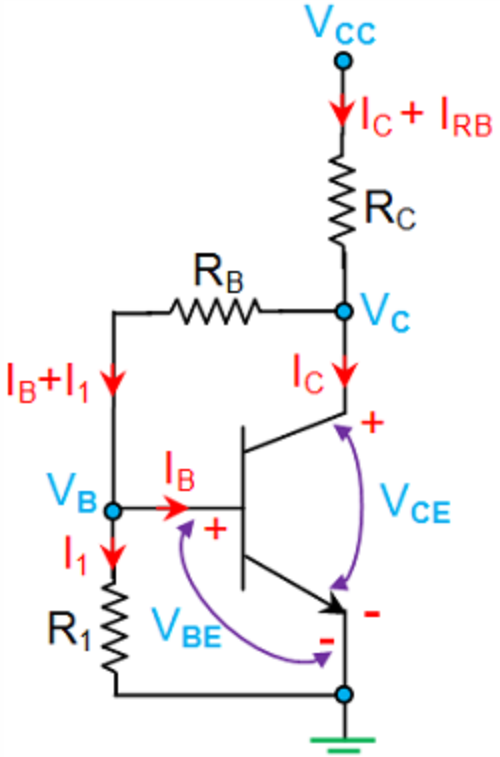
$$I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{10 - 0.7}{470k/100 + 4.7k} = 0.989mA$$

$$\beta = 300$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{10 - 0.7}{470k/300 + 4.7k} = 1.48mA$$

Dual Feedback Bias

- Figure shows a dual feedback bias network which is an improvisation over the collector feedback biasing circuit as it has an additional resistor R_1 which increases the stability of the circuit. This is because an increase in the current flow through the base resistors results in a network which is resistant to the variations in the values of β.



Dual Feedback Bias Circuit

Dual Feedback Bias

$$I_1 = 0.1 I_c$$

$$V_C = V_{cc} - (I_C + I_c R_B) R_C$$

$$V_B = V_{BE} = I_1 R_1 = V_C - (I_1 + I_B) R_B$$

$$I_C = \beta I_B$$

$$I_E \approx I_C$$

Collector-Emitter Feedback Bias

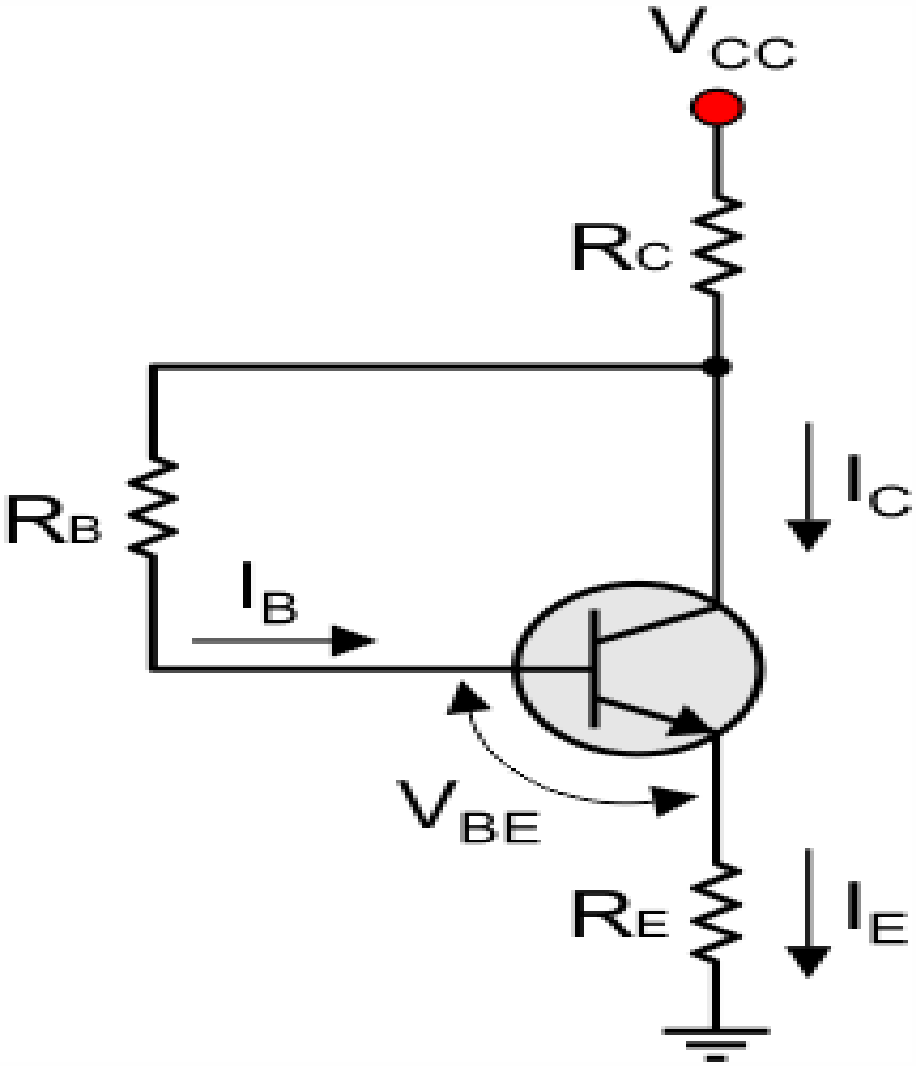
- The collector-emitter feedback bias circuit that can be obtained by applying both the collector-feedback and emitter-feedback.
- Here collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connection an emitter resistance from the emitter to ground.
- Both the feedbacks used to control the collector current Ic and base current IB in the opposite direction to increase the stability.

$$(I_B + I_C)R_E + V_{BE} + I_B R_B + (I_B + I_C)R_C - V_{CC} = 0$$

$$IB = \frac{V_{CC} - V_{BE}}{R_E + R_C + R_B} - \left(\frac{R_E + R_C}{R_E + R_C + R_B}\right) I_C$$

$$\frac{dI_B}{dI_C} = -\left(\frac{R_E + R_C}{R_E + R_C + RB}\right)$$

Collector-Emitter Feedback Bias

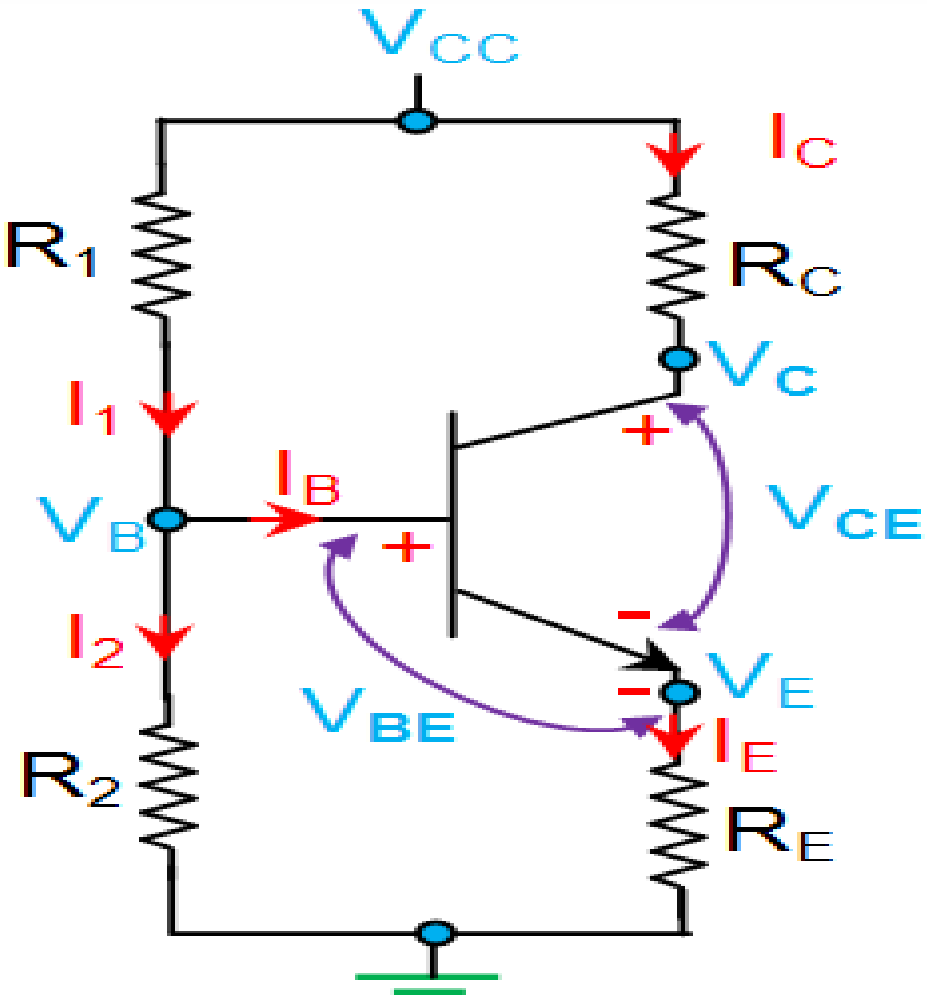


Voltage Divider Bias

- A simple circuit used to establish a stable operating point is the self-biasing configuration. The self bias, also called as emitter bias that can be used for low collector resistance.
- The current in the emitter resistor causes a voltage drop which is in the direction to reverse bias the emitter junction. For the transistor to remain in the active region, the base-emitter junction has to be forward biased.
- This type of biasing network employs a voltage divider formed by the resistors R_1 and R_2 to bias the transistor. This means that here the voltage developed across R_2 will be the base voltage of the transistor which forward biases its base-emitter junction.

- In general, the current through R_2 will be fixed to be 10 times required base current, I_B (i.e. $I_2 = 10I_B$). This is done to avoid its effect on the voltage divider current or on the changes in β.

Voltage Divider Bias(contd.)



Voltage Divider Bias Circuit

Voltage Divider Bias(contd.)

Stabilization Factors:

To determine stability factor, S Applying Thevenin's Theorem to the circuit

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \; and \; R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating this equation wrt Ic, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$

Voltage Divider Bias(contd.)

- In this kind of biasing, I_C is resistant to the changes in both β as well as V_{BE} which results in a stability factor of 1 (theoretically), the maximum possible thermal stability.

- This is because, as I_C increases due to a rise in temperature, IE also increases causing an increase in the emitter voltage V_E which in turn reduces the base-emitter voltage, V_{BE}.

- This results in the decrease of base current I_B which restores I_C to its original value. The higher stability offered by this biasing circuit makes it to be most widely used in spite of providing a decreased amplifier gain due to the presence of R_E

Voltage Divider Bias(contd.)

- Example: In a CE ge transistor amplifier circuit, the bias is provided by bias, i.e. emitter resistor and potential divider arrangement. The various parameters are Vcc=16V, Rc=3K,Re=2K,R1=56K,R2=20K and α=0.985. Determine (a) the coordinates of the operating point and (b) the stability factor S.

Solution: For a ge transistor Vbe=0.3v, as α=0.985

(a) To find coordinates of the operating point

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} = 66$$

$$R_B = \frac{R_2}{R_1 + R_2}.V_{cc} = \frac{20X10^3}{76X10^3}.16 = 4.21V$$

$$R_B = \frac{R_2}{R_1 + R_2} = \frac{20X10^3}{76X10^3} = 14.737K\Omega$$

Voltage Divider Bias(contd.)

- The loop equation around the base circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$3.91 = I_C [0.223 + 2.03].10^3$$

$$I_c = 1.73 mA$$

$$V_{CE} = V_{CC} - I_c R_c - I_E R_E = 7.35V$$

- (b) To find the stability factor S,

$$S = (1+\beta).\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}$$

$$S = (1+66).\frac{1+\frac{14.737}{2}}{1+66+\frac{14.737}{2}} = 7.536$$

Emitter-Feedback bias

- This biasing circuit is nothing but a fixed bias network with an additional emitter resistor, R_E. Here, if I_C rises due to an increase in temperature, then the I_E also increases which further increases the voltage drop across R_E. This results in the reduction of V_C, causing a decrease in I_B which in turn brings I_C back to its normal value.

- Thus this kind of biasing network is seen to offer better stability when compared to fixed base bias network.

- However the presence of R_E reduces the voltage gain of the amplifier as it results in unwanted AC feedback. In this circuit, the mathematical equations for different voltages and current are given as

Emitter-Feedback bias(contd.)

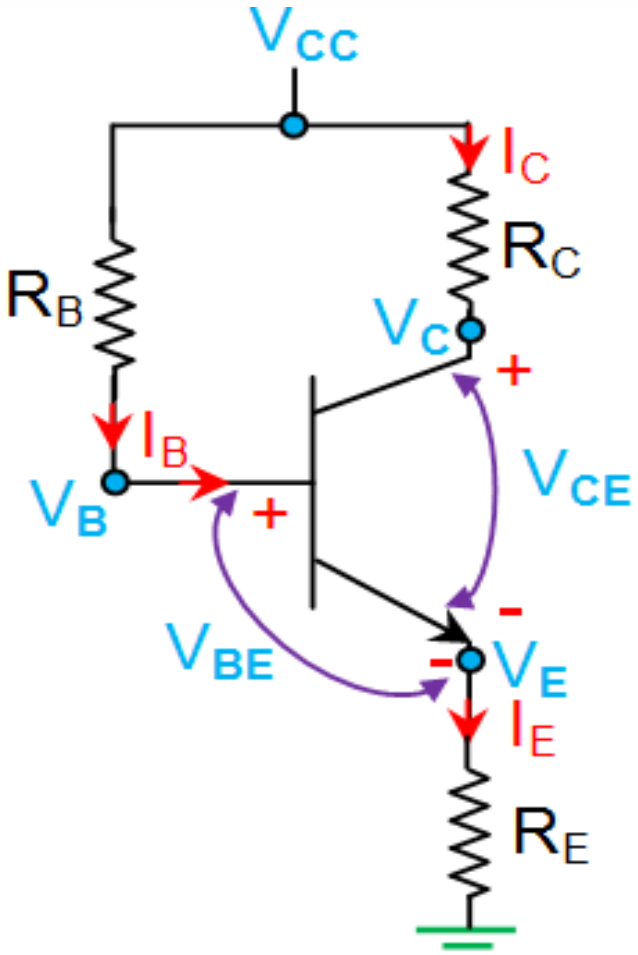
$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_E + R_B} - \left(\frac{R_E}{R_E + R_B} \right) I_C$$

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$



Fixed Bias with Emitter Resistor

Emitter-Feedback bias(contd.)

- Applying kirchoff's voltage law for the collector-emitter loop, we get

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E = I_C$$

- VE is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E$$

- The voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

- The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_E$$

$$V_B = V_{BE} + V_E$$

Emitter-Feedback bias(contd.)

Example:1

For the emitter feedback bias circuit, Vcc=+10v, Rc=1.5K, Rb=270K and Re=1K. Asuuming β=50, determine

a) stability factor

b) Ib and Ic

c) Vce

Sol:

a) The stability factor is

$$s = \frac{1 + \beta}{1 + \frac{\beta R_E}{(R_E + R_B)}}$$

$$s = \frac{1 + 50}{1 + \frac{50 \ X \ 1 X \ 10^{3}}{(1 X \ 10^{3} + 270 \ X \ 10^{3})}} = 43 .04$$

Emitter-Feedback bias(contd.)

b)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_B = \frac{10 - 0.7}{27\ X\ 10^{3} + (50 + 1)1\ X\ 10^{3}} = 28.97\ \mu A$$

c)

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_{CE} = 10 - 1.45\ X\ 10^{-3} (1.5\ X\ 10^{3} + 1\ X\ 10^{3}) = 6.38\ V$$

Stabilization against variations in V_{BE} and β

- Variation in the device parameters I_{CO}, V_{BE}&changes the value of the dc collector current I_C and thereby location of the Q-point is changed. This change of location of Q-point is called Q-point instability or biasinstability.

- This bias instability is reduced considerably in a self-bias C.E amplifier. The situation under which greater bias stability in a self bias C_E amplifier is as discussed below.

- $I_C = f(I_{CO}, V_{BE}, \beta)$ --------(1)

$$\Delta I_C = \frac{\partial I_C}{\partial I_{Co}}\Bigg|_{\beta,\ V_{BE}} \Delta I_{Co} + \frac{\partial I_C}{\partial V_{BE}}\Bigg|_{I_{Co},\ \beta} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta}\Bigg|_{I_{CO},\ V_{BE}} \Delta\beta \qquad \text{----------(2)}$$

Stabilization against variations in V_{BE} and β

- $\Delta I_C = S\Delta I_{CO} + S'\Delta V_{BE} + S''\Delta\beta$ ----------(3)

  S --> S_I

  S' --> S_V

  S'' --> S_β

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \quad \text{when } V_{BE} \& \ \beta \text{ is assumed to be constant}$$

V_{BE}, β

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big|_{I_{CO}, V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S'' = \frac{\partial I_C}{\partial \beta} \Big|_{I_{CO}, V_{BE}} \approx \frac{\Delta I_C}{\Delta \beta}$$

Stabilization against variations in V_{BE} and β

- Stability factor S or S_I

$$S \equiv \frac{\partial I_C}{\partial I_{Co}} \Bigg|_{V_{BE},\ \beta}$$

$$I_C = \frac{\beta(V_B - V_{BE})}{R_B + (1+\beta)R_E} + \frac{(R_B + R_E)(1+\beta)I_{Co}}{R_B + (1+\beta)R_E}$$

$$S = \frac{\partial I_C}{\partial I_{Co}} = 0 + \frac{(R_B + R_E)(1+\beta)}{R_B + (1+\beta)R_E} \text{-----(1)}$$

V_{BE}, β

- $R_B << (1 + \beta) R_E, \quad \beta >> 1$
  Under this condition

$$S = \frac{(1+\beta)(R_B + R_E)}{(1+\beta) R_E} = \frac{1 + R_B}{R_E} \text{ - - - - - - -(2)}$$

$$\therefore \quad S = 1 + \frac{R_B}{R_E}$$

To keep S minimum, $\frac{R_B}{R_E}$ is kept as small as possible. The value of S lies between 3 to 15.

Bias Compensation techniques

Diode Compensation for Instability:

- These are the circuits, as the gain of the amplifier is a very important consideration, some compensation techniques are used to maintain excellent bias and thermal stabilization.

- These are the circuits that implement compensation techniques using diodes to deal with biasing instability. The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant.

There are two types of diode compensation methods. They are −

- Diode compensation for instability due to V_{BE} variation

- Diode compensation for instability due to I_{CO} variation

Bias Compensation techniques(contd.)

Diode Compensation for Instability due to V_{BE} Variation:

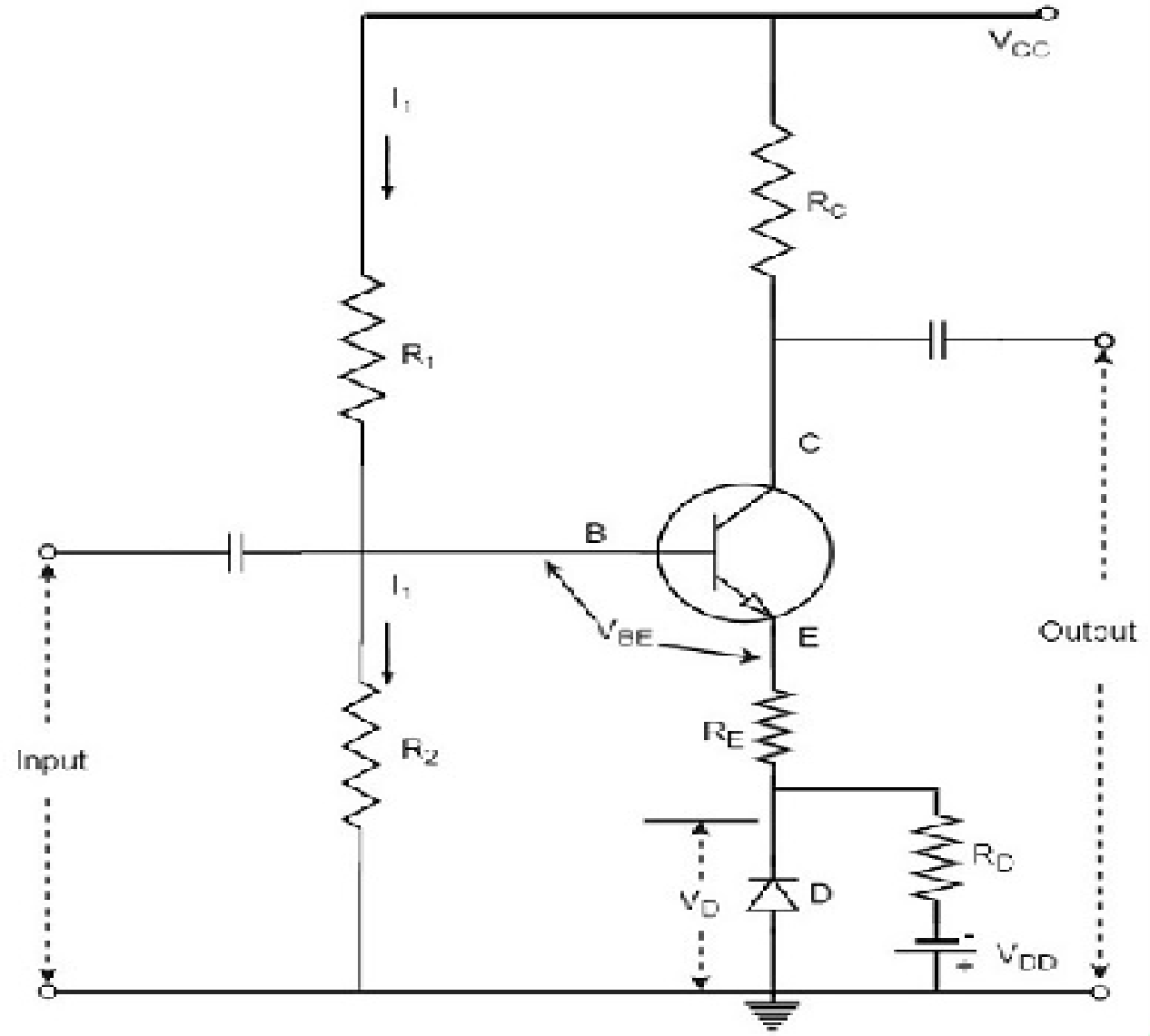
- In a Silicon transistor, the changes in the value of V_{BE} results in the changes in I_C. A diode can be employed in the emitter circuit in order to compensate the variations in V_{BE} or I_{CO}.

- As the diode and transistor used are of same material, the voltage V_D across the diode has same temperature coefficient as V_{BE} of the transistor.

- The diode D is forward biased by the source VDD and the resistor RD. The variation in VBE with temperature is same as the variation in VD with temperature, hence the quantity (VBE – VD) remains constant.

- So the current IC remains constant in spite of the variation in VBE.

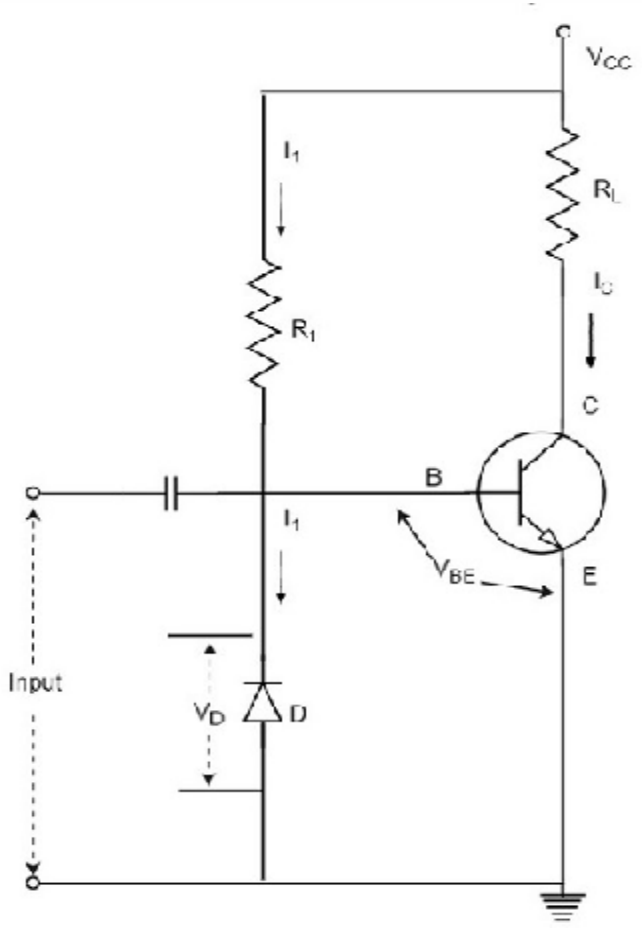
Bias Compensation techniques(contd.)



Bias Compensation techniques(contd.)

Diode Compensation for Instability due to I_{CO} Variation

- The following figure shows the circuit diagram of a transistor amplifier with diode D used for compensation of variation in I_{CO}.



Bias Compensation techniques(contd.)

- So, the reverse saturation current I_O of the diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO}.

$$I = \frac{V_{CC} - V_{BE}}{R} \cong \frac{V_{CC}}{R} = cons\ \tan\ t$$

- The diode D is reverse biased by V_{BE} and the current through it is the reverse saturation current I_O.
- Now the base current is, $I_B = I - I_O$
- Substituting the above value in the expression for collector current.

$$I_C = ß(I - I_O) + (1 + ß)I_{CO}$$

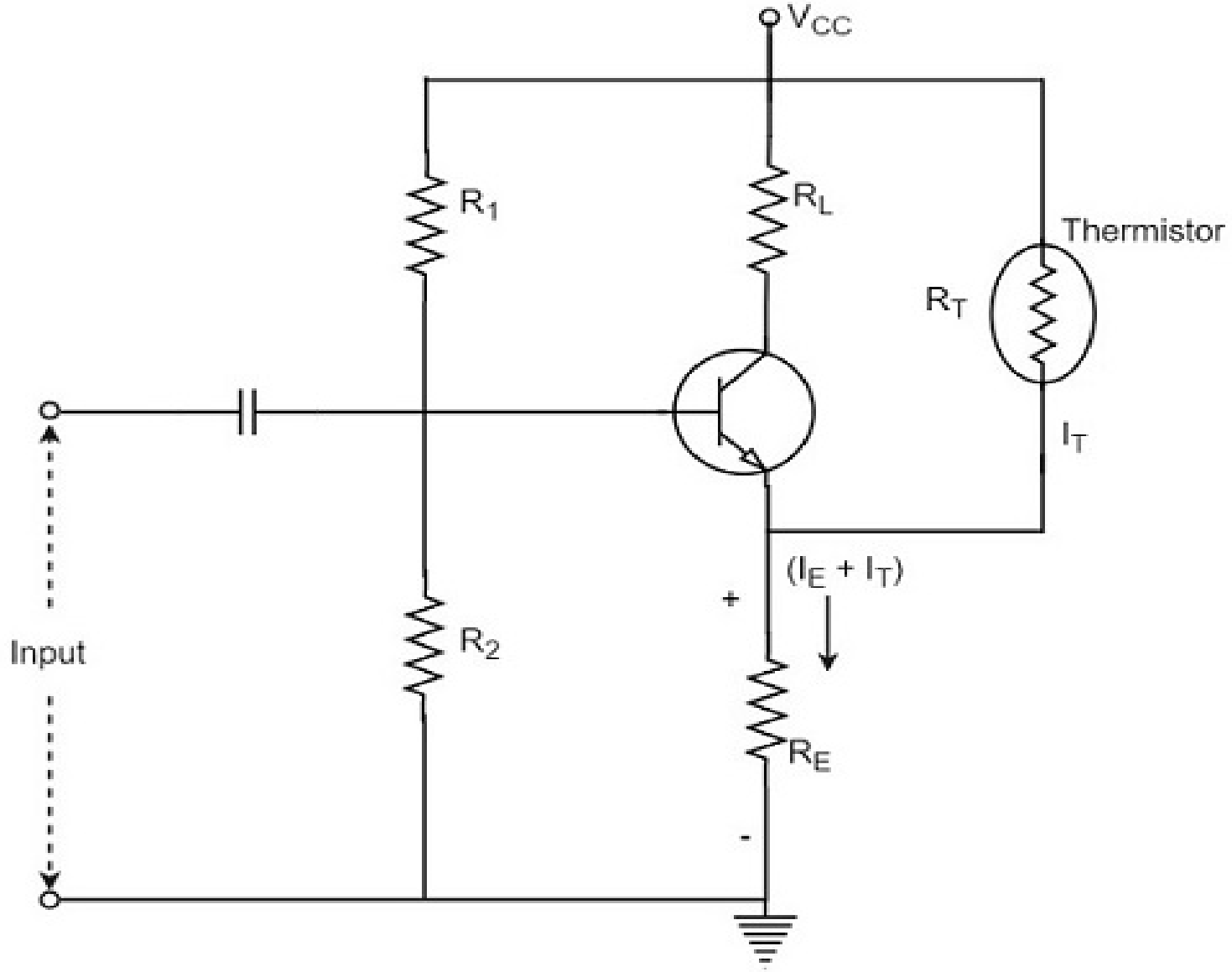
- If $\beta \gg 1$, $I_C = ßI - ßI_O + ßI_{CO}$
- **I** is almost constant and if I_O of diode and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

Bias Compensation techniques(contd.)

Thermistor Compensation

- Thermistor is a temperature sensitive device. It has negative temperature coefficient. The resistance of a thermistor increases when the temperature decreases and it decreases when the temperature increases. The below figure shows a self-bias amplifier with thermistor compensation.
- In an amplifier circuit, the changes that occur in ICO, VBE and β with temperature, increases the collector current. Thermistor is employed to minimize the increase in collector current. As the temperature increases, the resistance RT of thermistor decreases, which increases the current through it and the resistor RE. Now, the voltage developed across RE increases, which reverse biases the emitter junction. This reverse bias is so high that the effect of resistors R1 and R2 providing forward bias also gets reduced. This action reduces the rise in collector current

Bias Compensation techniques(contd.)



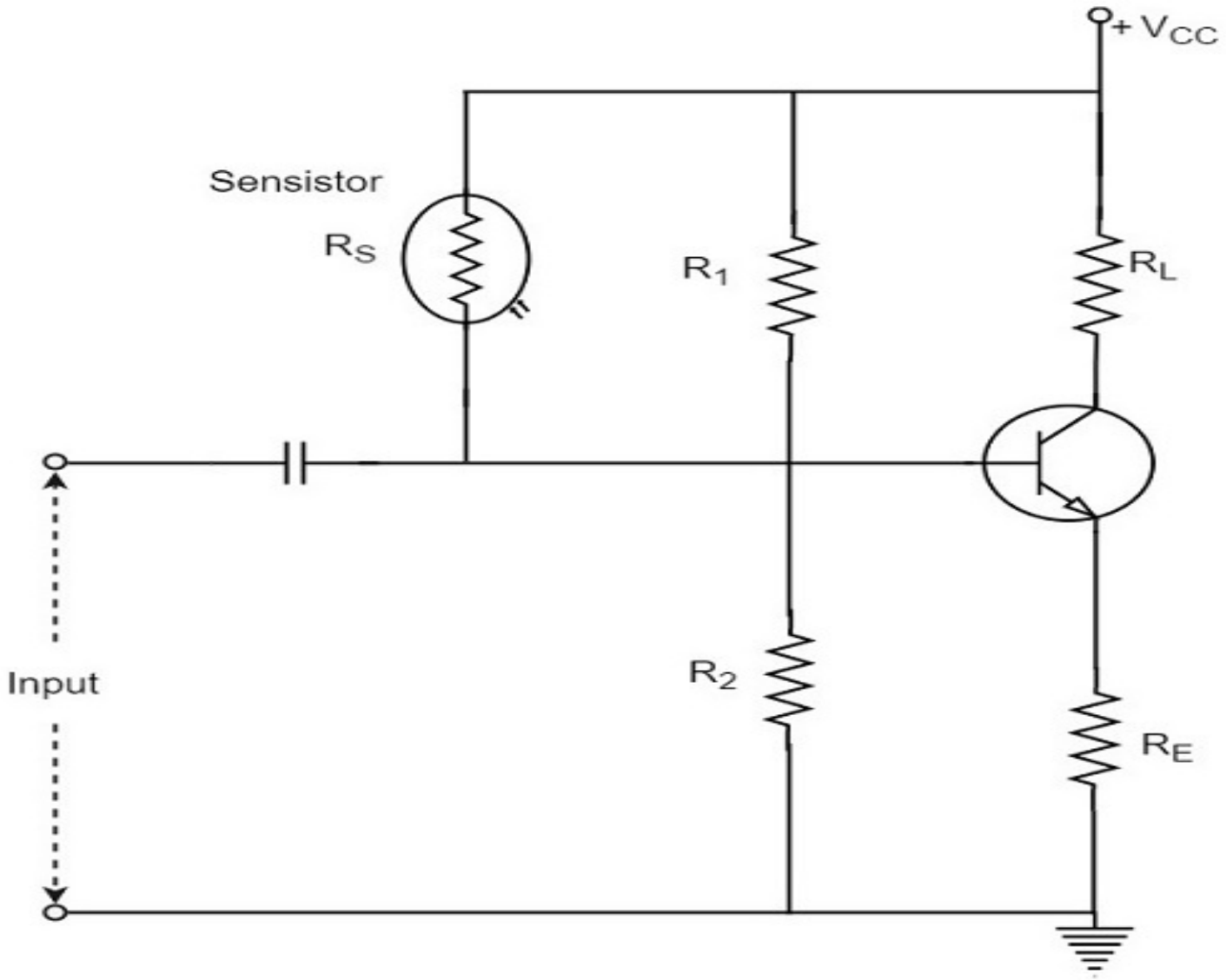
Sensistor Compensation

- A Sensistor is a heavily doped semiconductor that has positive temperature coefficient. The resistance of a Sensistor increases with the increase in temperature and decreases with the decrease in temperature. The figure below shows a self-bias amplifier with Sensistor compensation.

- In the below figure, the Sensistor may be placed in parallel with R1 or in parallel with RE. As the temperature increases, the resistance of the parallel combination, thermistor and R1 increases and their voltage drop also increases. This decreases the voltage drop across R2. Due to the decrease of this voltage, the net forward emitter bias decreases. As a result of this, IC decreases.

- Hence by employing the Sensistor, the rise in the collector current which is caused by the increase of ICO, VBE and β due to temperature, gets controlled.

Sensistor Compensation



Thermal Resistance

- The transistor is a temperature dependent device. When the transistor is operated, the collector junction gets heavy flow of electrons and hence has much heat generated. This heat if increased further beyond the permissible limit, damages the junction and thus the transistor.
- In order to protect itself from damage, the transistor dissipates heat from the junction to the transistor case and from there to the open air surrounding it.
- Let, the ambient temperature or the temperature of surrounding air = $T_A{}^oC$
- And, the temperature of collector-base junction of the transistor = $T_J{}^oC$
- As $T_J > T_A$, the difference $T_J - T_A$ is greater than the power dissipated in the transistor P_D will be greater. Thus,

$$H = \frac{T_J - T_A}{P_D}$$

$$T_J - T_A \propto P_D$$

$$T_J - T_A = HP_D$$

Thermal Resistance

- Where H is the constant of proportionality, and is called as **Thermal resistance**.
- Thermal resistance is the resistance to heat flow from junction to surrounding air. It is denoted by H.

$$H = \frac{T_J - T_A}{P_D}$$

- The unit of H is oC/watt.
- If the thermal resistance is low, the transfer of heat from the transistor into the air, will be easy. If the transistor case is larger, the heat dissipation will be better. This is achieved by the use of Heat sink.

Thermal Runaway

- The collector current for the CE circuit is given by

$$I_c = \beta I_B + (1 + \beta) I_{c0}$$

- The three variables in the equation, β ,IB and IC0 increase with rise in temperature.
- In particular, the reverse saturation current changes greatly with temperature.

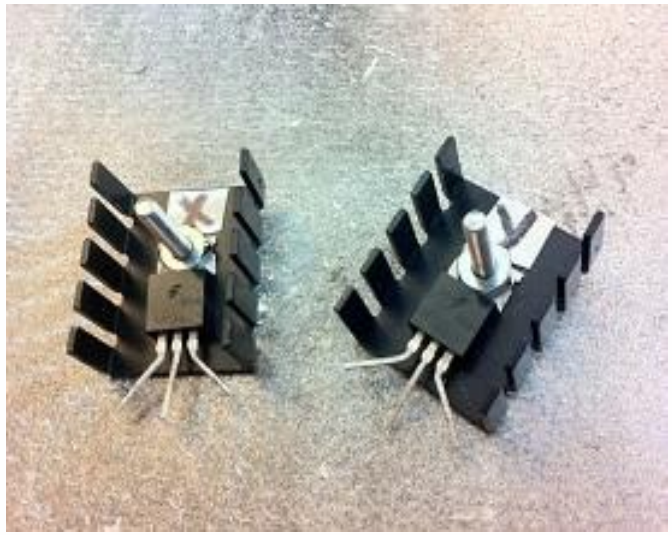
- The collector current causes the collector base junction temperature to rise which, in turn, increase leakage current, as result Ic will increase still further, which will further rise the temperature at the collector base junction.

- This process will become cumulative leading to "**thermal runaway**".

Thermal Runaway

- The use of heat sink avoids the problem of **Thermal Runaway**. It is a situation where an increase in temperature leads to the condition that further increase in temperature, leads to the destruction of the device itself. This is a kind of uncontrollable positive feedback.

- **Heat sink** is not the only consideration; other factors such as operating point, ambient temperature, and the type of transistor used can also cause thermal runaway.



Thermal Stability

- For preventing thermal runaway, the required condition is that the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition.
- Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_c}{\partial T_J} < \frac{1}{\Theta}$$

- In the self bias circuit, the transistor is biased in the active region. The power generated at the collector junction without any signal is

$$P_c = I_c V_{CB} \approx I_c V_{CE}$$

- The condition o prevent thermal runaway can be rewritten as

$$\frac{\partial P_c}{\partial I_c} \frac{\partial I_c}{\partial T_c} < \frac{1}{\Theta}$$

Thermal Stability(contd.)

- Differentiating above equation with respect to Ic, we get

$$\frac{\partial P_c}{\partial T_J} = V_{CC} - 2I_C(R_E - R_C)$$

- Hence to avoid thermal runaway, it is necessary that

$$I_C \lhd \frac{V_{CC}}{2(R_E + R_C)}$$

- Since VCE=Vcc - Ic(Re+Rc).
- When the effect of Ico dominates $\Delta I_C = S\Delta I_{C0}$ There fore eq becomes

$$\frac{\partial P_c}{\partial I_C}\left(S\,\frac{\partial I_{C0}}{\partial T_J}\right) \lhd \frac{1}{\Theta}$$

- Since the reverse saturation current for either silicon or ge increases about 7 percent/0C

$$\frac{\partial I_{C0}}{\partial T_J}) = 0.07\ I_{C0}$$

Thermal Stability(contd.)

The thermal stability of a transistor is closely related to its thermal resistance.

- Thermal resistance can be defined as the resistance to the flow of heat which is trying to flow from the collector area to the atmosphere.
- In a particular transistor, there is a lot of current flowing through the collector region. Due to this, there will be a large amount of heat produced in that region.
- Now, if this heat is not released in the atmosphere then the transistor may become over heated and even burn due to excess temperature than the collector region can handle.
- Here thermal resistance comes into picture.
- Lower the thermal resistance, and more heat is allowed to flow into the atmosphere.
- Thus power transistors have less thermal resistance than ordinary transistors as they generate more heat energy.

Biasing the FET and MOSFET

- Biasing an FET amplifier circuit is similar to BJT amplifiers. We will use components external to the transistor and dc sources to define a predictable and stable operating point (our old friend, the Qpoint), about which the circuit may provide linear amplification. Bias stability in FET amplifiers means that the dc drain current (ID) stays as constant as possible with variations in operating conditions and device parameters. As a rule of thumb:

- For the FET to operate as a linear amplifier, the Q-point should be in the middle of the saturation region, the instantaneous operating point must at all times be confined to the saturation region, and the input signal must be kept sufficiently small.

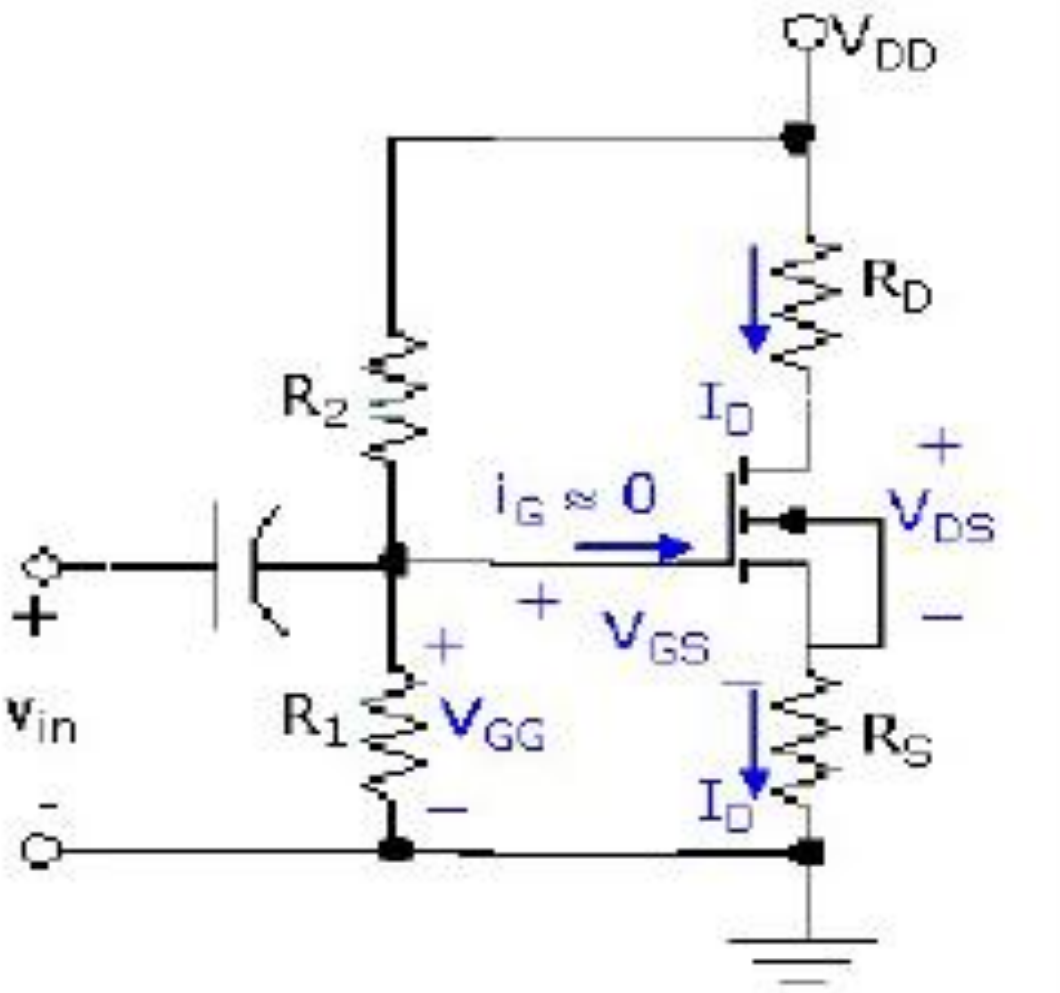
Biasing the FET and MOSFET(contd.)

- Discrete-component biasing using source-resistance feedback is illustrated in the figure. Although the circuit is shown with an enhancement MOSFET, this biasing arrangement works for depletion MOSFETs and JFETs (and should look familiar as a biasing circuit for BJTs).

- Note that if two supplies (VDD and –VSS) are used instead of the single-supply illustrated, all derived expressions will use VDD-VSS, rather than VDD.

- Also, for depletion mode MOSFETs or JFET devices, R2 can be either finite or infinite (open). To start with, we are also going to use the assumption that capacitors used in the circuit are large enough to provide dc isolation and act as shorts under ac conditions (the old “infinite and ideal” ploy).

Biasing the FET and MOSFET(contd.)



Biasing the FET and MOSFET(contd.)

$$R_G = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{GG} = \frac{V_{DD} R_1}{R_1 + R_2}$$

- Looking at the figure above, we have three unknown variables to define for biasing (IDQ, VGSQ and VDSQ), so we need three dc equations. The first is found from the definition of the drain current in the saturation region, while the other two are the KVL equations obtained from the Thevenin equivalent circuit.

$$I_{DQ} = K(V_{GSQ} - V_T)^2(1 + \lambda V_{DSQ}) \cong K(V_{GSQ} - V_T)^2 = KV_T^2\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_T}\right)^2 \quad (MOSFET)$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2(1 + \lambda V_{DSQ}) \cong I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \quad (JFET)$$

UNIT 5

BJT AND FET AMPLIFIERS

BJT small signal analysis

What is a Small Signal Model?

- A small signal model is a linear model which is independent of amplitude. It may or may not have time dependence (i.e. capacitors).
- The small signal model for a nonlinear component such as a BJT is a linear model about some nominal operating point. The deviations from the operating point are small enough that it approximates the nonlinear component over a limited range of amplitudes. Illustration of the pn diode.
- The hybrid model has four h-parameters. The "h" stands for hybrid because the parameters are a mix of impedance, admittance and dimensionless units. In common emitter the parameters are:
- **Hie input impedance (Ω)**
- **hre reverse voltage ratio (dimensionless)**
- **hfe forward current transfer ratio (dimensionless)**
- **hoe output admittance (Siemen)**

BJT small signal analysis(contd..)

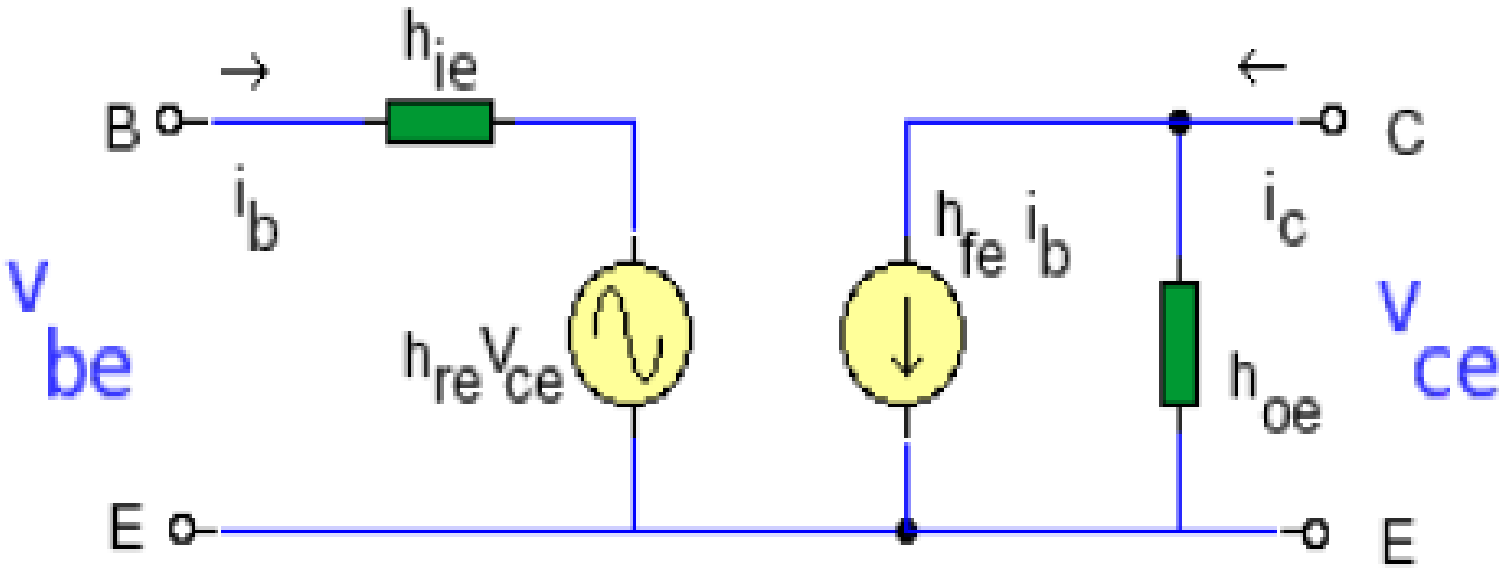
- The hybrid model is suitable for small signals at mid band and describes the action of the transistor. Two equations can be derived from the diagram, one for input voltage vbe and one for the output ic:
- vbe = hie ib + hre vce
- ic = hfe ib + hoe vce

- If ib is held constant (ib=0) then hre and hoe can be solved:
- hre = vbe / vce | ib = 0
- hoe = ic / vce | ib = 0

- Also if vce is held constant (vce=0) then hie and hfe can be solved:
- hie = vbe / ib | vce = 0
- hfe = ic / ib | vce = 0

BJT small signal analysis(contd..)

- These are the four basic parameters for a BJT in common emitter. Typical values are hre = 1 x10-4, hoe typical value 20uS, hie typically 1k to 20k and hfe can be 50 - 750. The Hparameters can often be found on the transistor datasheets. The table below lists the four h-parameters for the BJT in common base and common collector (emitter follower)



BJT small signal analysis(contd..)

Common Base	Common Emitter	Common Collector	Definitions
$h_{ib} = \frac{v_{eb}}{i_e}$	$h_{ie} = \frac{v_{be}}{i_b}$	$h_{ic} = \frac{v_{bc}}{i_b}$	Input Impedance with Output Short Circuit
$h_{rb} = \frac{v_{eb}}{v_{cb}}$	$h_{re} = \frac{v_{be}}{v_{ce}}$	$h_{rc} = \frac{v_{bc}}{v_{ec}}$	Reverse Voltage Ratio Input Open Circuit
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$	Forward Current Gain Output Short Circuit
$h_{ob} = \frac{i_c}{v_{cb}}$	$h_{oe} = \frac{i_c}{v_{ce}}$	$h_{oc} = \frac{i_e}{v_{ec}}$	Output Admittance Input Open Circuit

BJT small signal analysis(contd..)

Typical h-parameter Values

h-parameters are not constant and vary with both temperature and collector current. Typical values for 1mA collector currents are:

$h_{ie} = 1000\ \Omega \quad h_{re} = 3 \times 10^{-4} \quad h_{oe} = 3 \times 10^{-6} S \quad h_{fe} = 250$

BJT hybrid model

- The circuit of the basic two port network is shown on the right. Depending on the application, it may be used in a number of different ways to develop different models. We will use it to develop the h-parameter model. Other models may be covered in EE III. The h-parameter model is typically suited to transistor circuit modeling. It is important because:
- 1. its values are used on specification sheets
- 2. it is one model that may be used to analyze circuit behavior
- 3. it may be used to form the basis of a more accurate transistor model
- The h parameter model has values that are complex numbers that vary as a function of:
- 1. Frequency
- 2. Ambient temperature
- 3. Q-Point

BJT hybrid model

The h-parameter model is defined by:

$$\begin{vmatrix} V_1 \\ I_2 \end{vmatrix} = \begin{vmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{vmatrix} \begin{vmatrix} I_1 \\ V_2 \end{vmatrix}$$

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2$$

The h-parameter model for the common emitter circuit is on the right. On spec sheet:

$h_{11} = h_{ix}$

$h_{12} = h_{rx}$

$h_{21} = h_{fx}$

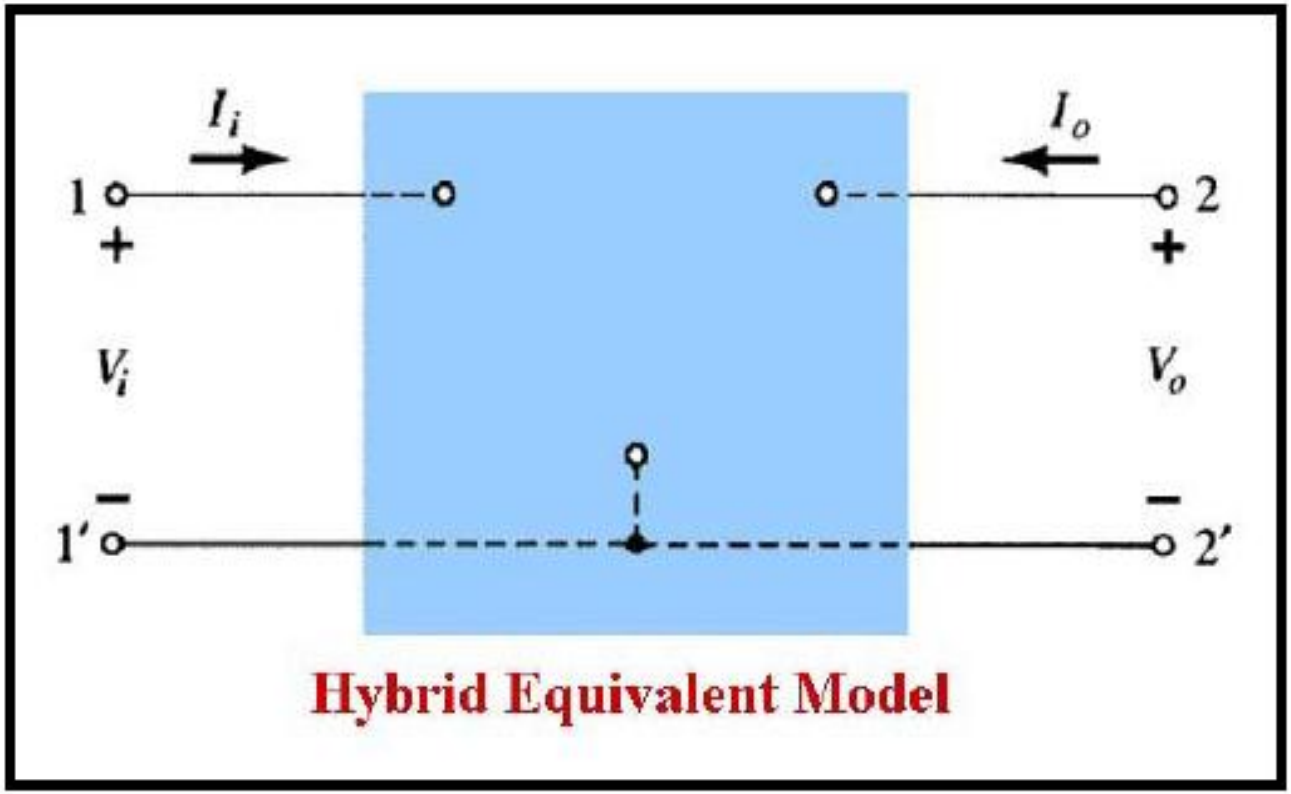
$h_{22} = h_{ox}$

h_{rx} and h_{fx} are dimensionless ratios

h_{ix} is an impedance <Ω>

h_{ox} is an admittance <S>

BJT hybrid model



Hybrid Equivalent Model

Hybrid parameters

- **Hybrid parameters** are also referred as **h parameters**. These are referred as hybrid because, here Z parameters, Y parameters, voltage ratio, current ratio, all are used to represent the relation between voltage and current in a two port network. The relations of voltages and current in **hybrid parameters** are represented as,

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

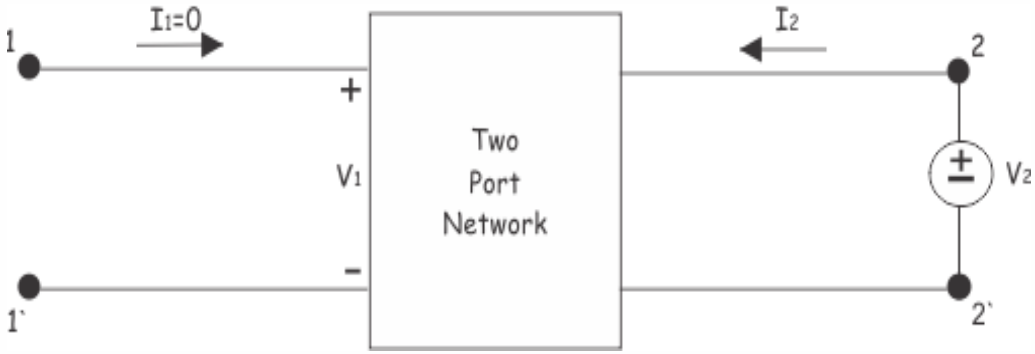
$$g_{11} = \left.\frac{I_1}{V_1}\right|_{I_2 = 0} = \textit{open circuit input admittance}$$

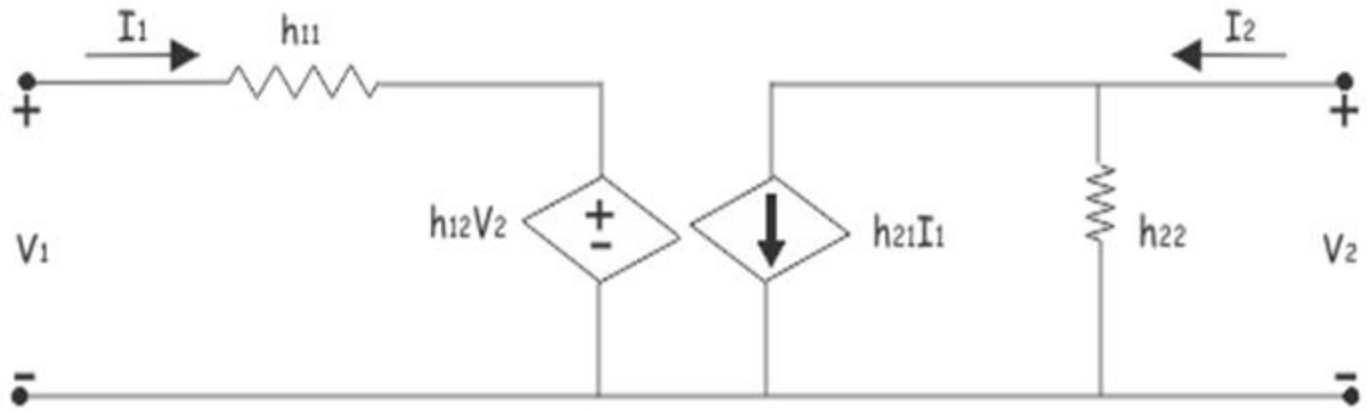
$$g_{12} = \left.\frac{I_1}{I_2}\right|_{V_1 = 0} = \textit{short circuit reverse current gain}$$

$$g_{21} = \left.\frac{V_2}{V_1}\right|_{I_2 = 0} = \textit{open circuit voltage gain}$$

$$g_{22} = \left.\frac{V_2}{I_2}\right|_{V_1 = 0} = \textit{short circuit output impedance}$$

General Model





h-Parameter model

General Model

Current gain:

$$A_i = \frac{I_L}{I_1}$$

$$I_2 = h_f I_1 + h_o V_2$$

$$V_2 = -I_2 R_L$$

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$I_2 + h_o (I_2 R_L) = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$$

General Model(contd.)

Current gain(Ais):

$$A_{is} = \frac{-I_2}{I_s} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_s} = A_i \cdot \frac{I_1}{I_s}$$

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$V_1 = \frac{Z_i}{R_s + Z_i} V_s$$

$$A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

Input Resistance(Zi):

$$Z_i = \frac{V_1}{I_1}$$

$$V_1 = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$V_2 = A_i I_1 R_L$$

$$Z_i = h_i + h_r A_i R_L$$

General Model(contd.)

Voltage Gain(Av):

$$A_v = \frac{V_2}{V_1}$$

$$A_v = \frac{A_i I_1 R_L}{Z_i}$$

Voltage Gain(Avs):

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} = \frac{V_1}{V_s}$$

$$A_p = \frac{p_2}{P_1} = A_i^2 \frac{R_L}{Z_i}$$

$$A_{vs} = A_v . \frac{V_1}{V_s}$$

$$V_1 = \frac{Z_i}{R_s + Z_i} V_s$$

$$A_{vs} = \frac{A_i R_L}{R_s + R_i}$$

General Model(contd.)

Output Resistance:

$$Y_o = \frac{I_2}{V_2}$$

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$Y_0 = h_f . \frac{-h_r}{R_s + h_i} + h_o$$

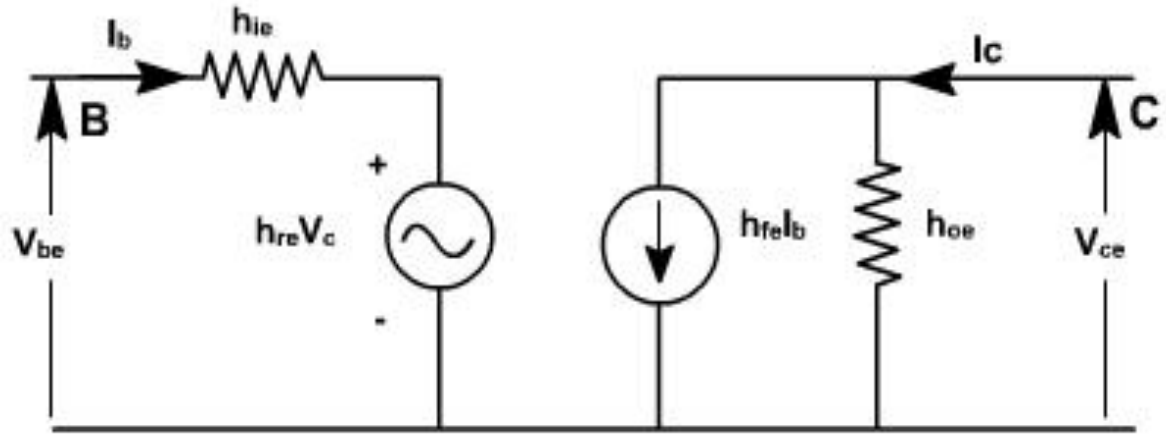
Power gain(Ap):

$$A_p = \frac{p_2}{P_1} = A_v A_i$$

$$A_p = \frac{p_2}{P_1} = A_i^2 \frac{R_L}{Z_i}$$

Common Emitter Exact Analysis

H-parameter model:



Current gain: $$\frac{I_2}{I_1} = \frac{-h_{fe}}{1 + h_{oe} R_L}$$

Input Resistance: $$Z_i = h_{ie} + h_{re} A_i R_L$$

Voltage Gain: $$A_v = \frac{A_i I_1 R_L}{Z_i}$$

Output Resistance: $$Y_0 = h_{fe} \cdot \frac{-h_{re}}{R_s + h_{ie}} + h_{oe}$$

Example

$R_s = 1K$, $R_1 = 50\ K$, $R_2 = 2\,K$, $R_L = 2\,K$, $Rc = 2\,Kh_{fe} = 50$, $h_{ie} = 1.1K$,

$h_{oe} = 25\,uA\ /V$ & $h_{re} = 2.5\,X\,10^{-4}$

$$A_i = -h_{fe}$$

$$A_i = -50$$

$$R_i = 1.1K$$

$$R_i = 1.1K$$

$$A_v = -45\ .45$$

$$A_v = -45\ .45$$

Example(Contd.)

Output Resistance:

$$R_0 = \frac{1}{Y_0} = \infty$$

$$A_{is} = -15.9$$

$$R_0' = 1k$$

Overall Voltage Gain:

$$Avs = \frac{V_o}{V_s} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_s}$$

$$Avs = \frac{A_v . R_i'}{R_i' + R_s}$$

$$Avs = -18.71$$

Overall Current Gain:

$$A_{is} = \frac{I_L}{I_s} = \frac{I_L}{I_c} \frac{I_c}{I_b} \frac{I_b}{I_s}$$

$$A_{is} = -15.9$$

CB Approximate Analysis

Current gain:

$$A_i = \frac{I_0}{I_e} = \frac{-I_c}{I_e} = \frac{-h_{fe} I_b}{-(1+h_{fe}) I_b}$$

$$A_i = \frac{h_{fe}}{(1+h_{fe})}$$

Input Resistance:

$$R_i = \frac{V_e}{I_e} = \frac{-hieI_b}{-(1+h_{fe}) I_b}$$

$$R_i = \frac{V_e}{I_e} = \frac{hie}{(1+h_{fe})}$$

Voltage Gain:

$$A_v = \frac{V_0}{V_e} = \frac{I_0 R_L}{I_e R_i} = \frac{A_i R_L}{R_i}$$

$$A_v = \frac{h_{fe} R_L}{h_{ie}}$$

CB Approximate Analysis(contd.)

Output Resistance:

$$R_0 = \frac{V_0}{I_c} | V_s = 0$$

$$R_0' = R_0 // R_L = R_L$$

Example:

A common Base Amplifier having following Values.

$R_s = 600\ \Omega, R_c = 5.6K, R_E = 5.6K, R_L = 39\ K, h_{ie} = 1k, h_{fe} = 85, h_{oe} = 2uA/V.$

Find Ai, Ri, Av, R0.

Current gain:

$$A_i = \frac{h_{fe}}{(1 + h_{fe})}$$

$$A_i = 0.98$$

Example

Input Resistance:

$$R_i = \frac{V_e}{I_e} = 11.6\,\Omega$$

$$R_i = \frac{V_e}{I_e} = 11.6\,\Omega$$

Voltage Gain:

$$A_v = \frac{h_{fe} R_L}{h_{ie}}$$

$$A_v = 416.23$$

Output Resistance:

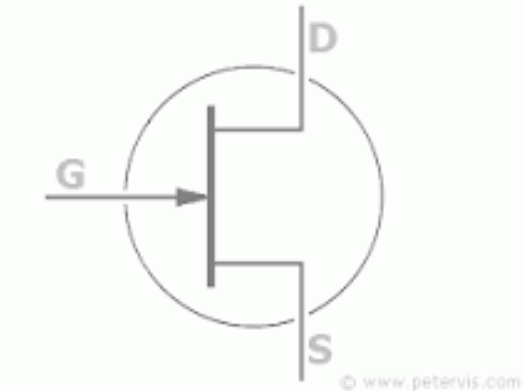
$$R_0' = R_0 // R_L = 4.89\ K$$

$$R_0' = R_0 // R_L = 4.89\ K$$

FET small signal model

FET:

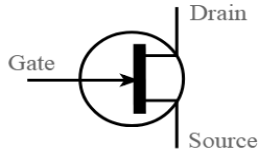
- The **field-effect transistor** (**FET**) is a transistor that uses an electric field to control the electrical behavior of the device. FETs are also known as **unipolar transistors** since they involve single-carrier-type operation. Many different implementations of field effect transistors exist. Field effect transistors generally display very high input impedance at low frequencies. The conductivity between the drain and source terminals is controlled by an electric field in the device, which is generated by the voltage difference between the body and the gate of the device.



FET small signal model

- **n-channel:**
- In an n-channel "depletion-mode" device, a negative gate-to-source voltage causes a depletion region to expand in width and encroach on the channel from the sides, narrowing the channel. If the active region expands to completely close the channel, the resistance of the channel from source to drain becomes large, and the FET is effectively turned off like a switch (see right figure, when there is very small current).

- This is called "pinch-off", and the voltage at which it occurs is called the "pinch-off voltage". Conversely, a positive gate-to-source voltage increases the channel size and allows electrons to flow easily (see right figure, when there is a conduction channel and current is large)

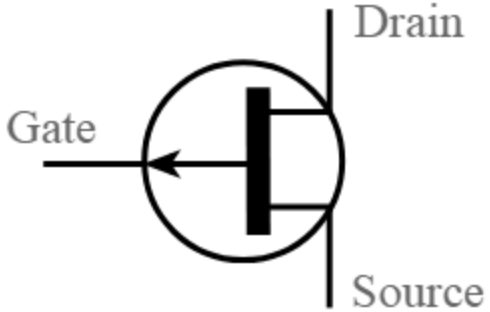


N-Channel

FET small signal model

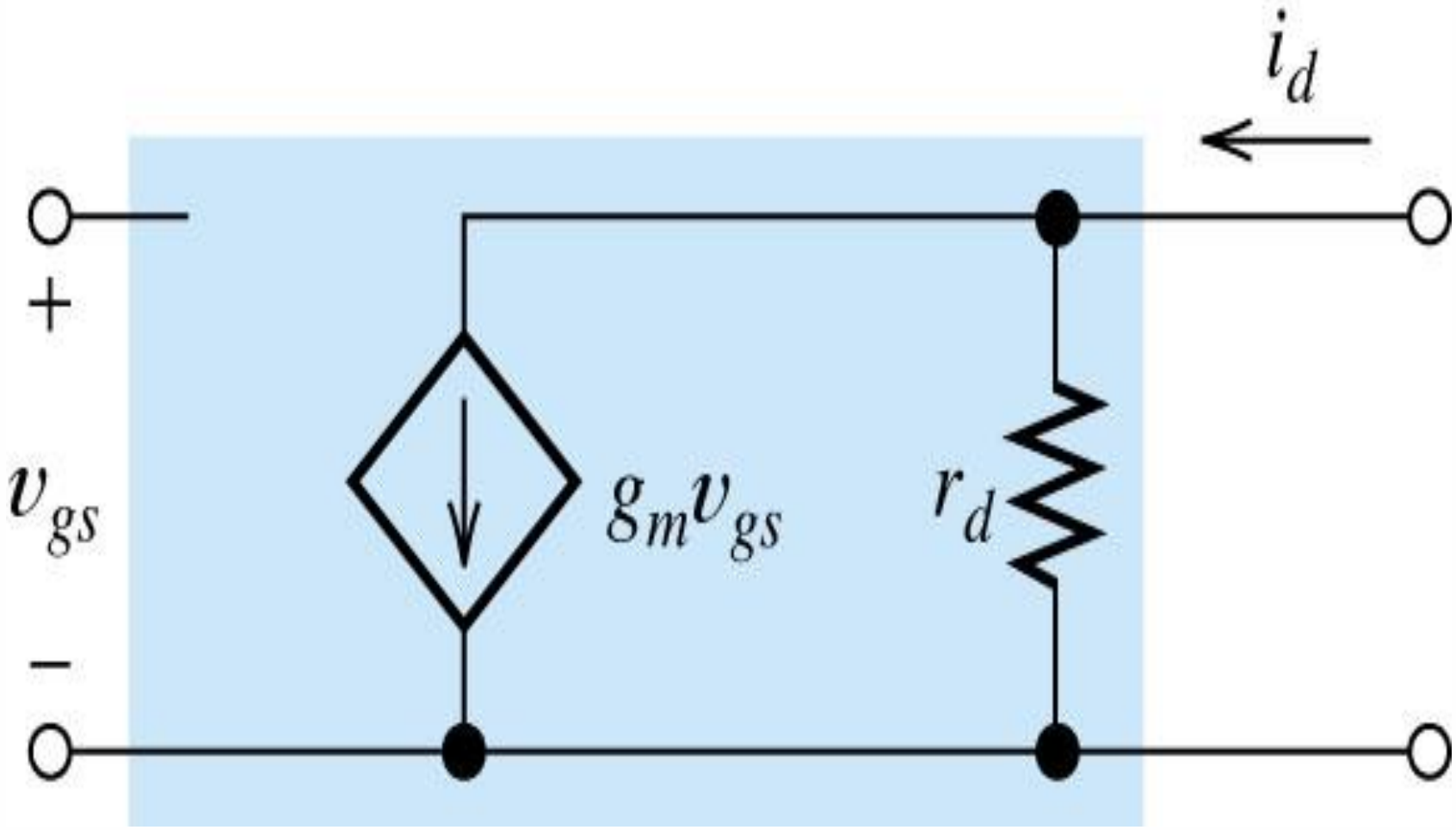
- **p-channel:**

  In a p-channel "depletion-mode" device, a positive voltage from gate to body widens the depletion layer by forcing electrons to the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, positively charged acceptor ions. Conversely, in a p-channel "enhancement-mode" device, a conductive region does not exist and negative voltage must be used to generate a conduction channel.



P-Channel

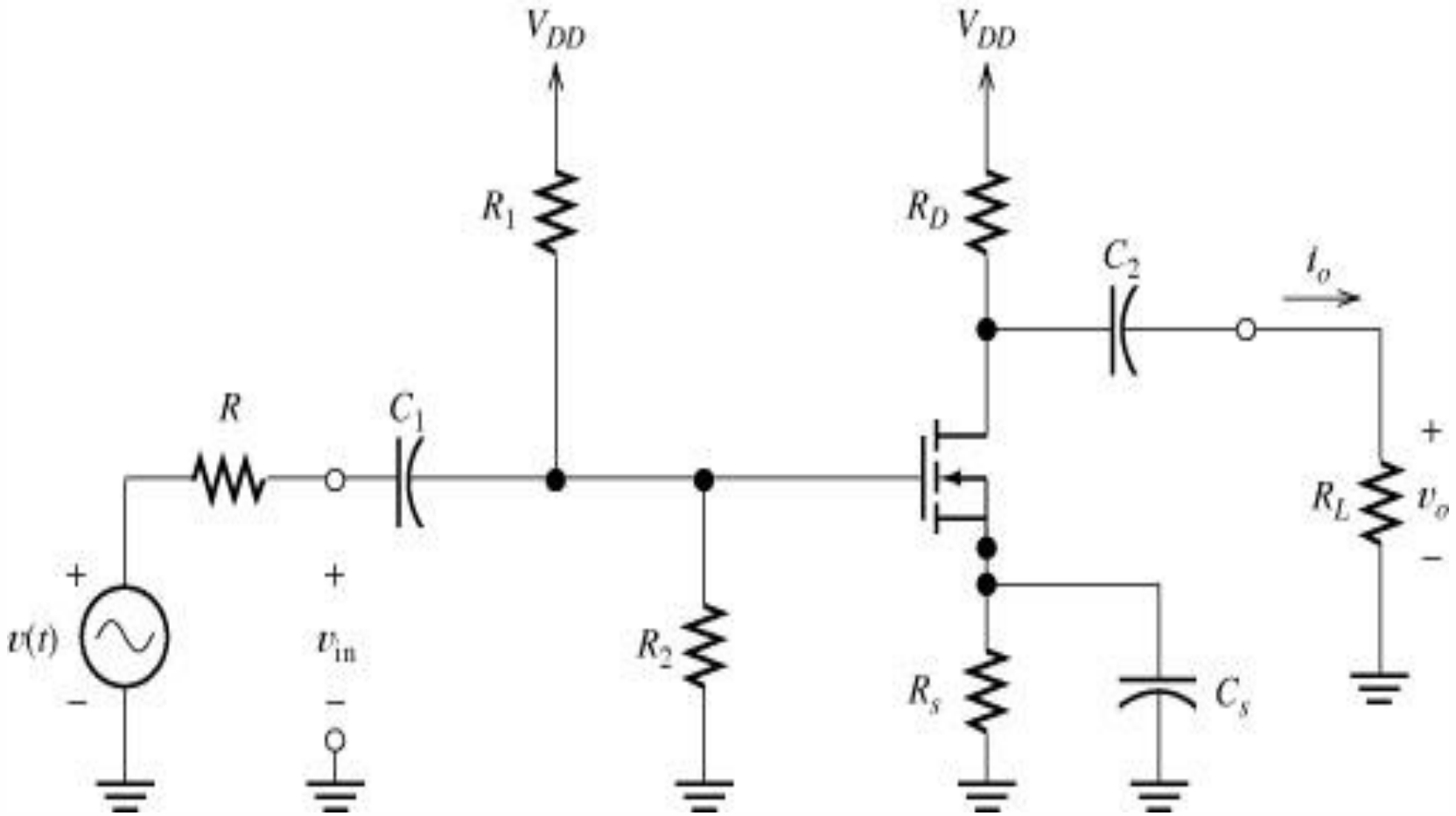
FET Small-signal Equivalent Circuit:



FET as common source amplifier

- **FET as common source amplifier:**
- The design of an amplifier circuit based around a junction field effect transistor or “JFET”, (N-channel FET for this tutorial) or even a metal oxide silicon FET or “MOSFET” is exactly the same principle as that for the bipolar transistor circuit used for a Class A amplifier circuit we looked at in the previous tutorial.
- Firstly, a suitable quiescent point or “Q-point” needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices.
- These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. In this tutorial about FET amplifiers we will look at the popular **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design..

FET as common source amplifier



Common Drain Amplifier

- In CS amplifier analysis we have seen that in order to achieve the high voltage gain the load impedance should be as high as possible. Therefore for low impedance load the buffer must be placed after the amplifier to drive the load with negligible loss of the signal level.

- The source follower thus worked as a buffer stage. The source follower is also called as the common drain amplifier.

- In this circuit, the signal at the gate is sensed and drives the load at the source which allows the source potential to follow the gate voltage. The small signal equivalent circuit of the source follower is shown in Figure below.