Hall Ticket No | | | | | | | | | | |

Question Paper Code: BESB02

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-I

M.Tech I Semester End Examinations, January - 2020

Regulations: IARE-R18

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING

(Embedded Systems)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

		UNIT – I	
1	a)	Describe the main features of the Cortex M3 processor core. And also explain its architecture, instruction set and major internal core blocks.	[7M]
	b)	Illustrate different Registers and Special Registers in Cortex M3 processor.	[7M]
2	a)	Briefly describe the features of the Cortex M3 based microcontrollers memory organization.	[7M]
	b)	What is Pipeline mechanism? Explain briefly the pipeline mechanism in Cortex-M3 Processor.	[7M]
		UNIT – II	
3	a)	Explain about Interrupt Inputs and Pending Behavior in Cortex M3 processor	[7M]
	b)	List out the Interrupt Sequences Stacking, Vector fetch, Register Updates	[7M]
4	a)	Describe the Supervisor and Pendable Service Call exceptions targeted at software and operating systems.	[7M]
	b)	Write a short note on Exception Exits and Tail-Chaining Interrupts.	[7M]
		UNIT – III	
5	a)	Describe the Features and benefits of LPC 17XX Microcontroller.	[7M]
	b)	List out the Features of PWM in LPC 17XX Microcontroller.	[7M]
6	a)	What are the functionalities of LPC 17XX general purpose parallel I/O (GPIO).	[7M]
	b)	Briefly explain about RTC in LPC 17XX Microcontroller.	[7M]
		UNIT – IV	
7	a)	Describe the Harvard architecture of Programmable DSP Processors.	[7M]
	b)	What is ALU of DSP system? Explain briefly ALU of DSP system with a neat block diagram.	[7M]
8	a)	Illustrate the Multi port memory of Programmable DSP Processors.	[7M]
	b)	Explain about circular addressing mode of Programmable DSP Processors?	[7M]
		UNIT – V	
9	a)	Explain in detail about the VLIW architecture with a neat diagram.	[7M]
	b)	Describe the Architectural details and features of a DSP TMS320C6000 processor.	[7M]
10	a)	Discuss the various addressing modes of a digital signal processor TMS320C6000 series.	[7M]
	b)	What is meant by instruction pipelining? How pipelining increases the through efficiency.	[7M]

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COURSE OBJECTIVES:

I	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
II	Identify and characterize architecture of Programmable DSP Processors
III	Develop small applications by utilizing the ARM processor core and DSP processor based platform

COURSE OUTCOMES (COs):

CO 1	Analyze the characteristics of ARM Cortex-M3 processor.
CO 2	Understand the various Exceptions and Interrupts in Cortex-M3 processor.
CO 3	Study the features of LPC 17xx microcontrollers based on Cortex-M3 processor.
CO 4	Identify and analyze the characteristics Programmable DSP Processors.
CO 5	Understand the TMS320C6000 series DSP Processor architectures.

COURSE LEARNING OUTCOMES:

BESB02.01	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.
BESB02.02	Study the Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations.
BESB02.03	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.
BESB02.04	Examine the various Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions
BESB02.05	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.
BESB02.06	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.
BESB02.07	Describe the LPC 17xx microcontroller- Internal memory, GPIOs, Timers.
BESB02.08	Study the features of ADC, UART and other serial interfaces.
BESB02.09	Understand the concepts of PWM, RTC,WDT.
BESB02.10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.
BESB02.11	Study the features of architectural structure of P-DSP- MAC unit, Barrel shifters.
BESB02.12	Understand the Introduction to TI DSP processor family.
BESB02.13	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.
BESB02.14	Understanding the ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence.
BESB02.14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.
BESB02.15	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNING OUTCOMES:

SEE Question No.		CLO Code	Course learning Outcomes	Course Outcome	Blooms Taxonomy Level
1	a	BESB02.01	Understanding the ARM Cortex-M3 processor architecture	CO 1	Understand
	b	BESB02.01	Explain to understand the various registers	CO 1	Understand
2	a	BESB02.02	Study the Instruction Set, Unified Assembler Language, Memory Maps	CO 1	Understand
	b	BESB02.03	Discuss the Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.	CO 1	Understand
3	a	BESB02.04	Understand the different types of interrupts	CO 1	Remember
	b	BESB02.06	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	CO 1	Understand
4	a	BESB02.05	Discuss the Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller.	CO 2	Understand
	b	BESB02.06	Understand the Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.	CO 2	Understand
5	a	BESB02.07	Describe the LPC 17xx microcontroller- Internal memory, GPIOs, Timers.	CO 2	Remember
	b	BESB02.9	Understand the concepts of PWM, RTC, and WDT.	CO 3	Understand
6	a	BESB02.08	Study the features of ADC, UART and other serial interfaces.	CO 3	Remember
	b	BESB02.09	Understand the concepts of RTC	CO 3	Understand
7	a	BESB02.10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	CO 4	Understand
	b	BESB02.10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	CO 4	Remember
8	a	BESB02.10	Describe the Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory.	CO 4	Understand
	b	BESB02.11	Study the Circular addressing mode of Programmable DSP Processors	CO 4	Remember
9	a	BESB02.11	Study the VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths.	CO 5	Understand
	b	BESB02.12	Understand the Introduction to TI DSP processor family.	CO 5	Understand
10	a	BESB02.14	Understand the Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.	CO 5	Understand
	b	BESB02.15	Describe the Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.	CO 5	Understand

Signature of Course Coordinator **HOD, ECE**