Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC017

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER-I

B.Tech VII Semester End Examinations, November - 2019

Regulations: R16

VLSI DESIGN

(ECE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1.	a)	Explain the MOS transistor operation with the help of neat sketches in the Enhancement mode.	**[7M]**
	b)	Consider an nMOS transistor in a 0.6 μm process with W/L = 4/2 λ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 A and the mobility of electrons is 350 cm2/V· s. The threshold voltage is 0.7 V. Plot I_{ds} vs. V_{DS} for V_{GS} = 0, 1, 2, 3, 4, and 5 V.	**[7M]**
2.	a)	What are different parasitic that arise in MOS circuits?	**[7M]**
	b)	Interpret the Pull-up to pull-down ratio (Zpu/Zpd) for an nMOS inverter driven by another nMOS inverter?	**[7M]**

UNIT – II

3.	a)	Draw the fabrication steps of CMOS transistor and explain its operation in detail	**[7M]**
	b)	Realize the function f=(AB+CD)' using nMOS and CMOS logic	**[7M]**
4.	a)	Briefly explain various forms of pull-up circuit ,its advantages and disadvantage of each form?	**[7M]**
	b)	Illustrate the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics	**[7M]**

UNIT – III

5.	a)	What are different reliability issues that occur in CMOS?	**[7M]**
	b)	What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate.	**[7M]**
6.	a)	Compare Full-Custom design with semi-custom design.	**[7M]**
	b)	Draw the Layout for two input XNOR gate.	**[7M]**

UNIT – IV

7.	a)	Explain the basic architecture of FPGA.	**[7M]**
	b)	Explain different wiring capacitance used in Gate level design with example.	**[7M]**

8.	a)	Draw and explain fan in and fan out characteristics of different CMOS design technologies	**[7M]**
	b)	Define transmission gate , realize any function using same gate and write its advantages and disadvantages.	**[7M]**

UNIT – V

9.	a)	Explain the structured design approach of parity generator.	**[7M]**
	b)	Explain the operation of SRAM?	**[7M]**
10.	a)	Briefly explain about different timing issues occur in VLSI?	**[7M]**
	b)	Explain the design of a 4-bit shifter	**[7M]**

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

COURSE OBJECTIVES:

I	Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II	Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III	Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout
IV	Focus in selecting appropriate building blocks of data path for given system.

COURSE OUTCOMES (COs):

CO 1	Explore the basic operations of MOSFET, parameters to be considered which effects the operation of MOS, effect of scaling on MOS devices, how to overcome draw back.
CO 2	Understand various VLSI design styles, fabrication process of MOS, able to Analyze the inverter characteristics, understand the delay, noise margin and power dissipation of MOS transistor.
CO 3	Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up.
CO 4	Understand various gate level designs, analyze various performance parameters like area, speed and capacitance and study the Fan-In and Fan-out.
CO 5	Understand design options for common datapath operators, various memories, low power memories. Analyze various timing issues, clocking strategies of VLSI designs and study various digital designs.

COURSE LEARNING OUTCOMES (CLOs):

AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.
AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
AEC017.03	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
AEC017.04	Understand the basic CMOS nano technology and the importance of it.
AEC017.05	Understand the fabrications steps involved in the MOS transistor.
AEC017.06	Study various inverter characteristics of NMOS, CMOS.
AEC017.07	Understand the effect of delay, noise margin and power dissipation of MOS devices.
AEC017.08	Understand implementation of logic designs using MOS transistors series & parallel circuits.

AEC017.09	Study other logic families like pass transistor logic, Bi-CMOS logic, and various pull-up networks
AEC017.10	Understand to implement layers using stick diagram along with the color representation
AEC017.11	Study the design rules of transistors, wires , contacts and layouts with respect to width, length and spacing based on type of technology
AEC017.12	Understand effects on VLSI Interconnects and electron migration.
AEC017.13	Study the latch up problems and reliability issues of CMOS
AEC017.14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.
AEC017.15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
AEC017.16	Understand the implementation strategies of VLSI design.
AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
AEC017.18	Understand data path subsystem designs, array subsystem designs
AEC017.19	Understand the operation of various static and dynamic latches and registers.
AEC017.20	Analyze the timing issues and the clock strategies of VLSI designs.
AEC017.21	Understand the purpose and operation of Low power memory Circuits
AEC017.22	Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES

SEE Question No.		Course Learning Outcomes		Course Outcomes	Blooms Taxonomy Level
1	a	AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.	CO 1	Understand
	b	AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.	CO 1	Understand
2	a	AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.	CO 1	Understand
	b	AEC017.03	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.	CO 1	Understand
3	a	AEC017.05	Understand the fabrications steps involved in the MOS transistor.	CO 2	Understand
	b	AEC017.08	Understand implementation of logic designs using MOS transistors series & parallel circuits.	CO 2	Remember
4	a	AEC017.09	Study other logic families like pass transistor logic, Bi-CMOS logic and various pull-up networks.	CO 2	Understand
	b	AEC017.06	Study various inverter characteristics of NMOS, CMOS.	CO 2	Understand
5	a	AEC017.13	Study the latch up problems and reliability issues of CMOS.	CO 3	Understand
	b	AEC017.10	Understand to implement layers using stick diagram along with the color representation.	CO 3	Understand
6	a	AEC017.16	Understand the implementation strategies of VLSI design.	CO 3	Understand
	b	AEC017.12	Understand effects on VLSI Interconnects and electron migration.	CO 3	Understand
	a	AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.	CO 4	Understand

7	b	AEC017.15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.	CO 4	Understand
8	a	AEC017.14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.	CO 4	Understand
	b	AEC017.15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.	CO 4	Understand
9	a	AEC017.19	Understand the operation of various static and dynamic latches and registers.	CO 5	Understand
	b	AEC017.18	Understand data path subsystem designs, array subsystem Designs.	CO 5	Understand
10	a	AEC017.20	Analyze the timing issues and the clock strategies of VLSI designs.	CO 5	Understand
	b	AEC017.22	Study various Synchronous and asynchronous circuit design; static and dynamic latches and registers.	CO 5	Understand

Signature of Course Coordinator **HOD, ECE**