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Question Paper Code: AECEB27



# INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal-500043, Hyderabad

B.Tech VII SEMESTER END EXAMINATIONS (REGULAR/SUPPLEMENTARY) - DECEMBER 2022

Regulation: R18

VLSI DESIGN

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours

Max Marks: 70

Answer FIVE Questions choosing ONE question from each module

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

## MODULE – I

- With neat sketches of cross sectional view of MOSFETS, explain the salient steps of n-well CMOS inverter fabrication. [BL: Understand| CO: 1|Marks: 7]
  - Build CMOS circuit for the gates defined by  $Y = \overline{((AB + C)D)}$  and for a 4-input NOR gate. [BL: Apply| CO: 1|Marks: 7]
- Summarize the concept of PMOS fabrication process with neat diagrams and follow the step by step methodology involved in the process. [BL: Understand| CO: 1|Marks: 7]
  - Construct the CMOS inverter schematic circuit, DC characteristics and write the output voltage when the input is varied from 0 to  $V_{DD}$ . Verify the DC characteristics for  $\beta_p / \beta_n = 0.1, 1$  and 10. [BL: Apply| CO: 1|Marks: 7]

## MODULE – II

- Mention one application each of thin oxide and thick oxide in silicon ICs. Explain wet oxidation and dry oxidation process. [BL: Understand| CO: 2|Marks: 7]
  - Design a pseudo-NMOS circuit for a 3-input XOR gate and also draw the circuit for a 3-input CMOS OR/NOR gate. Assume all input are available in both true and complement forms. [BL: Apply| CO: 2|Marks: 7]
- Explain the RESET operation and normal operation in a D-latch and a D-flip flop, with asynchronous reset. [BL: Understand| CO: 2|Marks: 7]
  - Solve a dynamic CMOS logic circuit for  $G1 = \overline{(A_1 A_2 A_3 + B_1 B_2)}$  and a domino CMOS circuit for  $G_2 = (E+F)(C+D)$  [BL: Apply| CO: 2|Marks: 7]

## MODULE – III

- Outline the structure of 4X4 barrel shifter. Explain the following operations on 4-bit input data: i) Rotate right ii) Rotate left iii) Rotate and shift. [BL: Understand| CO: 3|Marks: 7]
  - Construct a 1-bit CMOS full adder expressing sum as a function of carryout. Relate the gate level and transistor level diagrams for the same. [BL: Apply| CO: 3|Marks: 7]

6. (a) With relevant circuit diagram and derivation, show that switching power dissipation in a CMOS circuit is directly proportional square of the power supply used.

[BL: Understand| CO: 4|Marks: 7]

- (b) Make use of RC equivalent circuit of a unit inverter driving another unit inverter. A unit inverter is composed from an nMOS transistor of unit size and a pMOS transistor of twice unitwidth to achieve equal rise and fall resistance. Write the expression for propagation delay,  $t_{pd}$ .

[BL: Apply| CO: 4|Marks: 7]

#### MODULE – IV

7. (a) Demonstrate the general interface diagram for a queue. Also explain the read and write operations in FIFO and LIFO queues.

[BL: Understand| CO: 5|Marks: 7]

- (b) Illustrate a schematic for an 8-word X 2-bit NAND ROM that serves as a lookup table to implement a full adder.

[BL: Apply| CO: 5|Marks: 7]

8. (a) Interpret the schematic and logic diagram for a single bit adder and explain its operation with truth table.

[BL: Understand| CO: 5|Marks: 7]

- (b) Organize a 4-word by 4-bit ROM using pseudo-nMOS pullups with the following contents:

word0: 0000

word1: 0010

word2: 0100

word3: 1000.

Also draw the corresponding dot diagram.

[BL: Apply| CO: 5|Marks: 7]

#### MODULE – V

9. (a) Describe semi custom and full custom design in terms turnaround time and time to market parameters.

[BL: Understand| CO: 6|Marks: 7]

- (b) List the properties of an ideal power distribution networks in a chip. Also draw the power distribution of standard cell layout.

[BL: Apply| CO: 6|Marks: 7]

10. (a) What is meant by logic verification, silicon debug and manufacturing tests? With relevant diagram, explain a typical clock sub-system.

[BL: Understand| CO: 6|Marks: 7]

- (b) Using simple diagram, explain how the H-tree clock distribution network overcome clock skew problem in clock distribution.

[BL: Apply| CO: 6|Marks: 7]

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