Hall Ticket No | | | | | | | | | | | Question Paper Code:AECB44

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
(Dundigal-500043, Hyderabad)

B.Tech VII SEMESTER END EXAMINATIONS (REGULAR/SUPPLEMENTARY) - DECEMBER 2022

Regulation:R18

DIGITAL DESIGN THROUGH VERILOG

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max Marks: 70**

Answer FIVE Questions choosing ONE question from each module
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Explain the following terms in Verilog HDL with the help of an example for each
i) Comments ii) Keywords iii) Numbers iv) Identifiers [BL: Understand| CO: 1|Marks: 7]
(b) Design a 2 bit magnitude comparator to compare two 2-bit data. Write a Verilog dataflow model for the same. [BL: Apply| CO: 1|Marks: 7]

2. (a) Outline the following terms in Verilog HDL i) Module definition ii) Module instantiation. List out different levels of design description available in verilog HDL. [BL: Understand| CO: 1|Marks: 7]
(b) Develop a Verilog structural code and testbench for a 1-bit full adder also write its truth table. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

3. (a) Discuss about the combinational user defined primitives. Write a UDP for a three input OR gate. [BL: Understand| CO: 2|Marks: 7]
(b) Construct the logic diagram and write a Verilog code for a 4:1 multiplexer using gate level modeling. [BL: Apply| CO: 2|Marks: 7]

4. (a) Describe in detail about inertial delay and transport delay used in Verilog with relevant examples. [BL: Understand| CO: 2|Marks: 7]
(b) Make use of Verilog gate level code for a 4-bit parallel adder by instantiating module of 1-bit full adder also draw its block diagram. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

5. (a) Distinguish between blocking and non-blocking assignment statements. Give example for each. List out the advantages and disadvantages of it. [BL: Understand| CO: 3|Marks: 7]
(b) Identify the importance of 'For' loop and 'While' loop. Explain with a relevant Verilog behavioral code for each. [BL: Apply| CO: 4|Marks: 7]

6. (a) Describe in detail about event based timing control in behavioral modeling with examples. [BL: Understand| CO: 4|Marks: 7]

(b) Develop a Verilog HDL model for a 4-bit universal shift register that performs the following functions Table 1 in behavioral level. [BL: Apply| CO: 3|Marks: 7]

Table 1

Mode		control
S1	S0	Register operations
0	0	Parallel load
0	1	Shift right
1	0	Shift left
1	1	Clear all

MODULE – IV

7. (a) Draw the circuit diagram of a CMOS switch using PMOS and NMOS. Outline the switch primitive used for implementing CMOS switch in Verilog. [BL: Understand| CO: 5|Marks: 7]

   (b) Construct a CMOS inverter and write a Verilog switch level code for it using 'NMOS' and 'PMOS' switch primitives. [BL: Apply| CO: 5|Marks: 7]

8. (a) How strength and delays are instantiated? Explain different types of bi-directional gates with the help of their instantiations. [BL: Understand| CO: 5|Marks: 7]

   (b) Design a 2-to-1 Multiplexer by using CMOS switches. Write a Verilog code for 2-to-1 Multiplexer in switch level modeling [BL: Apply| CO: 5|Marks: 7]

MODULE – V

9. (a) What is sequential circuit testing? Draw and explain the general block diagram of an Asynchronous sequential machine. [BL: Understand| CO: 6|Marks: 7]

   (b) The sequential circuit depicted by the state diagram in Figure 1 is a two-bit binary counter controlled by input x_{in} . The output, y_{out}, is enabled when the count reaches binary 11. Write a Verilog behavioral code for the sequential circuit and obtain its testbench. [BL: Apply| CO: 6|Marks: 7]

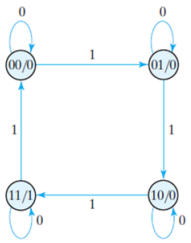

Figure 1

10. (a) How the memory initialization is carried out in Verilog? Explain with the help of an example. [BL: Understand| CO: 6|Marks: 7]

    (b) Build Verilog behavioral model for D flip-flop with Synchronous Reset and Asynchronous Reset and compare the controls of both. [BL: Apply| CO: 6|Marks: 7]