Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB05

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

B.Tech III Semester End Examinations (Regular), February – 2021
Regulation: IARE–R18

ANALOG AND DIGITAL ELECTRONICS

Time: 3 Hours **(CSE | IT)** **Max Marks: 70**

Answer any Four Questions from Part A
Answer any Five Questions from Part B

PART – A

1. Compare the characteristics of half wave rectifier and full wave rectifier. **[5M]**
2. Explain the h parameter model of BJT CE Amplifier. **[5M]**
3. State and prove absorption laws in boolean algebra. **[5M]**
4. Explain in detail about BCD to excess-3 code conversion **[5M]**
5. Explain the operation of serial in and serial out shift register using D-flip flop. **[5M]**
6. Write the expressions for voltage gain, input resistance, current gain and output resistance of CE amplifier. **[5M]**
7. Convert 372.34_8 to hexadecimal system number. **[5M]**
8. Perform the following operation using 2's complement method i) 48 – 23 ii) 23 – 48 **[5M]**

PART – B

9. Explain in detail about the working principle of full wave rectifier with circuit diagram and waveforms. **[10M]**
10. Outline the V-I characteristics of p-n junction diode for forward bias and reverse bias voltages. **[10M]**
11. Demonstrate the working of transistor in common base configurations and draw its input and output characteristics. **[10M]**
12. The h-parameters of a transistor used as an amplifier in the CE configuration are are h_{ie}= 800Ω, h_{re}= 5.4x10^{-4}, h_{fe}=-50 and h_{oe}=80 x 10^{-6}. If the load resistance is 5k Ω Find A_i, R_i, R_o and A_v. **[10M]**
13. Explain what do you mean by error detection and correcting code with examples. **[10M]**
14. Solve the canonical SOP form of the following functions.
    i) Y(A,B,C) = AB+C
    ii) Y(A,B,C,D) = AB+ACD **[10M]**
15. Implement 8 to 1 multiplexer using 2 to 1 multiplexer and 4 to 1 multiplexer. **[10M]**
16. Explain in detail about a bit comparator with the help of logic diagram. **[10M]**
17. Discuss in detail about SR latch and design it using NAND gates. **[10M]**
18. Design a synchronous counter using JKFF to count the following sequence 0, 2, 5, 6, 0….. undesired states 1,3,4,7must go to 0 on the next clock pulse. **[10M]**

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