Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB06

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

B.Tech III Semester End Examinations (Regular), February – 2021

Regulation: IARE–R18

ELECTRONIC DEVICES AND CIRCUITS

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer any Four Questions from Part A
Answer any Five Questions from Part B

PART – A

1. Discuss various current components in a PN junction diode with neat sketches. **[5M]**
2. Briefly explain the input characteristics of common emitter transistor configuration with neat sketches? **[5M]**
3. Explain the concept of fixed biased NPN BJT circuit in detail? **[5M]**
4. Describe various characteristics of n-channel JFET circuits in detail? **[5M]**
5. List out and explain the breakdown mechanisms in semiconductor devices in detail. **[5M]**
6. List the differences between ideal diode and practical diode. **[5M]**
7. A JFET has V_P = -4.5 V, I_{DSS} = 10 mA and I_{DS} = 2.5 mA, Determine the transconductance? **[5M]**
8. Outline the circuit diagram of a fixed bias circuit of CE amplifier. **[5M]**

PART – B

9. Explain the working principle of halfwave rectifier. Determine expressions for I_{DC}, I_{rms} and V_{DC}. **[10M]**
10. Calculate the dynamic forward and reverse resistance of a p-n junction diode, when the applied Voltage is 0.25 V, -0.25 V for germanium diode. If I_0 = 1μA and at T= 300 ° K. **[10M]**
11. What is meant by base width modulation of a transistor circuit? explain the input and output characteristics of common base transistor configuration with neat sketches? **[10M]**
12. For a PNP transistor the base current is 45 μA and collector current is 5.45 mA. Determine the Values of α, β and I_E. **[10M]**
13. With neat sketches for a common emitter NPN transistor amplifier with self biasing model, determine the input impedance, forward current gain from the small signal. equivalent h-parameter model of CE mode BJT amplifier? **[10M]**
14. An NPN transistor with β =50 is used in a common emitter circuit with V_{cc}=10V, R_c=2KΩ. The bias is obtained by connecting a 100KΩ resistance from collector to base. Assume V_{BE}=0.7V. Solve i) The quiescent point ii) The stability factor S. **[10M]**
15. Explain the operation of N-channel enhancement mode- MOSFET in detail with neat sketches? **[10M]**
16. A common Source n-channel JFET circuit with R_D = 3.5 KΩ, R_G = 2 MΩ, V_{GG} = -3 V, I_{DSS}= 12 mA, V_{DD} = 35 V, V_P= -6 V. Find out the V_{DS} , I_D for the JFET Circuit? **[10M]**
17. With the neat sketches draw and explain the common source n-channel JFET amplifier circuit and find out the voltage gain from the AC equivalent circuit of JFET? **[10M]**
18. A Zener voltage regulator has variable load R_L , required load current to vary 10 mA to 85 mA. If V_Z = 10V, I_{Zmin} = 15 mA, I_{Zmax} = 100 mA and the series resistance R_S = 40 Ω. Calculate the range of DC voltage variation permissible and power dissipation? **[10M]**