Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB07

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

B.Tech III Semester End Examinations (Regular), February – 2021

Regulation: IARE–R18

DIGITAL SYSTEM DSIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer any Four Questions from Part A
Answer any Five Questions from Part B

PART – A

1. Convert the following codes
   i) $(215)_{10}$ to octal
   ii) $(1001011101)_2$ to a hexadecimal **[5M]**
2. Design a BCD adder with the help of truth table. **[5M]**
3. Design a Moore type sequence generator to detect a sequence 101. **[5M]**
4. Draw and explain CMOS NAND and NOR. **[5M]**
5. Discuss in detail about configuration declaration, package and generic **[5M]**
6. Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. i) 100 – 110000 ii) 11010 - 1101. **[5M]**
7. Compare logic families of CMOS and TTL with their specifications. **[5M]**
8. Write a VHDL code for a gated D-Latch **[5M]**

PART – B

9. Convert AB'C + A'B' + ABCD to standard SOP form. **[10M]**
10. Simplify F(A,B,C,D) = π(0,1,2,4,5,12,13,8,9). **[10M]**
11. Discuss in detail about magnitude comparator with the help of truth table and logic diagram. **[10M]**
12. Describe about 4 to 1 Multiplexer with the help of logic diagram. **[10M]**
13. Illustrate the operation of master slave JK flip flop with neat diagram. **[10M]**
14. Explain the operation of serial in serial out shift register using D-flip flop. **[10M]**
15. Give the classification of PLDs and list the major differences between PLA and PAL. **[10M]**
16. Implement the following boolean expression using 3 input, 3 product terms and 2 outputs using PLA
    F_1= AC + BC
    F_2= AC + AB' **[10M]**
17. Write VHDL code for a 2 to 4 decoder circuit. Use sequential architecture model. **[10M]**
18. Write architecture body of R-S flip flop using behavior model. Assume 10ns delay time. **[10M]**