Hall Ticket No | | | | | | | | | | | Question Paper Code: AECB27

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech VII SEMESTER END EXAMINATIONS (REGULAR) - FEBRUARY 2022
Regulation: R18
VLSI DESIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer FIVE Questions choosing ONE question from each module
(NOTE: Provision is given to answer TWO questions from any ONE module)
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) What is the difference between CMOS and NMOS. Explain NMOS fabrication process with neat diagrams. **[7M]**
   (b) Outline the derivation of the expression for drain current of MOSFET in linear/non saturation region. **[7M]**
2. (a) What is pull down device in CMOS inverter? Enumerate about various steps in n-well process of CMOS. **[7M]**
   (b) For a CMOS inverter, show the shift in the transfer characteristic curve when B_n/B_p ratio is varied from 1/1 to 10/1. **[7M]**

MODULE – II

3. (a) Design the transistor level schematic and stick diagram for OAI22(OR AND inverter) gate. **[7M]**
   (b) Design 4-input logical expression $Y_b = \overline{(PQ + R)S}$ using CMOS gate design. **[7M]**
4. (a) Mention two applications of SiO_2 in silicon ICs. How oxidation of silicon is achieved? Explain. **[7M]**
   (b) Design dynamic CMOS logic circuit for $G_1 = \overline{A(B + C)}$ and domino CMOS circuit for $G_2 = AB$. **[7M]**

MODULE – III

5. (a) Name the sources of static power dissipation in a CMOS inverter. Also derive an expression for switching power dissipation in a CMOS inverter. **[7M]**
   (b) Design a pseudo-NMOS circuit for 2-input NAND gate and CVSL circuit for 2 input AND/NAND gate. **[7M]**
6. (a) Write a short note on logical effort of a gate. Also determine the logical effort of a 3-input NAND gate and 3-input NOR gate. **[7M]**
   (b) Design a 1-bit full adder using 28 MOSFETs. Draw the corresponding gate level and transistor level diagram for the same. **[7M]**

MODULE – IV

7. (a) Draw the structure of 4-bit magnitude comparator and explain the comparison operation. **[7M]**

(b) Design 4-word by 4-bit ROM using pseudo-nMOS pullups with thefollowing contents:
word0: 0000
word1: 0010
word2: 0100
word3: 1000.
Also draw the corresponding dot diagram. **[7M]**.

8. (a) Draw the circuit of 6T SRAM cell. Explain the read and write operation. **[7M]**

(b) Design AND/OR PLA for 1-bit full adder. Also draw the pseudo NMOS schematic of the same. **[7M]**

MODULE – V

9. (a) Draw and explain the functional block diagram of CPLD with its applications. **[7M]**

(b) Describe and compare between channeled gate array and channel less gate array. **[7M]**

10. (a) List important elements of FPGA. Describe the features of FPGA with functional block diagram. **[7M]**

(b) How the V_{DD} and GND are distributed in a standard cell? Explain. What are the properties of an ideal power distribution networks in a chip? **[7M]**

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