Hall Ticket No | | | | | | | | | | | Question Paper Code: ACSB07

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

B.Tech IV Semester End Examinations (Regular/Supplementary) - July, 2021

Regulation: R18

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **(CSE|IT)** **Max Marks: 70**

Answer FIVE Questions choosing ONE question from each module
(NOTE: Provision is given to answer TWO questions from any ONE module)
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) List the various components of computer system and explain with neat diagram. **[7M]**
   (b) Explain briefly memories organized in hierarchy .Describe the factors to be considered while selecting a particular memory type and draw a suitable diagram. **[7M]**
2. (a) Describe the difference between the general purpose register and accumulator and stack processor architecture. **[7M]**
   (b) Explain instruction set architecture and design a simple set architecture with an example .**[7M]**

MODULE – II

3. (a) State the use of buffers? Explain about tri-state buffers. Explain about high impedance state. **[7M]**
   (b) Define addressing modes. Give the details of different addressing modes with examples. **[7M]**
4. (a) Define control memory unit and with a neat sketch explain the organization of a micro programmed control unit. **[7M]**
   (b) Describe registers selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. **[7M]**

MODULE – III

5. (a) Explain interrupts handled by a basic computer and interrupt cycle with a flowchart. **[7M]**
   (b) Explain the differences between direct and indirect addressing instructions with example for each with the required memory reference. **[7M]**
6. (a) Write the logic diagram of 4-bit carry look ahead adder. Explain the operation. **[7M]**
   (b) Explain about following floating point representations. i)Single-precision format ii)Double-precision format **[7M]**

MODULE – IV

7. (a) Explain about direct and set associative mapping techniques in cache memory. **[7M]**
   (b) Draw and explain the block diagram of DMA controller. **[7M]**
8. (a) Compare paging and segmentation mechanisms for implementing the virtual memory. **[7M]**
   (b) Explain strobe control in asynchronous data transfer along with hand shaking problem? **[7M]**

MODULE – V

9. (a) What is cache coherence and why is it important in shared memory Multiprocessor systems? How can the problem be solved with a snoopy cache controller? **[7M]**

   (b) What is instruction pipelining? What are the conflicts that occurred during instruction pipelining? **[7M]**

10. (a) Define parallel processing and explain the flynn's classification of computer with suitable diagram. **[7M]**

    (b) List the different kinds of multi stage switching networks? Explain with neat sketch. Compare their functioning. **[7M]**

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