



# INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech IV Semester End Examinations (Regular), November – 2020

Regulation: IARE–R18

## COMPUTER ORGANIZATION AND ARCHITECTURE

**Time: 2 Hours**

**(CSE | IT )**

**Max Marks: 70**

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**Answer any Four Questions from Part A**

**Answer any Five Questions from Part B**

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### PART – A

1. How does instruction set architecture work? [5M]
2. Brief about the register transfer language. [5M]
3. What are data transfer instructions give an example? [5M]
4. With a neat diagram, describe auxiliary memory. [5M]
5. What is pipelining? Name the two pipeline organizations. [5M]
6. Explain about the CPU organization. [5M]
7. Mention the types of shifts micro-operations. Explain [5M]
8. Elaborate the synchronization concept used in inter processor communication. [5M]

### PART – B

9. List and explain the functional units of a computer with a neat diagram. [10M]
10. Discuss about the computer levels of programming languages. [10M]
11. Write in detail the different addressing modes in computer architecture with suitable examples. [10M]
12. Discuss the principle operation of micro programmed control unit. [10M]
13. Draw the flowchart for Booth's algorithm for multiplication of signed 2's complement numbers and explain with an example. [10M]
14. Discuss in detail about the memory reference instructions of a basic computer. [10M]
15. What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory. [10M]
16. Discuss the different mapping techniques used in cache memories and their relative merits and demerits. [10M]
17. A nonpipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved [10M]
18. What are the various physical forms available for establishing an interconnection network? Explain. [10M]