Hall Ticket No | | | | | | | | | | | Question Paper Code: AECC12

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR / SUPPLEMENTARY) - AUGUST 2023
Regulation: UG-20
IC APPLICATIONS
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 Hours **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) With neat diagram derive the AC performance characteristics of OP-Amp to discuss on the circuit bandwidth, frequency response and slew rate. [BL: Understand| CO: 1|Marks: 7]

   (b) Determine the output voltage of a differential amplifier for the input voltages of 300μ volts and 240μ volts, the differential gain of the amplifier is 5000 and the value of the CMRR is i) 100 and ii) 105. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Draw the circuit diagram of an instrumentation amplifier. Explain its operation and applications. [BL: Understand| CO: 2|Marks: 7]

   (b) A sine wave of 0.5 V peak voltage is applied to an inverting amplifier using $R_1 = 10k$ and $R_f = 50k$. It uses the supply voltages of $\pm$ 12V. Determine the output and sketch the waveform. If now the amplitude of input sine wave is increased to 5V, what will be the output? Is it practically possible? Sketch the waveform. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Demonstrate monostable multivibrator with necessary diagrams and obtain the expressions for ON time and recovery time. [BL: Understand| CO: 3|Marks: 7]

   (b) Design a stable multivibrator circuit to generate output pulses of 25%, 50% duty cycle using a 555 timer IC, with choice of $C = 0.01\mu F$, frequency as 4.0 kHz. [BL: Apply| CO: 3|Marks: 7]

4. (a) Demonstrate the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. [BL: Understand| CO: 4|Marks: 7]

   (b) Design a second order low pass filter using operational amplifier for the upper cut off frequency of 2 KHZ. Assume the value of capacitor to be 0.1 μF. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Outline the following data conversion techniques.
   i) Flash type ADC ii) Weighted resistor DAC [BL: Understand| CO: 5|Marks: 7]

   (b) An 8-bit A/D converter accepts an input signal voltage of range 0 to 9 V. What is the minimum value of the input voltage required for generating a change of 1 least significant bit? Specify the digital output for an input voltage of 4V. What input voltage will generate all 1s at the A/D converter output? [BL: Apply| CO: 5|Marks: 7]

6. (a) List different ADC and DACs. Describe in detail on the dual slope type analog to digital converter. [BL: Understand| CO: 5|Marks: 7]

   (b) A dual slope ADC has a full scale input of 2 volts. It uses an integrating time of 10 ms and integrating capacitor of 0.1 μF the maximum magnitude of the integrator output should not exceed 3V. Calculate the value of the integrating resistor. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Demonstrate the operation of universal shift register with neat block diagram. [BL: Understand| CO: 6|Marks: 7]

   (b) Design a synchronous counter with the following sequence: 0, 1, 3, 5, 7,..... using JK flip flop. [BL: Apply| CO: 6|Marks: 7]

8. (a) List the characteristics of digital gates. Discuss the CMOS transmission gate and CMOS tri state outputs. [BL: Understand| CO: 6|Marks: 7]

   (b) Design a 3-bit binary counter using T flip-flop. Give the state table, state diagram and logic diagram. [BL: Apply| CO: 6|Marks: 7]