Hall Ticket No | | | | | | | | | | | Question Paper Code: AECC16

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR/SUPPLEMENTARY) - AUGUST 2023
Regulation: UG-20
DIGITAL ELECTRONICS

Time: 3 Hours **(ELECTRICAL AND ELECTRONICS ENGINEERING)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Describe the operation of TTL with neat circuit diagram and mention its application and advantages. [BL: Understand| CO: 1|Marks: 7]
   (b) What is tri-state logic? Discuss the operation of tri-state logic. Mention its importance in digital system. [BL: Understand| CO: 1|Marks: 7]

MODULE – II

2. (a) Discuss the operation of parity checker/generator with necessary truth table, K-Map and draw the logic diagram. [BL: Understand| CO: 2|Marks: 7]
   (b) Describe in detail about full adder circuit with the help of truth table and why this is very important compared to multiplier in digital system. [BL: Understand| CO: 2|Marks: 7]

MODULE – III

3. (a) Write about latch and flip flop. Explain about bi-stable latch and the clocked SR flip flop with suitable diagram. [BL: Understand| CO: 3|Marks: 7]
   (b) Design a synchronous counter using JK flip flop to count the following sequence 0, 2, 5, 6 undesired states 1,3,4,7 must go to 0 on the next clock pulse. [BL: Apply| CO: 3|Marks: 7]

4. (a) Outline bit ring counter using D flip flop. Give its applications and advantages over other counters. [BL: Understand| CO: 4|Marks: 7]
   (b) Design a synchronous decade counter using JK flip flop. Illustrate the operation of serial in serial out shift register using D-flip flop. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) List the broad classification of ADCs. Discuss weighted resistor converter and R-2R Ladder D/A converter. [BL: Understand| CO: 5|Marks: 7]
   (b) Mention the performance parameters of DAC. Explain the operation of A/D converter using voltage to frequency method [BL: Understand| CO: 5|Marks: 7]

6. (a) What are the major building blocks of A/D converter? Explain the specifications of A/D and D/A converters. [BL: Understand| CO: 5|Marks: 7]

(b) Find the digital output of an ADC having t1 as 83.33ms and Vr as 100mv for an input voltage of +100mv.The clock frequency is 12KHz. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Draw the full adder circuit with truth table. Discuss in detail about the READ/WRITE operations in RAM. [BL: Understand| CO: 6|Marks: 7]

   (b) Elucidate complex programmable logic devices (CPLDs) with necessary block diagram. Whether CPLD's are volatile or non volatile. [BL: Understand| CO: 6|Marks: 7]

8. (a) Discuss in detail about the charge coupled device memory (CCD). Differentiate programmable array logic and programmable logic array. [BL: Understand| CO: 6|Marks: 7]

   (b) Explain about different programmable logic devices (PLD's). Design a BCD to excess-3 code converetrs and implement using suitable PLA. [BL: Apply| CO: 6|Marks: 7]